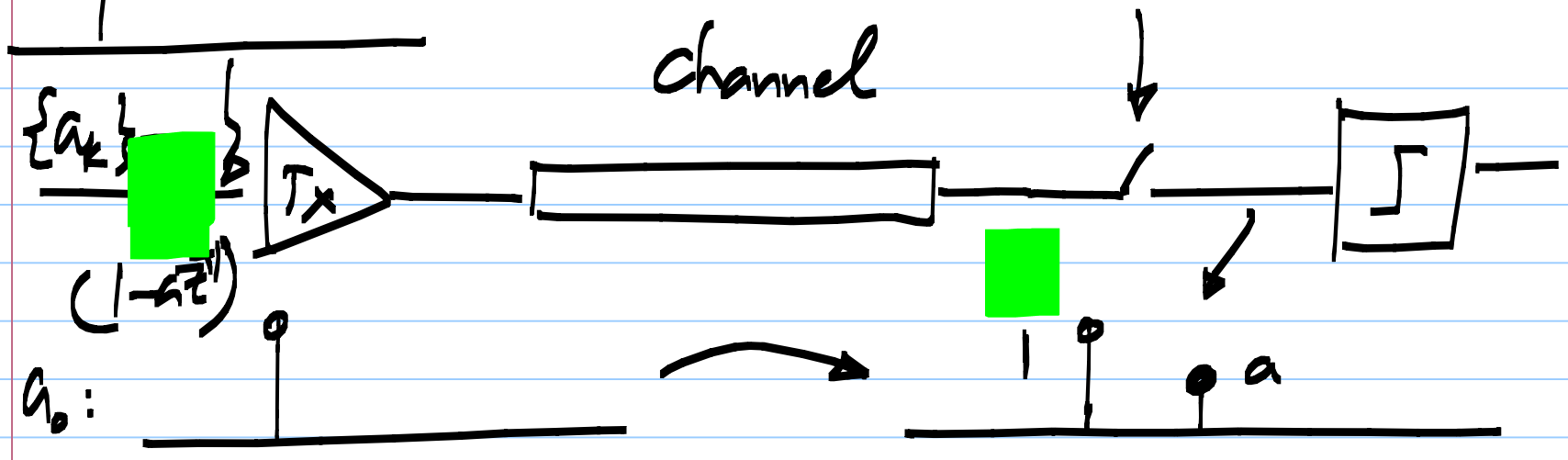
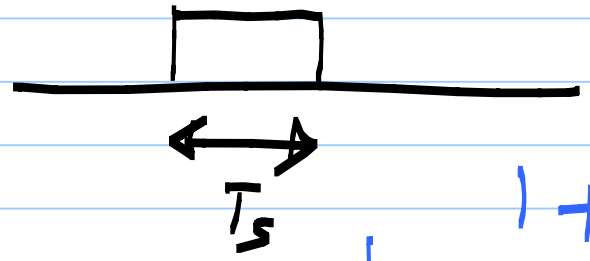
Equalization:



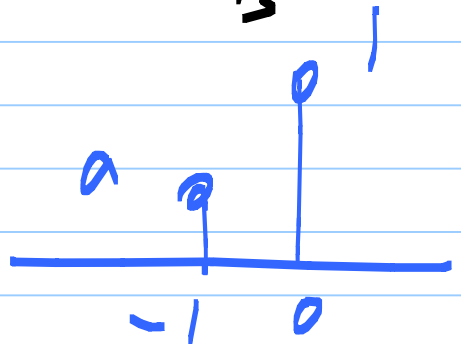
$$(1+az^{-1}) \cdot H(z) \simeq 1$$

H_{Tx}



$$H(z) = \frac{1}{1+az^{-1}}$$

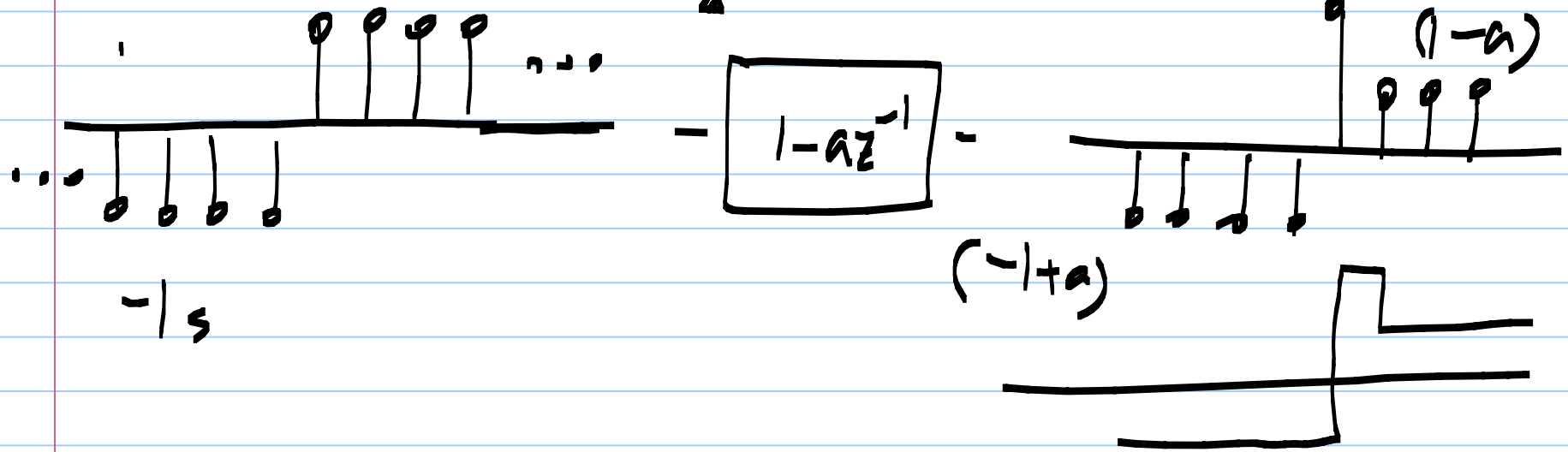
$$1+az$$

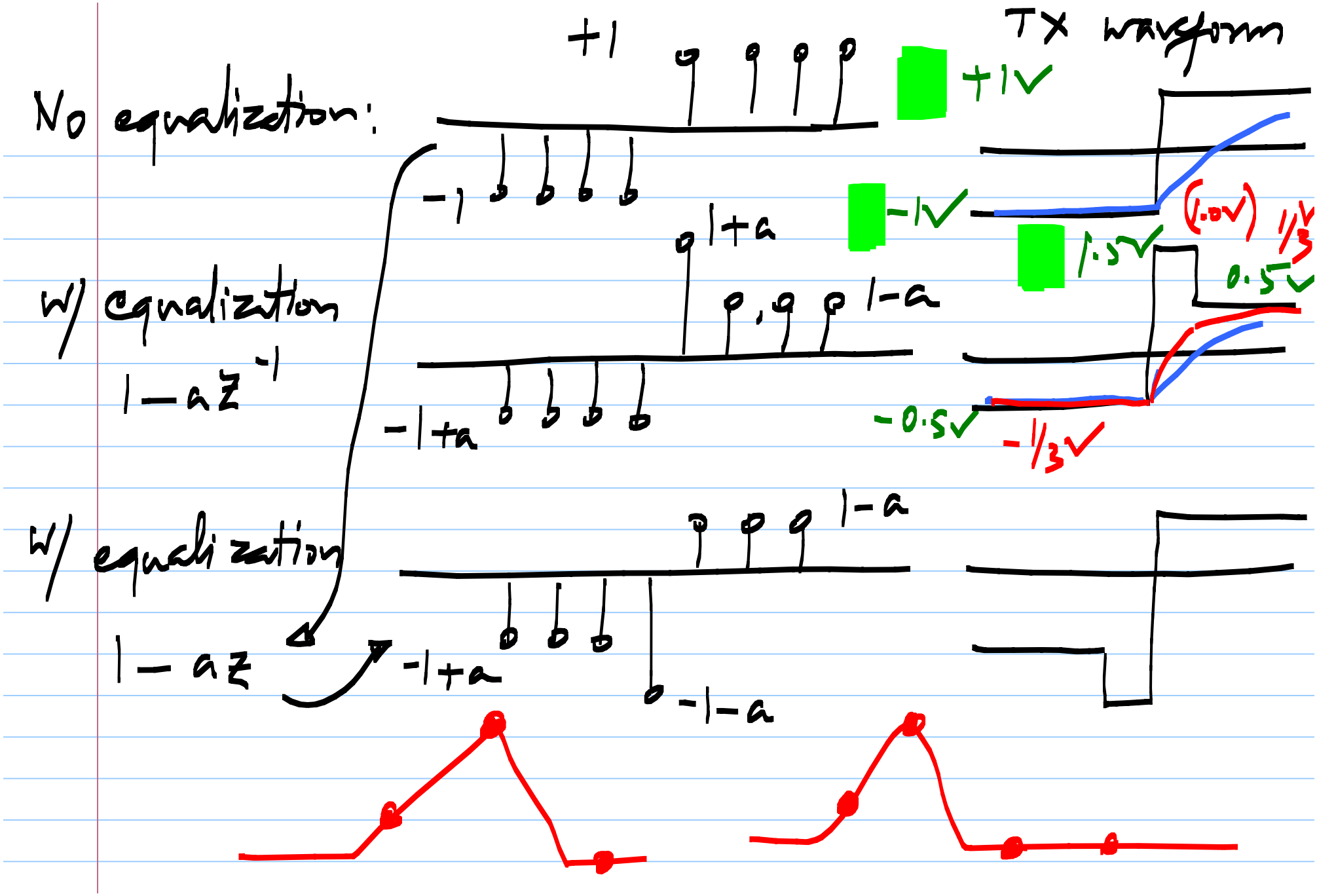


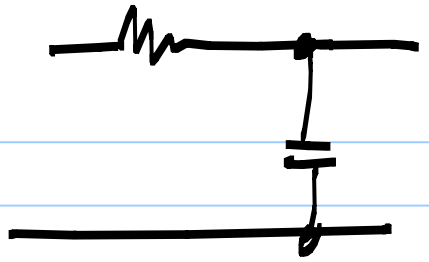
$$1-az \simeq \underbrace{1-az^{-1}+(az^{-1})^2-\dots}$$

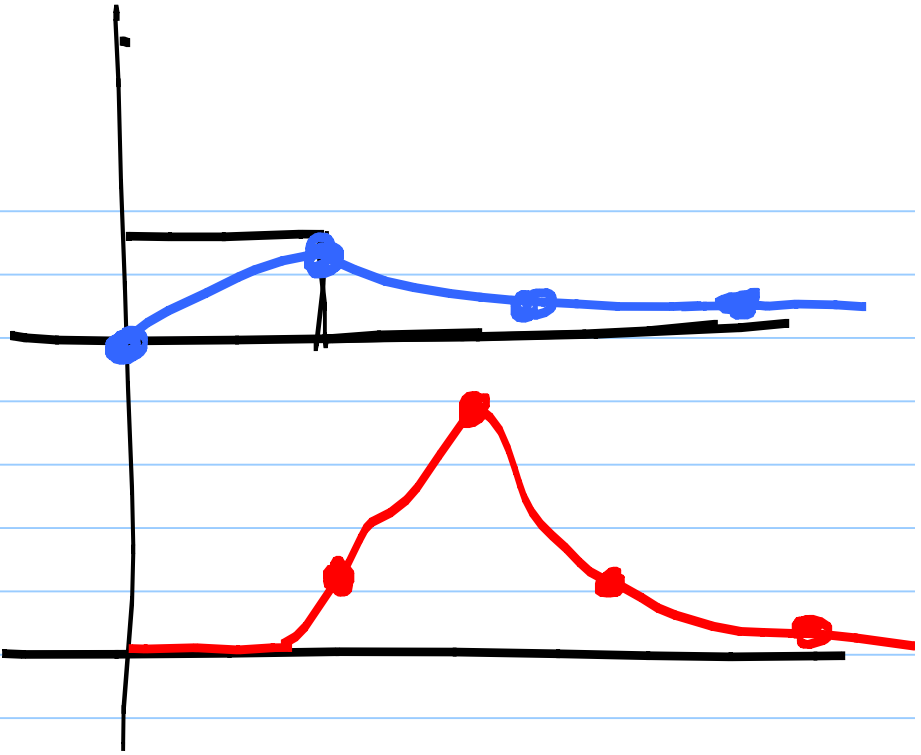
$$\underbrace{(1+az^{-1})}_{\text{Channel + Tx}}\ \underbrace{(1-az^{-1})}_{\text{Equalizer}} = \underbrace{1-a^2z^{-2}}_{\text{Smaller ISI than the original}}$$

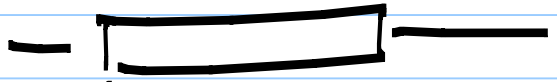
Case if $a < 1$



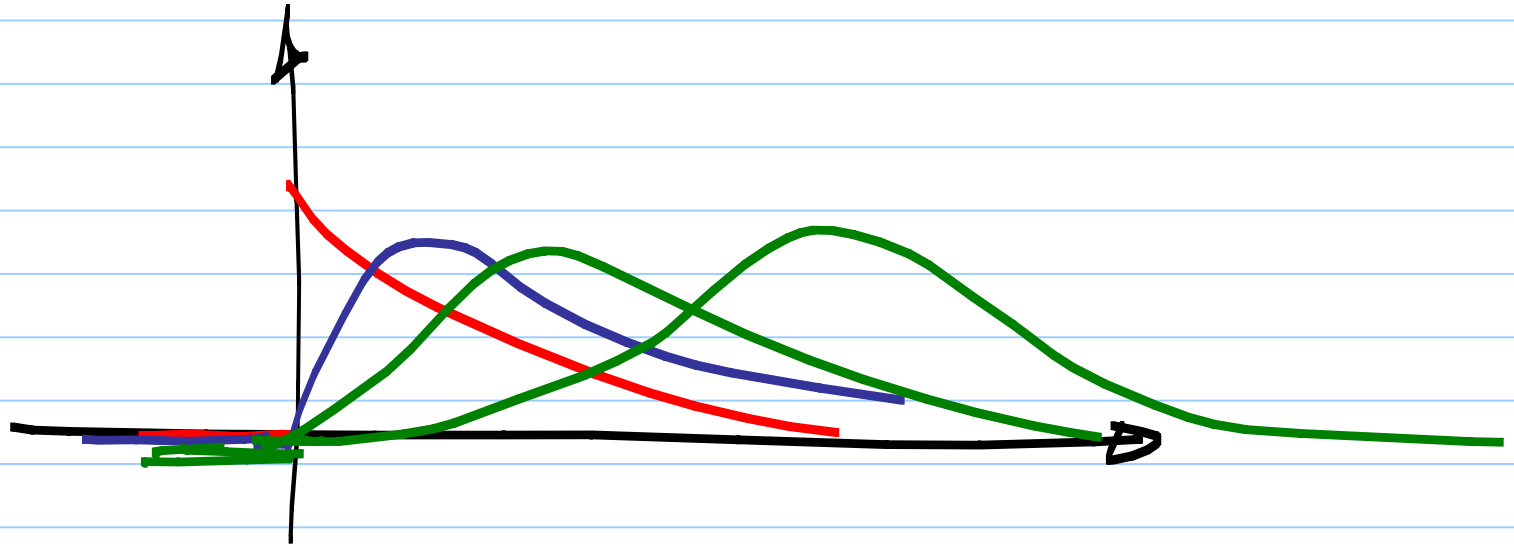

No equalization:
w/ equalization
$1 - aZ^{-1}$
w/ equalization
$1 - aZ$
+1
-1
1+a
-1+a
1-a
-1-a
TX waveform
+1V
-1V
1.5V
(1.0V)
1/3
0.5V
-0.5V
-1/3V







higher order



$$H_{Tx}(z) = 1 + \sum_{k=k_1,\, k\neq 0}^{k_2} a_k z^{-k}$$

Max. possible value $\longrightarrow$ $1 + \sum_{k\neq 0} |a_k|$

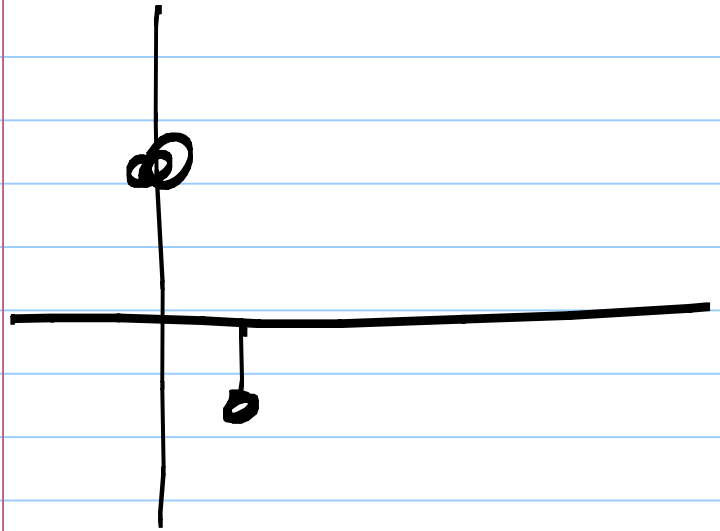
$\{a_k\}$

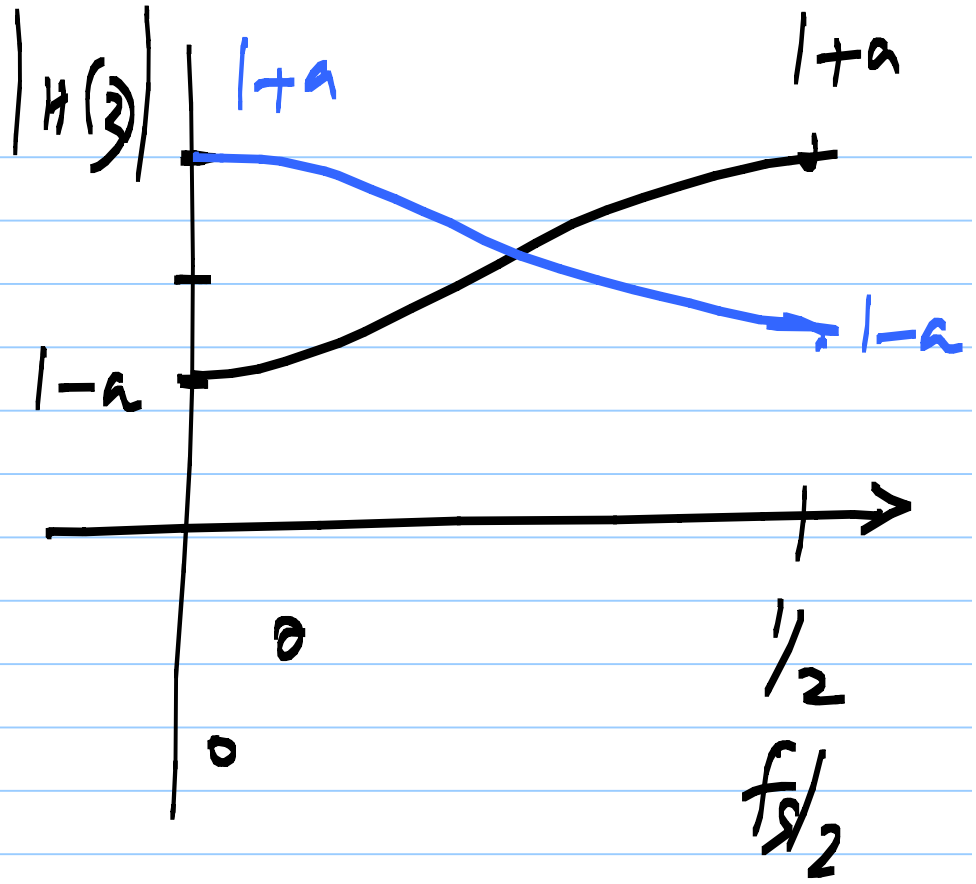
± 1

dc gain: $1 + \sum_{k\neq 0} a_k$

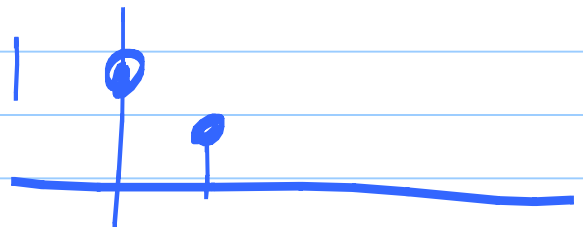
Equalizer: $1 - az^{-1}$

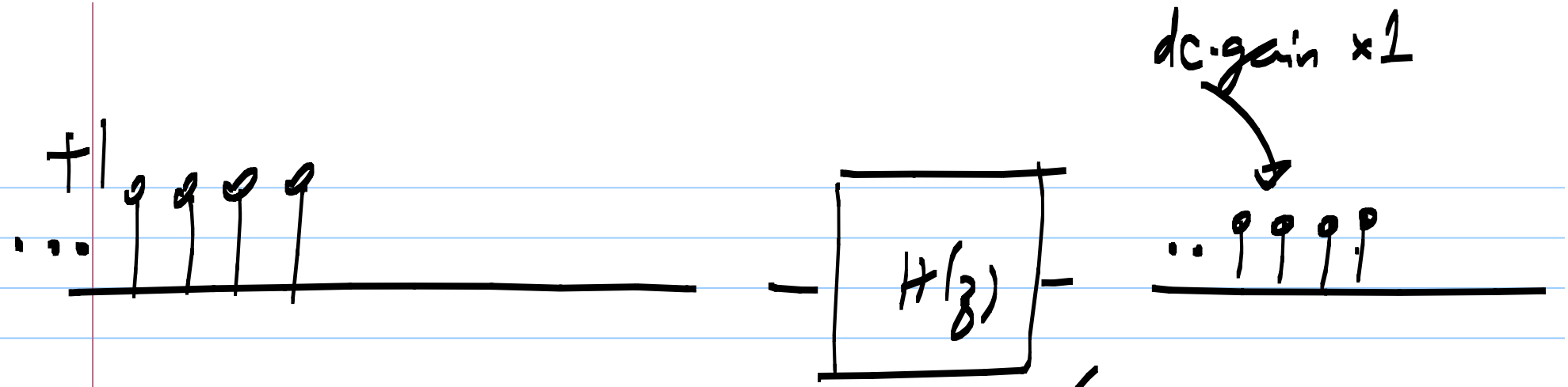
$a > 0$





Channel: $1 + az^{-1}$



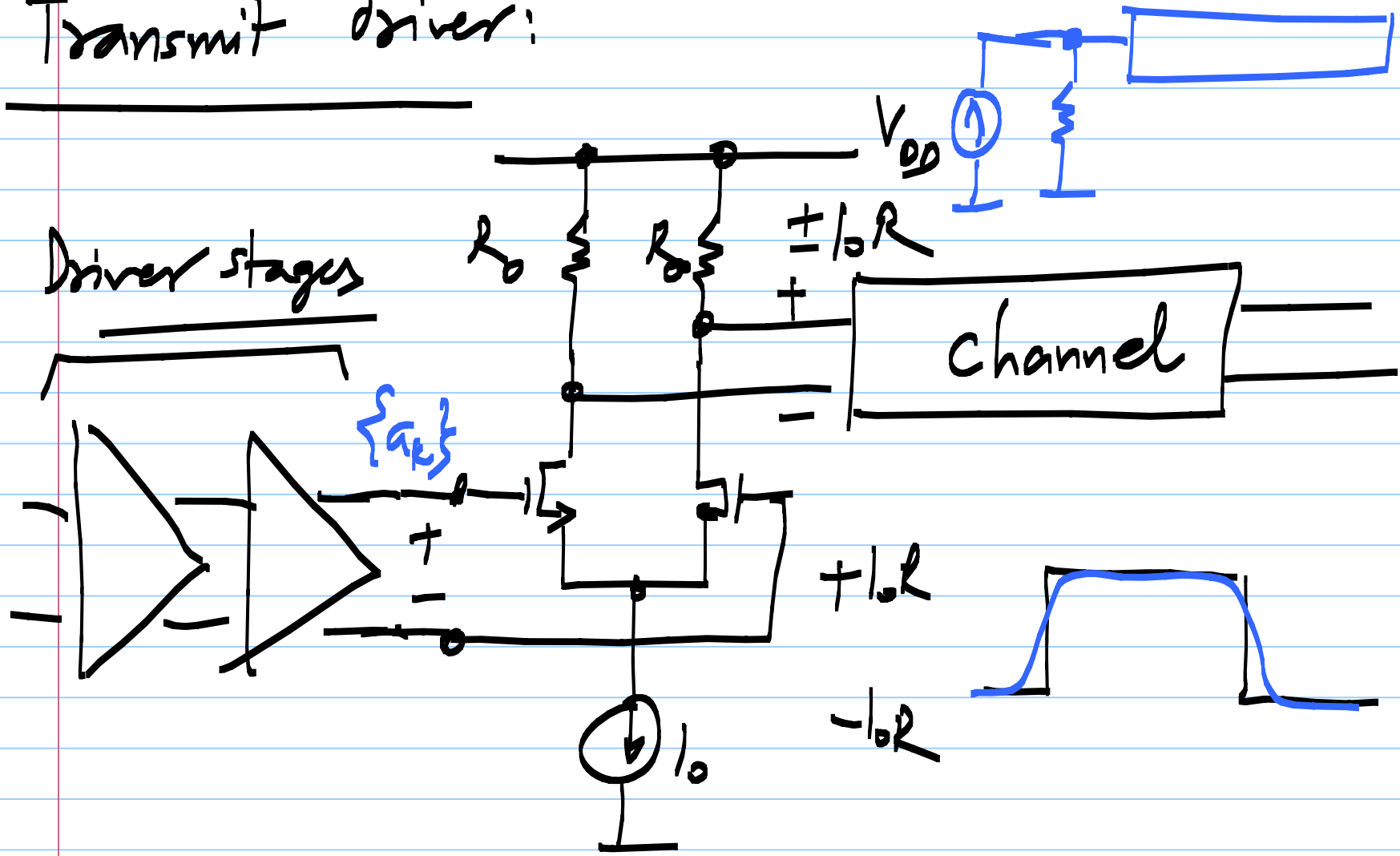


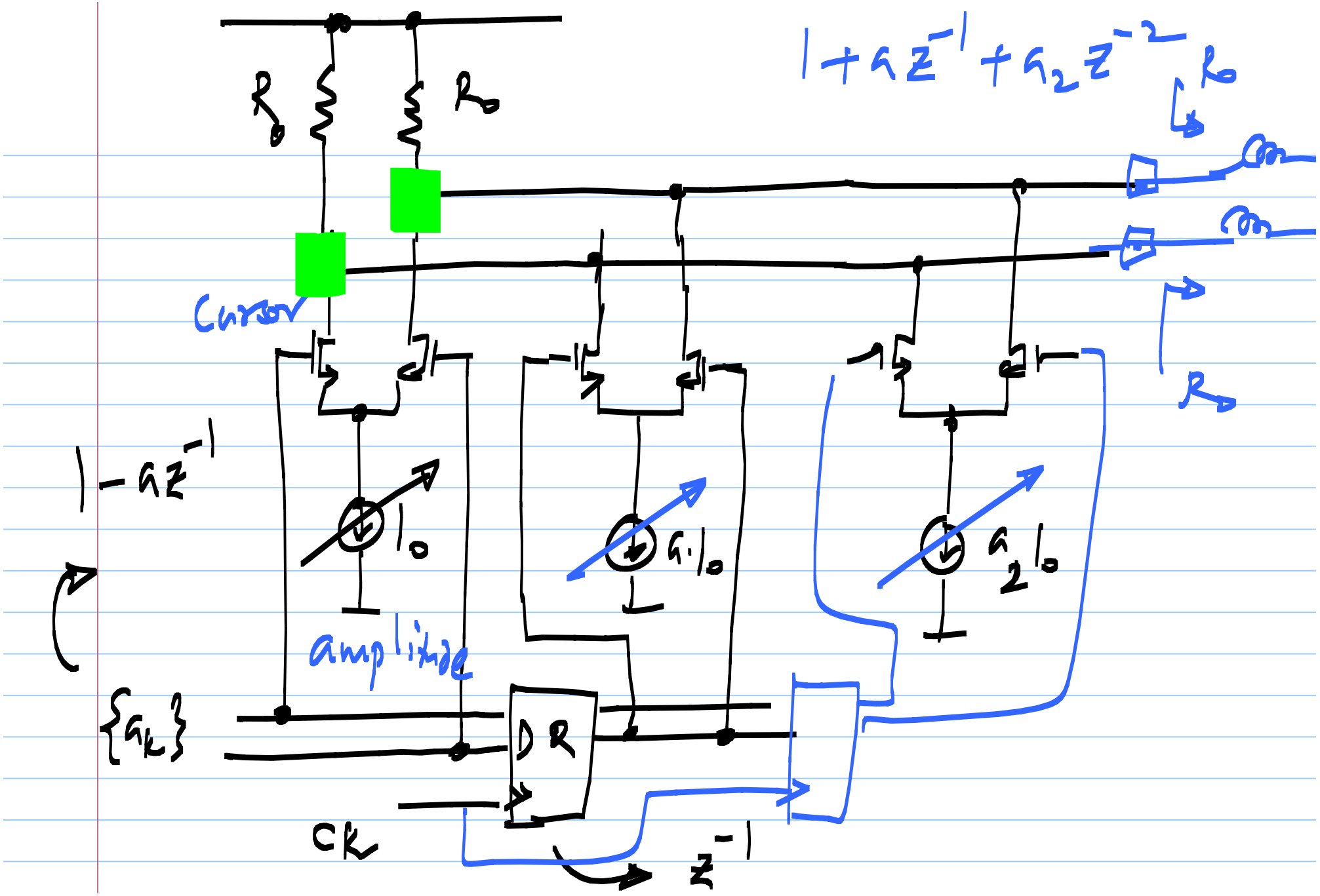
$$1 + \sum_{k \neq 0} |a_k| \xrightarrow{\text{Scale}} 1 \qquad \left(\begin{array}{c}\text{max. value} \\ \text{constraint}\end{array}\right)$$

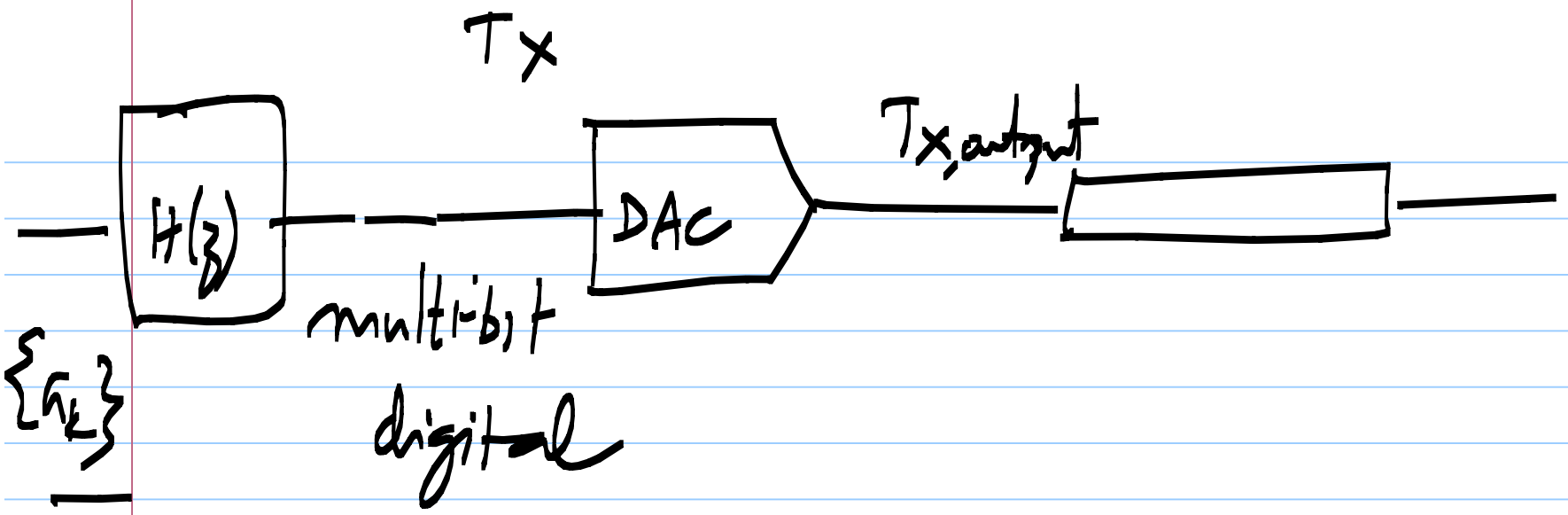
$$\text{dc gain:} \quad \frac{1 + \sum_{k \neq 0} a_k}{1 + \sum_{k \neq 0} |a_k|}$$

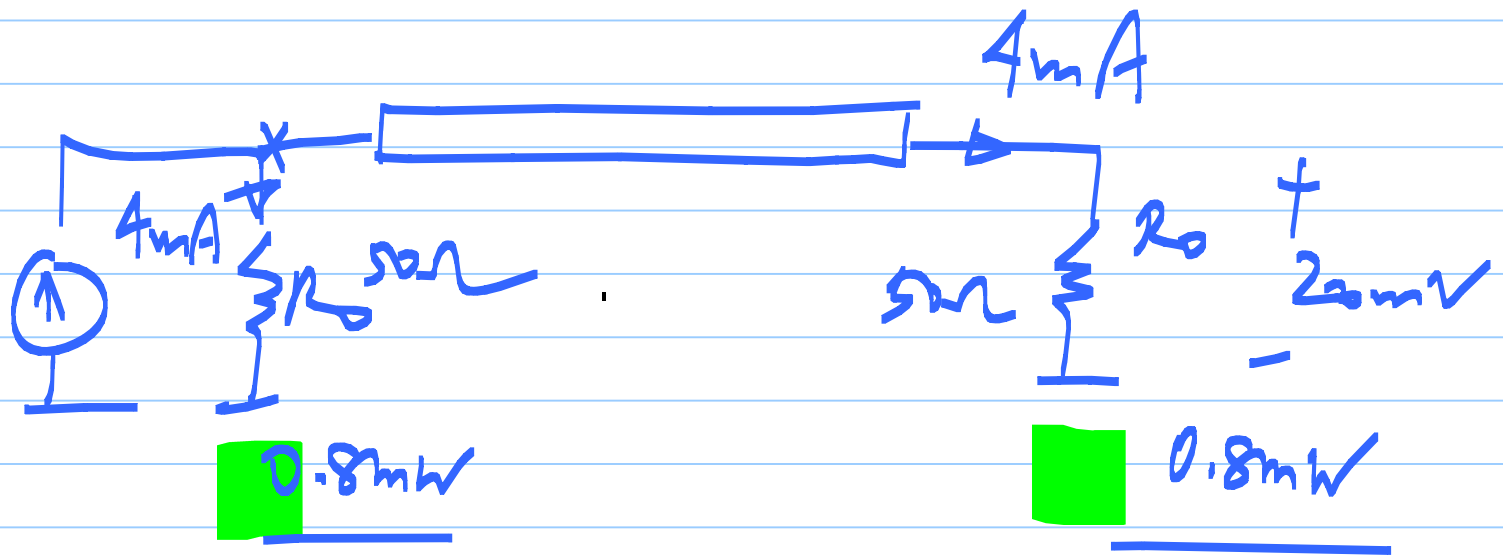
Semi digital FIR equalizer in the transmitter

Transmit driver:




$1+a_1z^{-1}+a_2z^{-2}$
R_0
R_0
R_0
R_0
Cursor
$1-az^{-1}$
I_0
$a_1 I_0$
$a_2 I_0$
amplitude
$\{a_k\}$
DR
CK
z^{-1}


Tx
H(z)
DAC
Tx, output
multi-bit
digital
{c_k}


4mA
4mA
50Ω
50Ω
R_o
+
2mV
−
0.8mW
0.8mW