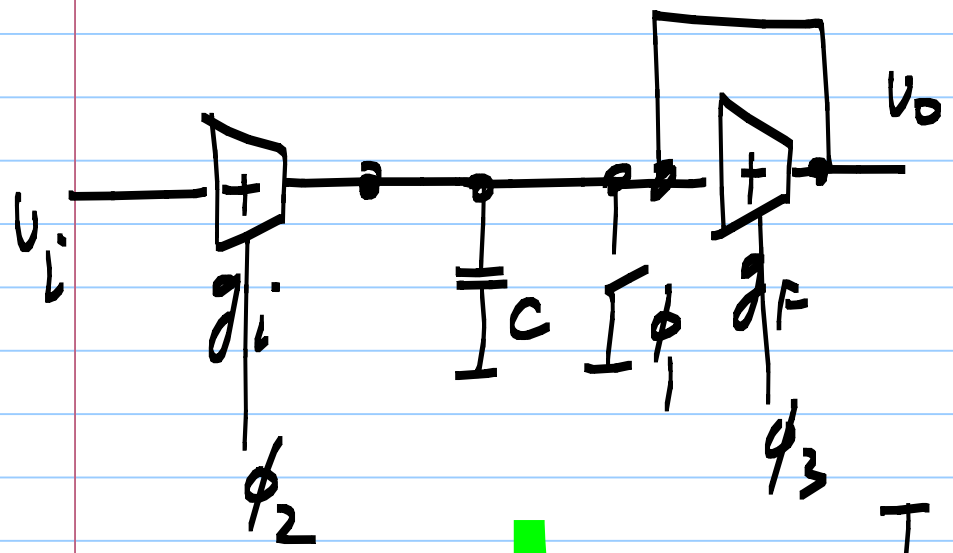
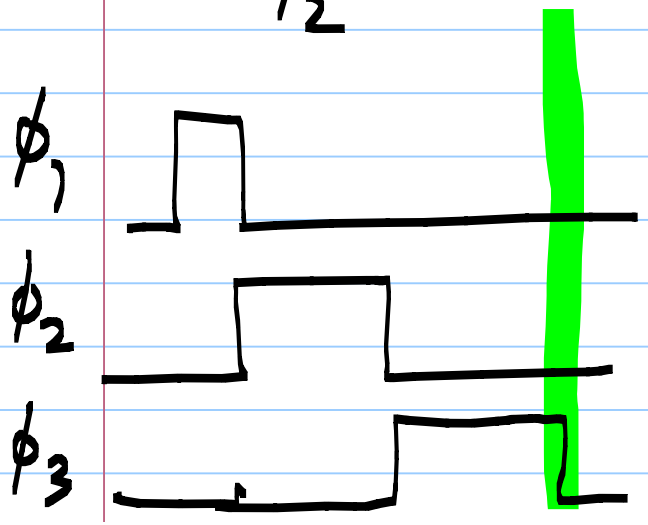
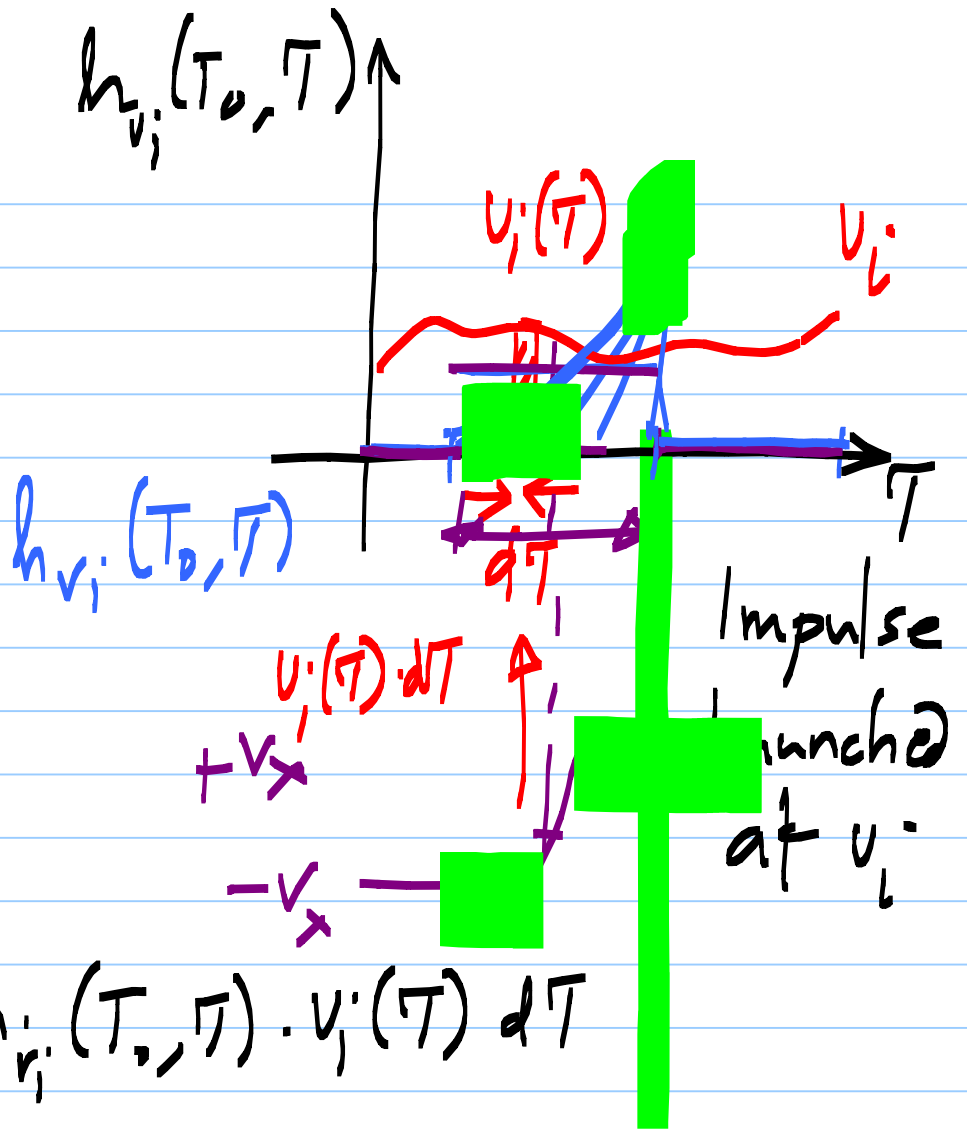
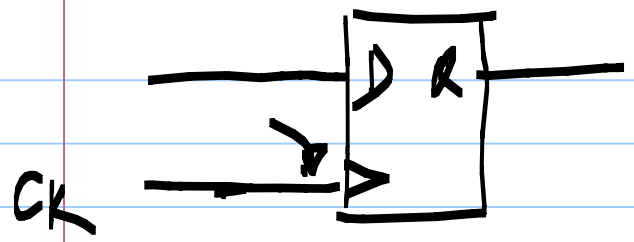
Latch aperture

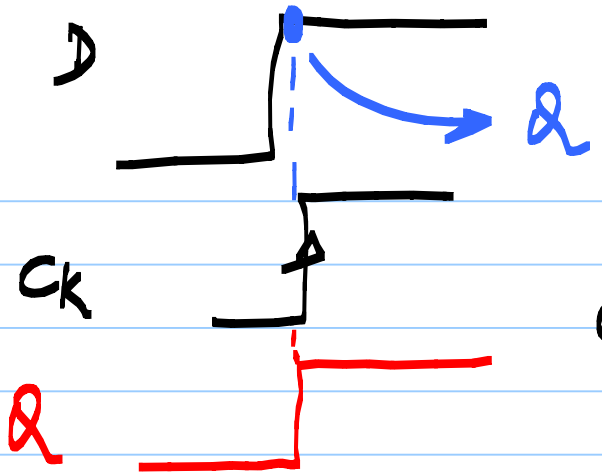




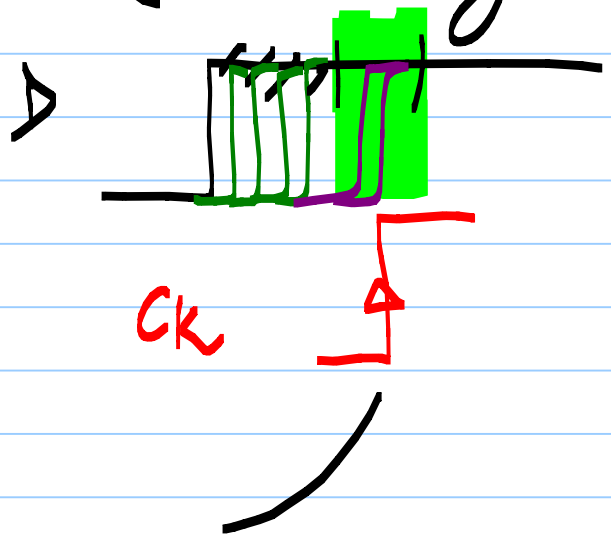


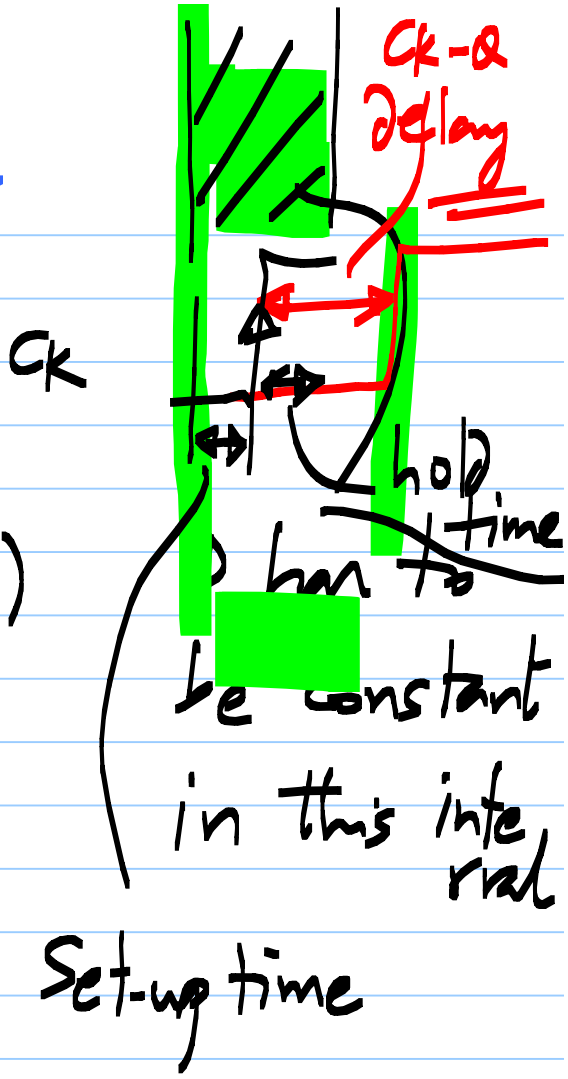
$$\int_0^{T_o} h_{v_i}(T_o, T) \cdot v_i(T)\, dT$$

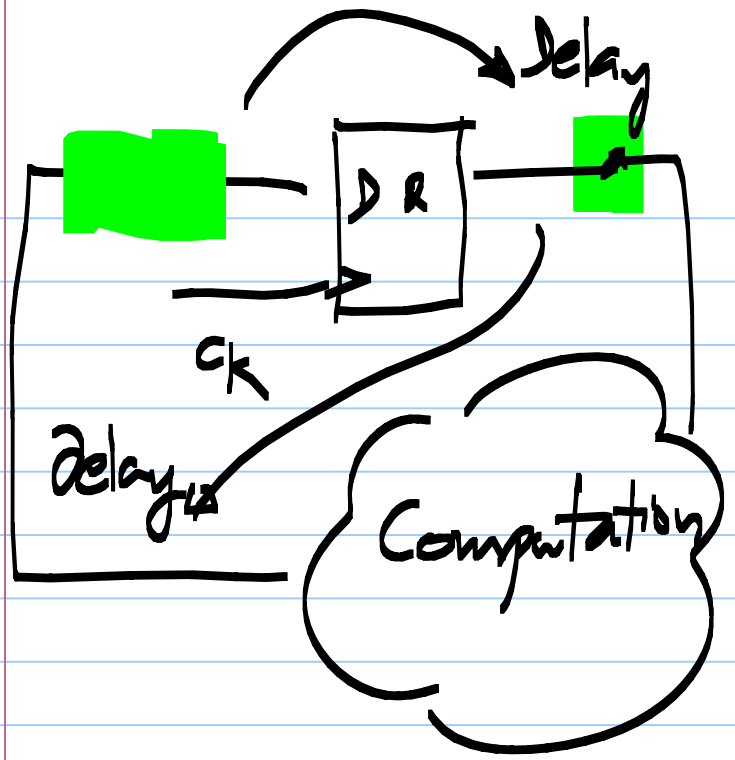




Q = D (@ rising edge of the clock)



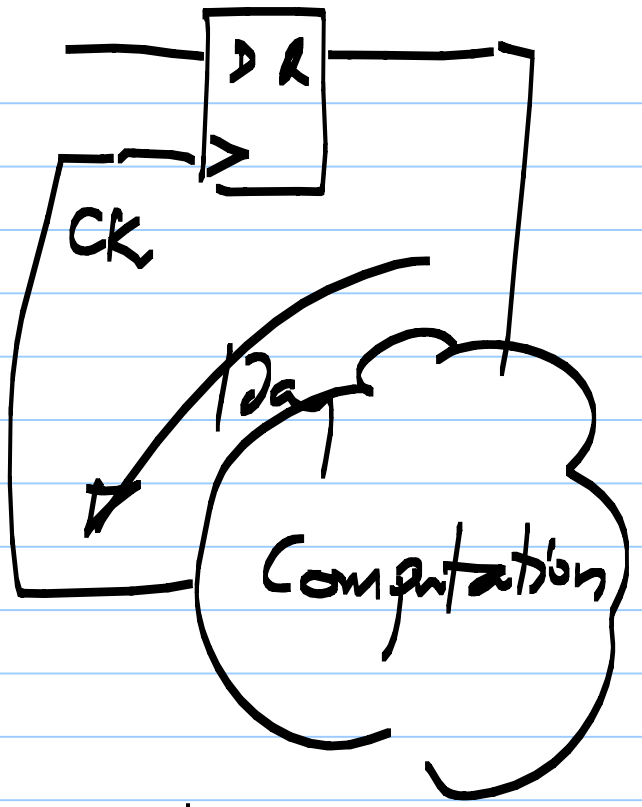




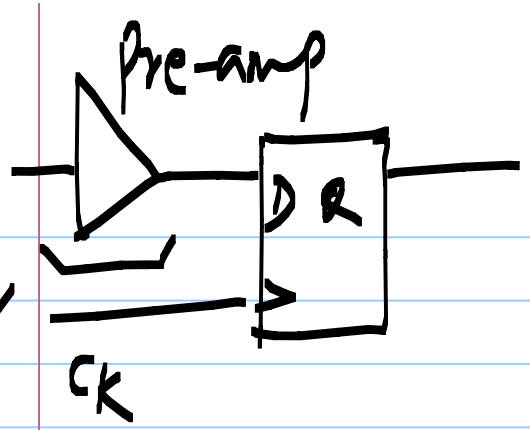
ADCs

Decision feedback equalizers

} delays set a limit on clock rate

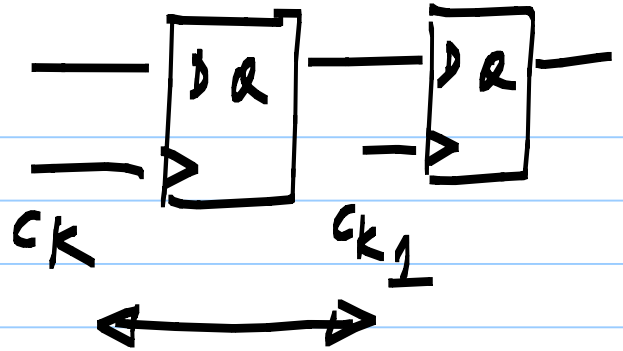


Clock/data recovery



Delay (depends on BW)

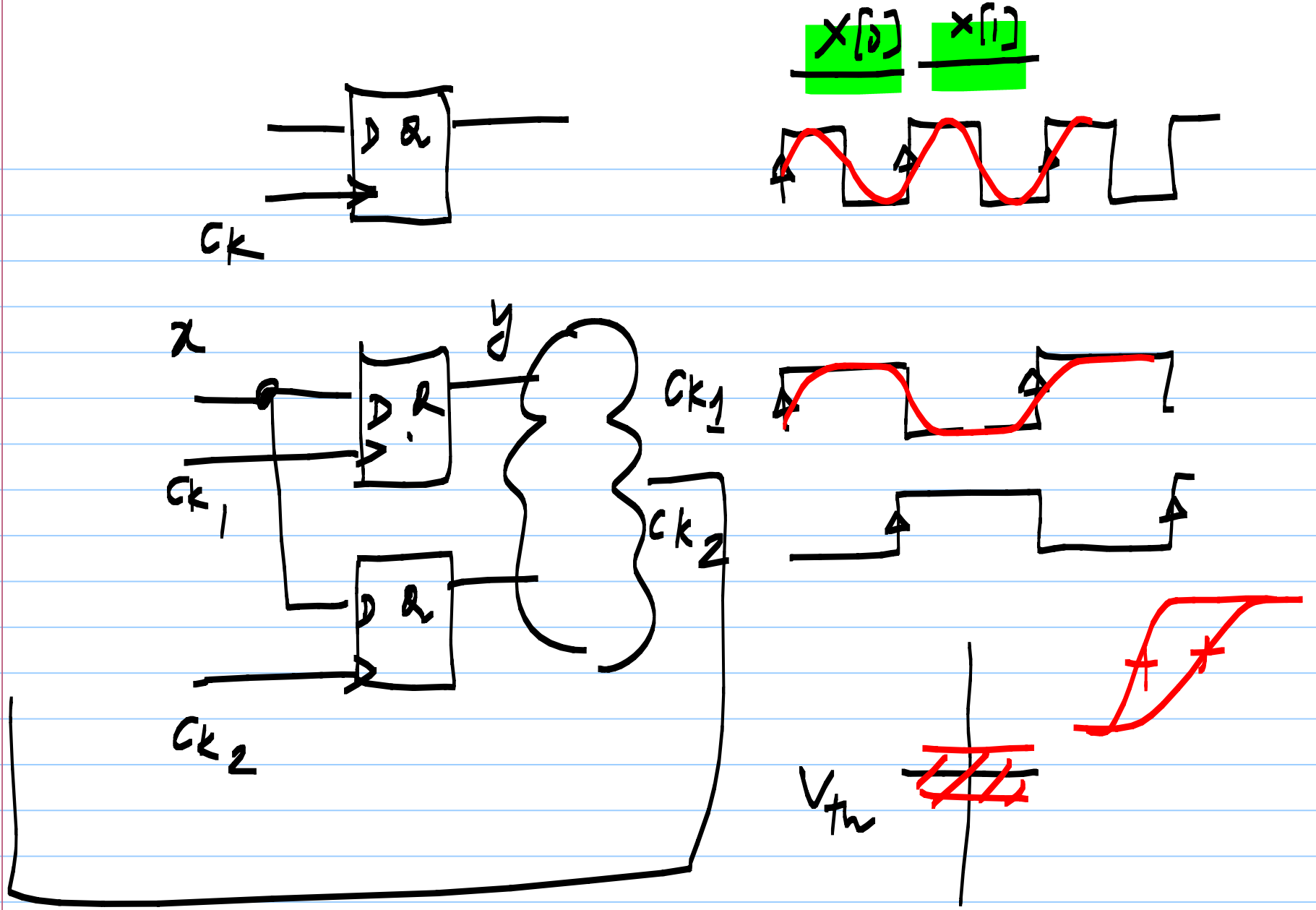
4 exp (4)

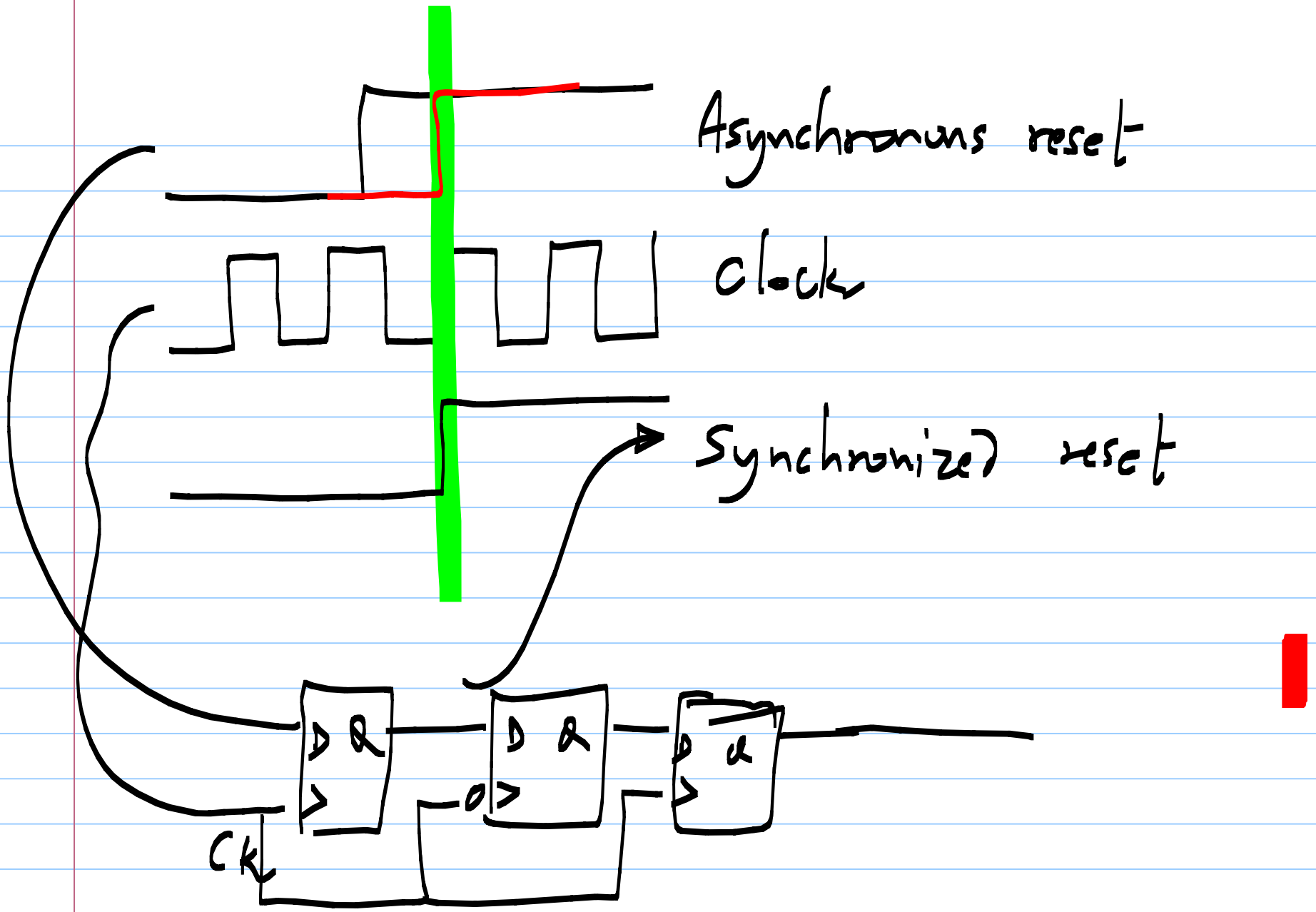


Multiple regeneration stages

Increases the delay

Not an issue if not in feedback


x[0]
x[1]
D
Q
Ck
x
y
Ck1
Ck2
Vth


Asynchronous reset
clock
Synchronized reset
D
Q
D
Q
D
Q
Clk