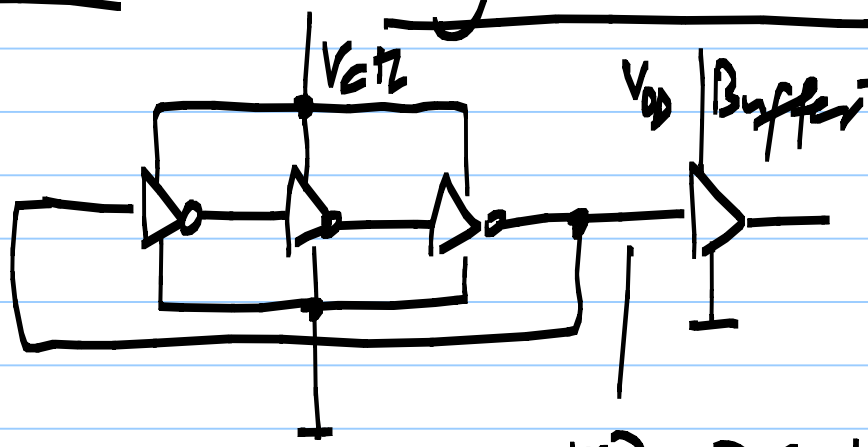
EE6322

Ring oscillators

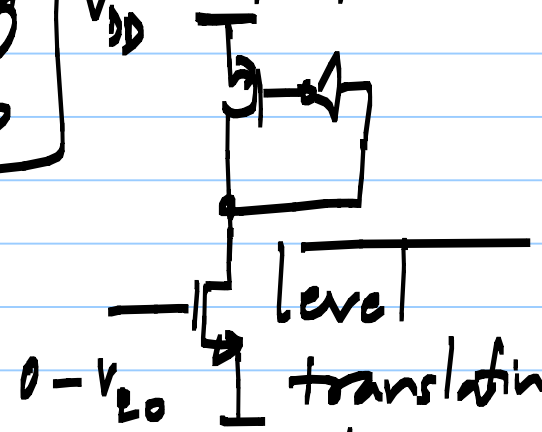


To drive the load w/o affecting the VCO

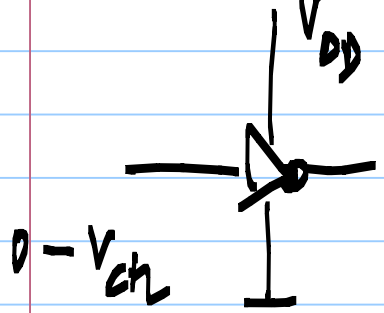
full rail swing

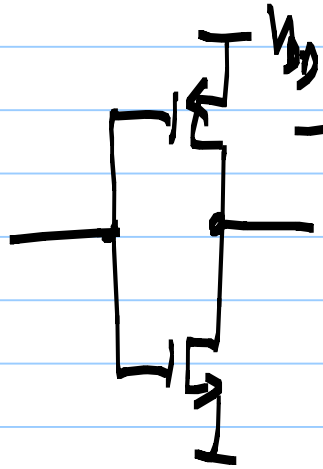
reduced swing

9/3/2018

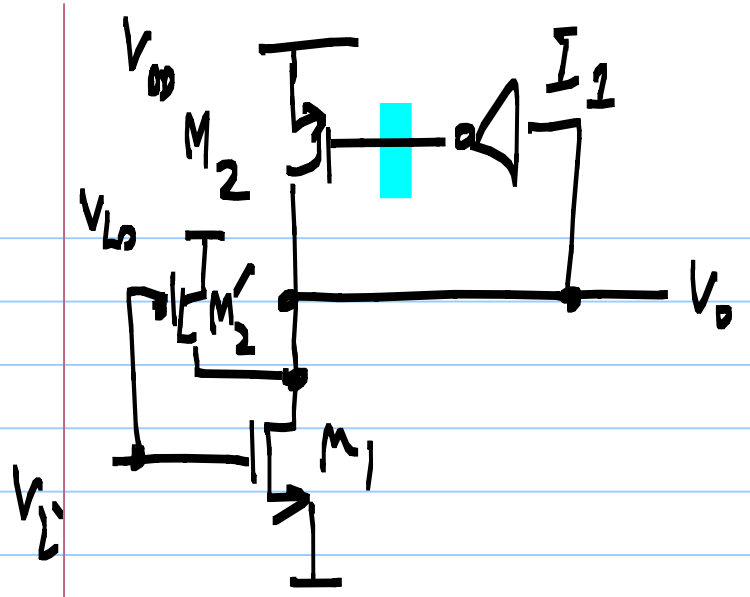


level translating buffer

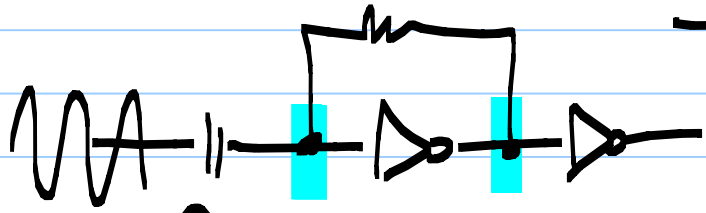


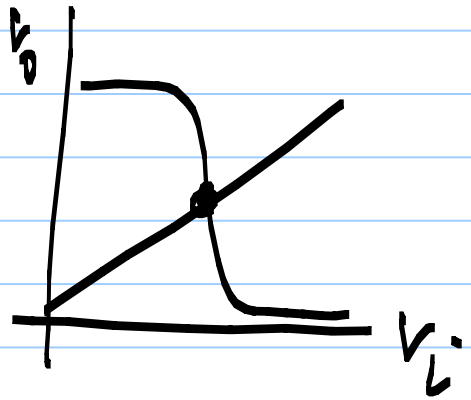


won't turn off if $V_{ctl} < V_{DD} - V_T$



periodic clock: use ac coupling





$V_i = 0$: M_1 off, $V_o = V_{DD}$ → V_o raised by M_2' to trigger I_1

$V_i = V_{LD}$: V_o lowered sufficiently to trigger I_1

M_2 turns off

$V_i = 0$

$$S_\phi(f) = \frac{8}{3}\frac{f_0^2}{(V_{GS} - V_T)I_p f^2}$$

$$\frac{P_d}{(S/N)(BW)} \propto kT$$

Phase noise of (an ideal model of) a ring oscillator

Figure of merit: $10\log_{10}\left[\frac{1}{\mathcal{L}(f)} \cdot \frac{f_0^2}{f^2} \cdot \frac{1}{P_d\,(mW)}\right]$

$$\text{FoM} = \frac{3}{8}\frac{1}{kT}\frac{V_{GS}-V_T}{V_{dd}}10^{-3}$$

10mW, 10GHz, $\mathcal{L}(f)$ @ f = 1MHz offset

V_{dd} = 1.2V ; $V_{GS} - V_T$ = 0.3V

$$S_\phi(f) = \frac{8}{3}\frac{kT}{(V_{GS}-V_T)I_p}\frac{f_0^2}{f^2}$$

$$\underline{FoM = 168\ dB} = 10\log\left(\frac{1}{\mathcal{L}(f)}\left(\frac{f_m}{f}\right)^2 \cdot \frac{1}{P_d(mW)}\right)$$

$$168\,dB = 10\log_{10}\left(\frac{1}{\mathcal{L}(f)} \cdot \underbrace{\left(\frac{10\,GHz}{1\,MHz}\right)^2 \frac{1}{10}}_{80 - 10}\right)$$

$$\mathcal{L}(f) = (-168 + 70)\ dBc/Hz \text{ @ } f = 1MHz$$

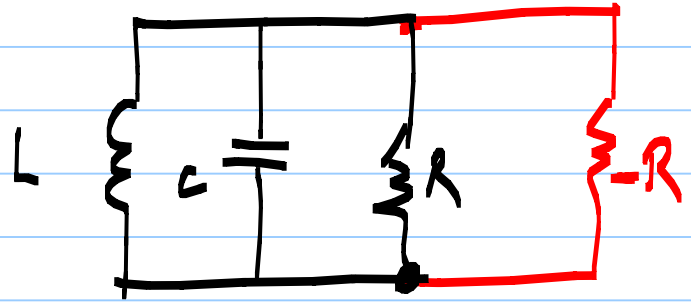
$$-98\ dBc/Hz \text{ @ } f = 1MHz$$

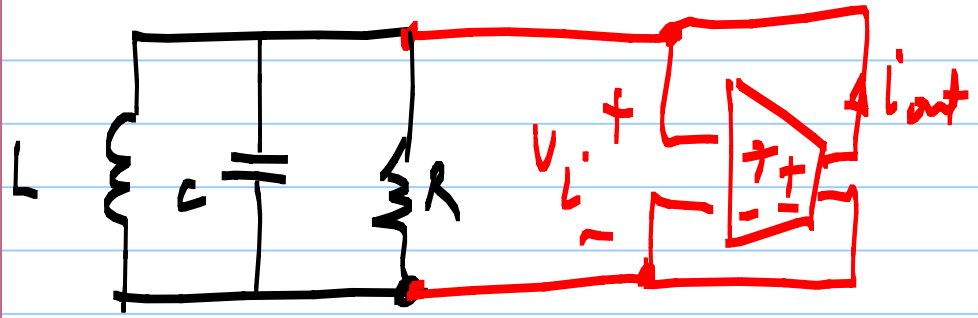
$$\underbrace{\frac{3}{32}}_{\frac{1}{10}} \cdot \frac{1}{kT} \cdot \frac{V_{GS} - V_T}{V_D} \cdot 10^{-3}$$

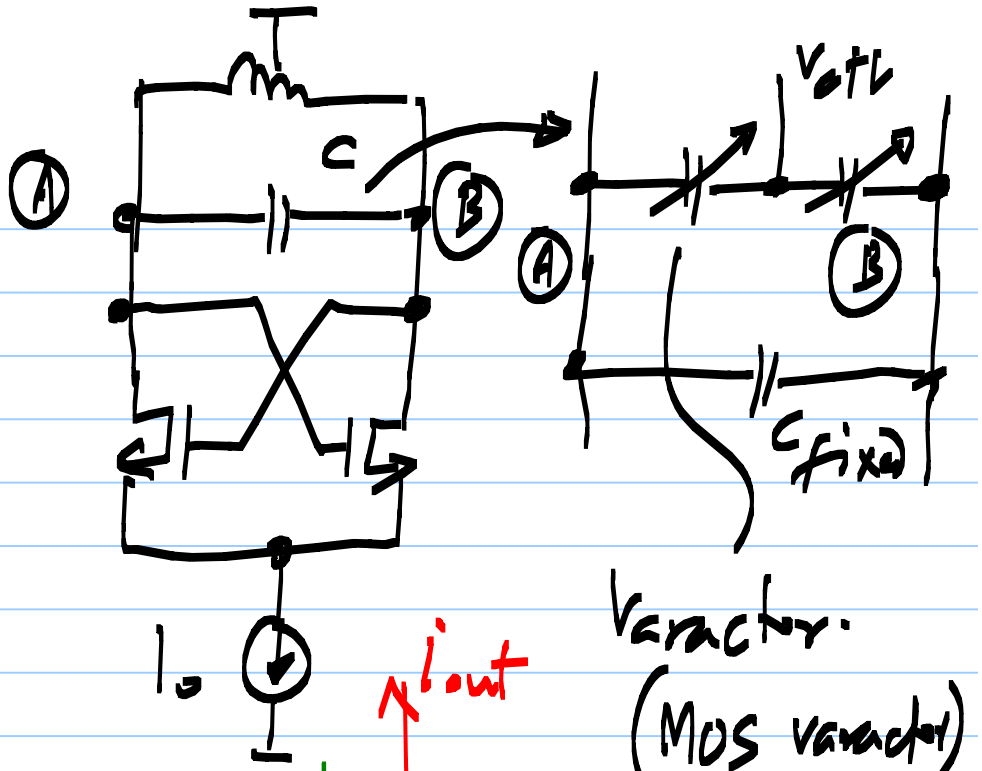
$$\frac{1}{10} \quad \frac{1}{4 \cdot 10^{-21}} \quad \frac{1}{4} \cdot 10$$

$$\mathcal{L}(f) \propto \frac{1}{\rho_d} \cdot \frac{f_0^2}{f^2} \Bigg] \text{FoM} =$$

LC oscillators:

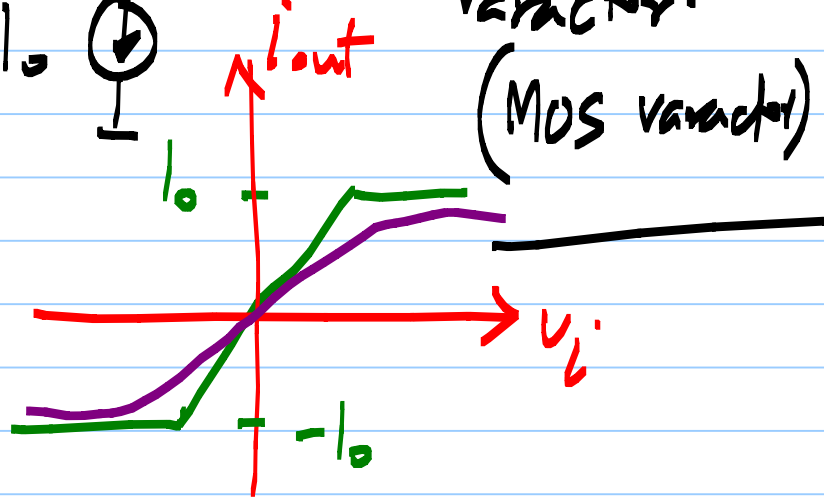


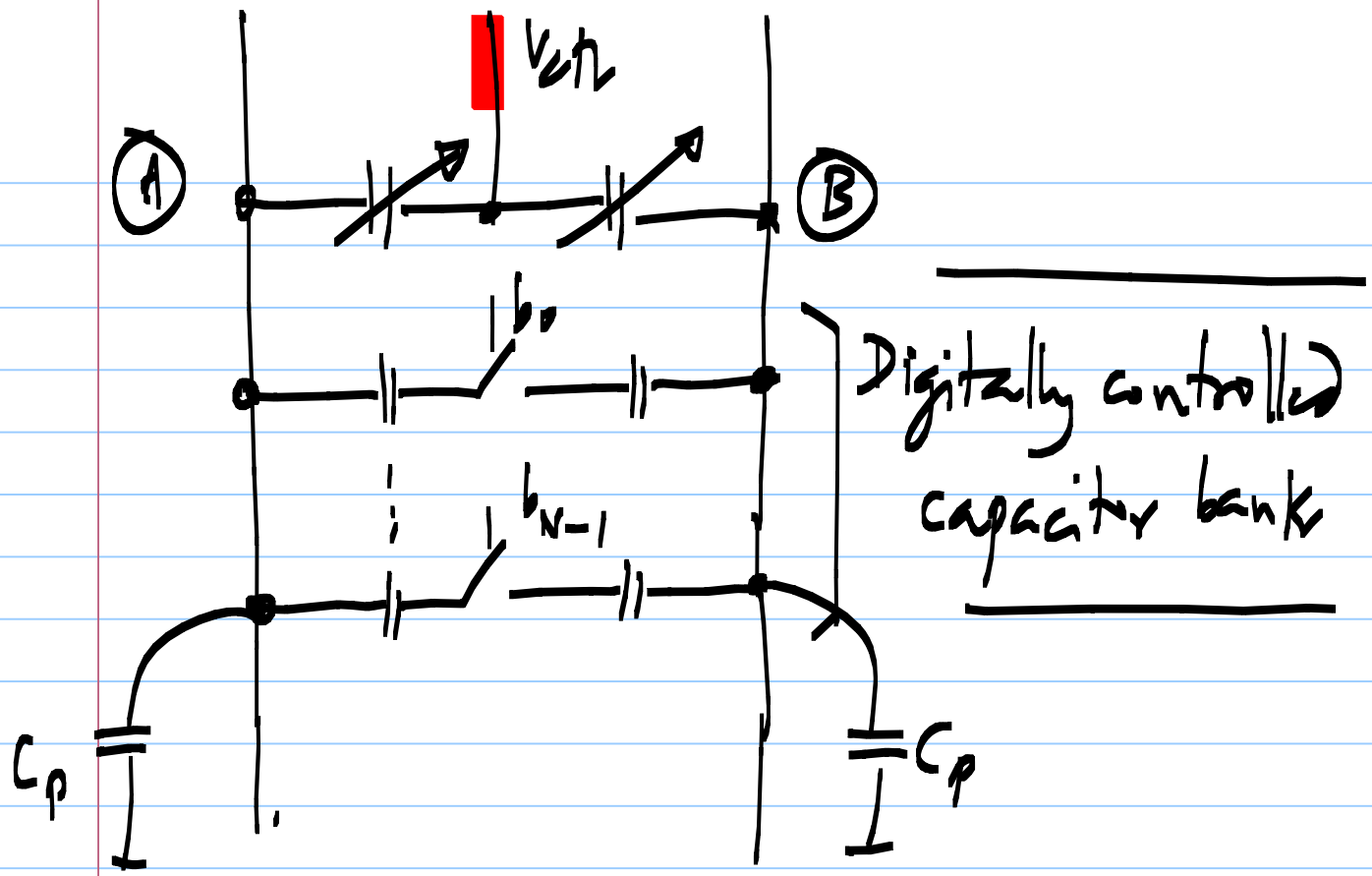




Varactor:

(MOS varactor)




V_{ctrl}
A
B
b_0
b_{N-1}
Digitally controlled capacitor bank
C_p
C_p