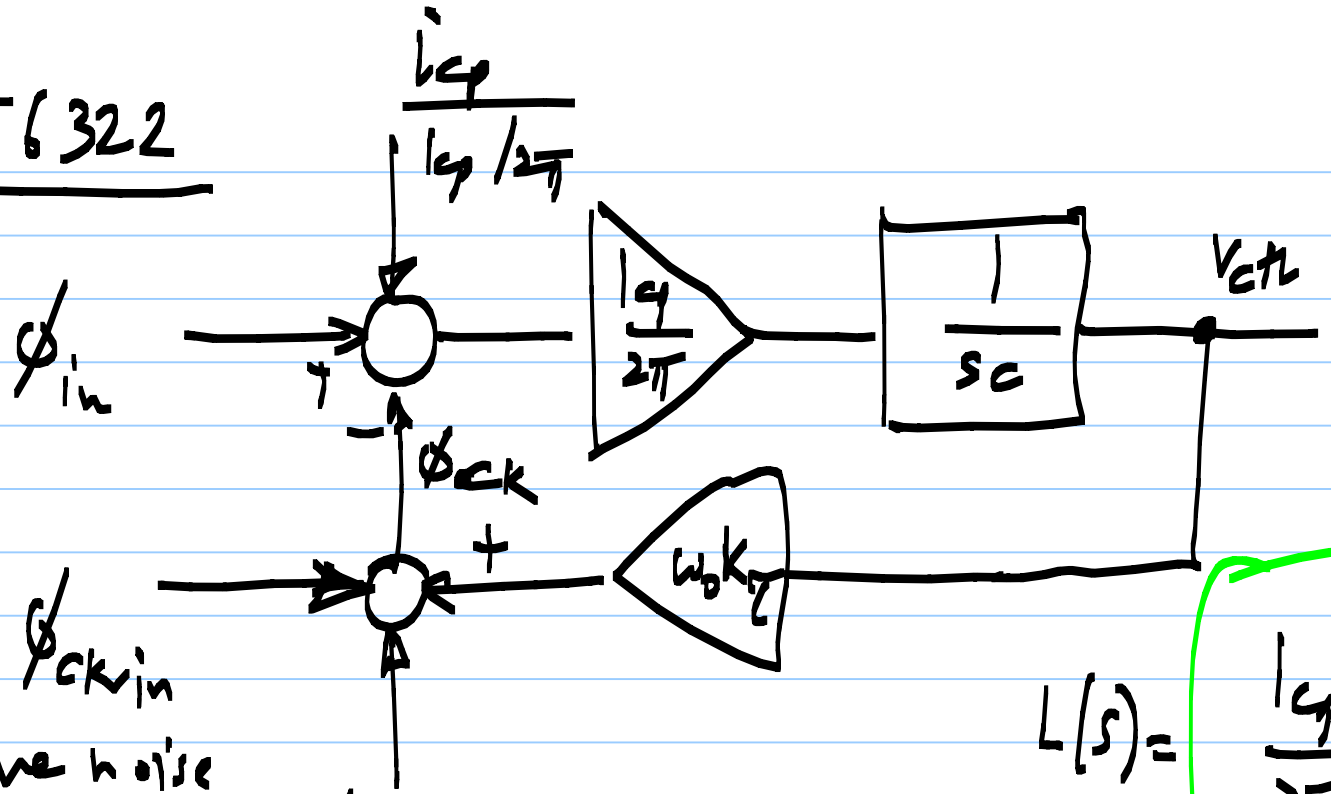
EE 6322

5/3/2018



phase noise of the input clock

(delay line)

$$L(s) = \frac{I_{cp}}{2\pi} \cdot \frac{w_0 K_\tau}{sC}$$

$$w_{u,\,loop} = \frac{I_{cp}}{2\pi} \cdot \frac{w_0 K_\tau}{C}$$

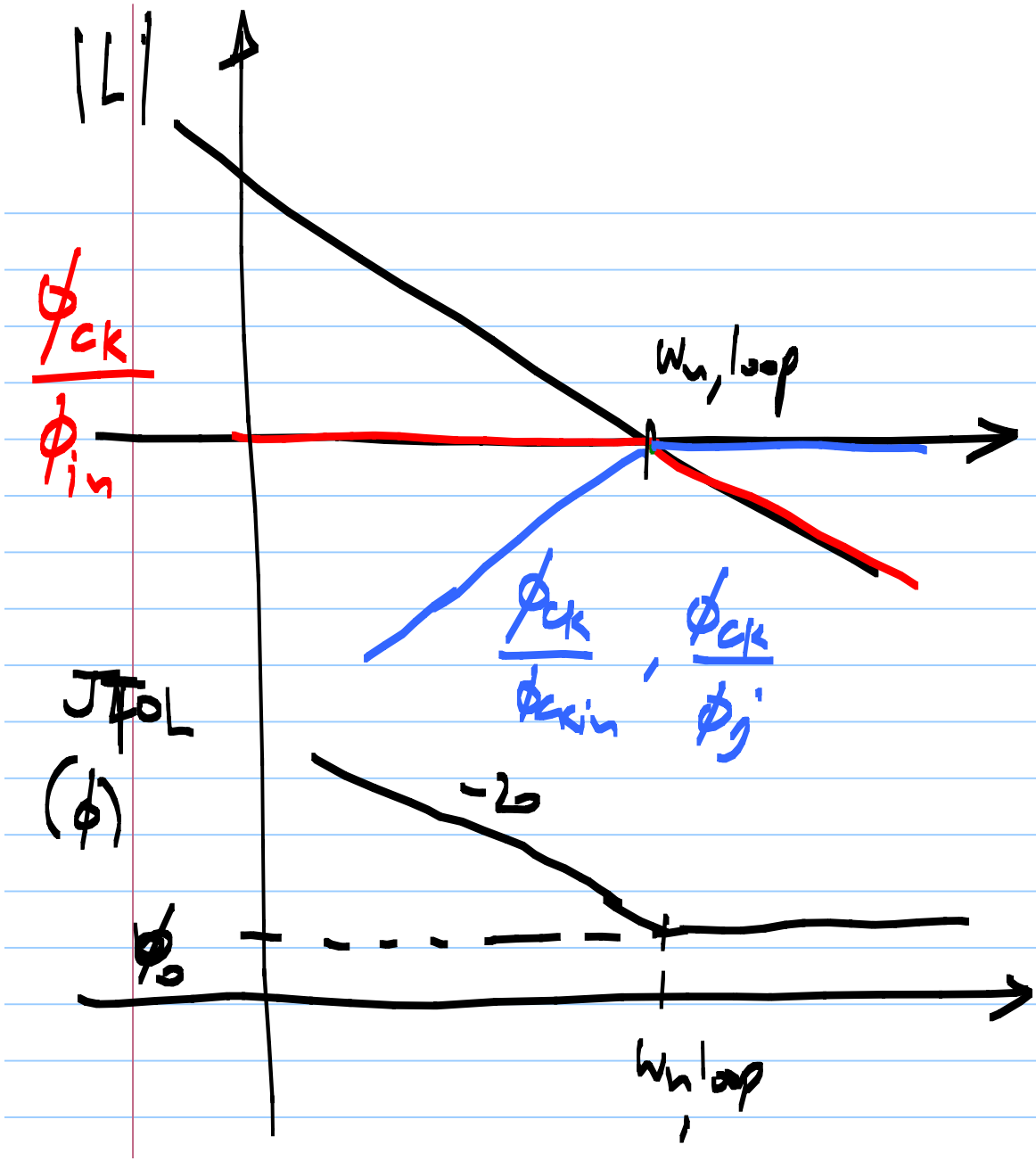
$$\frac{\phi_{clk}}{\phi_{in}} = \frac{1}{1 + s/\omega_{n,loop}} = \frac{\phi_{clk}}{i_{cp}/(I_{cp}/2\pi)}$$

$$\frac{\phi_{clk}}{\phi_{clkin}} = \frac{\phi_{clk}}{\phi_j} = \frac{s/\omega_{n,loop}}{1 + s/\omega_{n,loop}}$$

JTOL: $|\phi_{in} - \phi_{clk}| < \phi_0$

$$\left|\phi_{in}\left(1 - \frac{1}{1+s/\omega_{n,loop}}\right)\right| < \phi_0$$

$$|\phi_{in}| < \left|\phi_0\left(1 + \frac{\omega_{n,loop}}{s}\right)\right|$$



Easier to satisfy stability constraint: (first order, unconditionally stable)

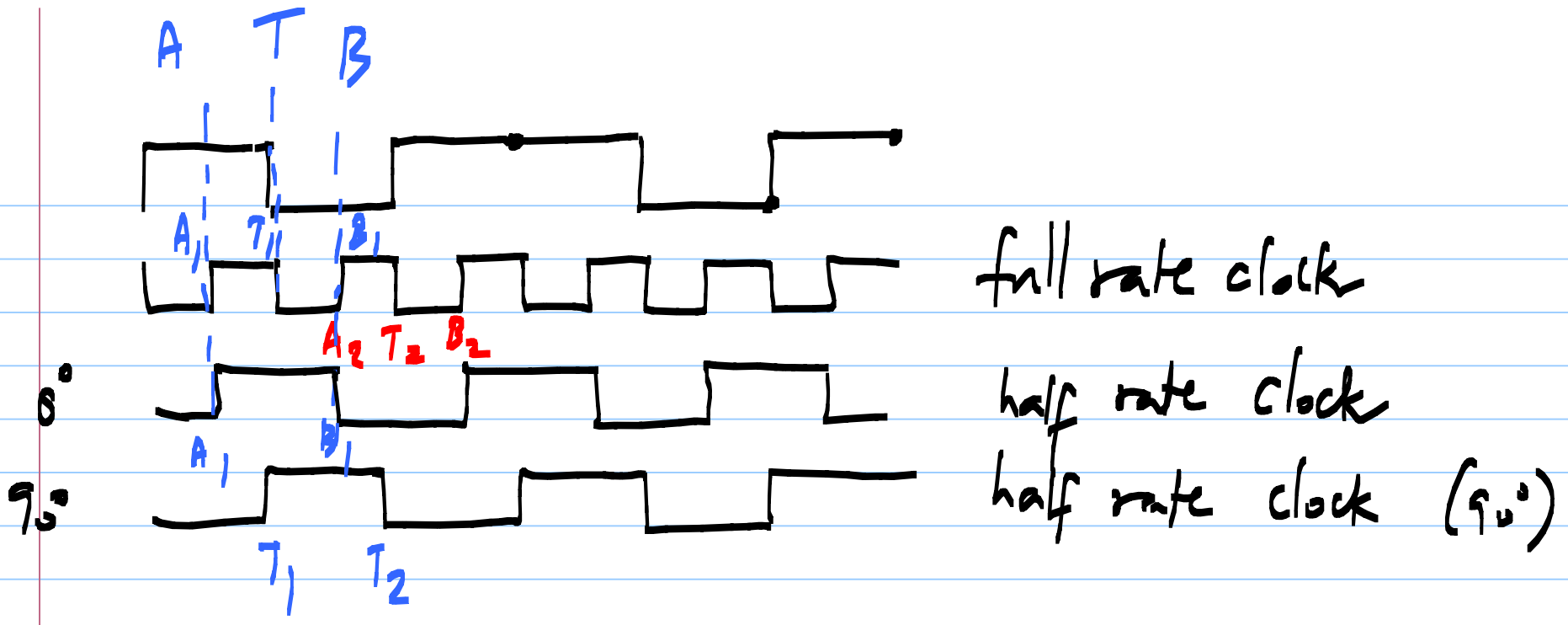
VCO noise: $1/f^2$

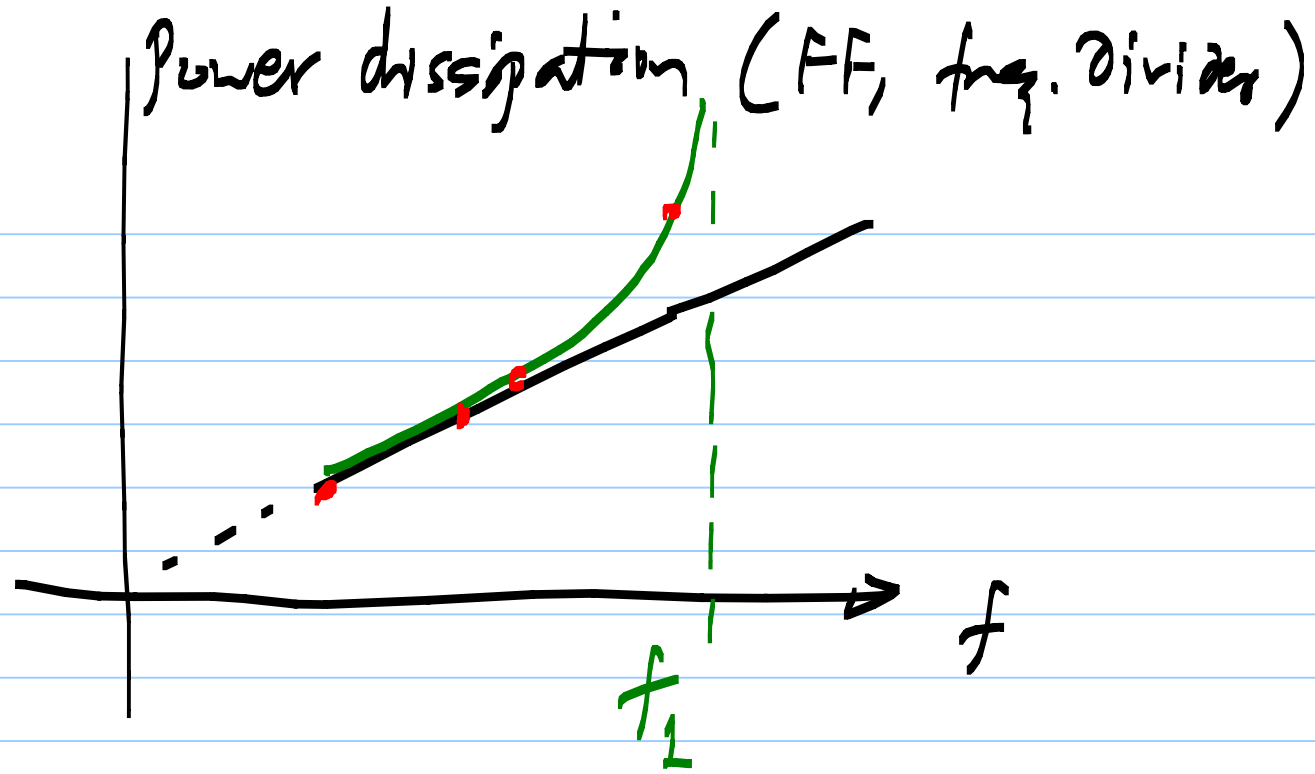
($1/f^3$ @ low freq.)

Delay line noise:

Constant (white)

($1/f$ @ low freq.)

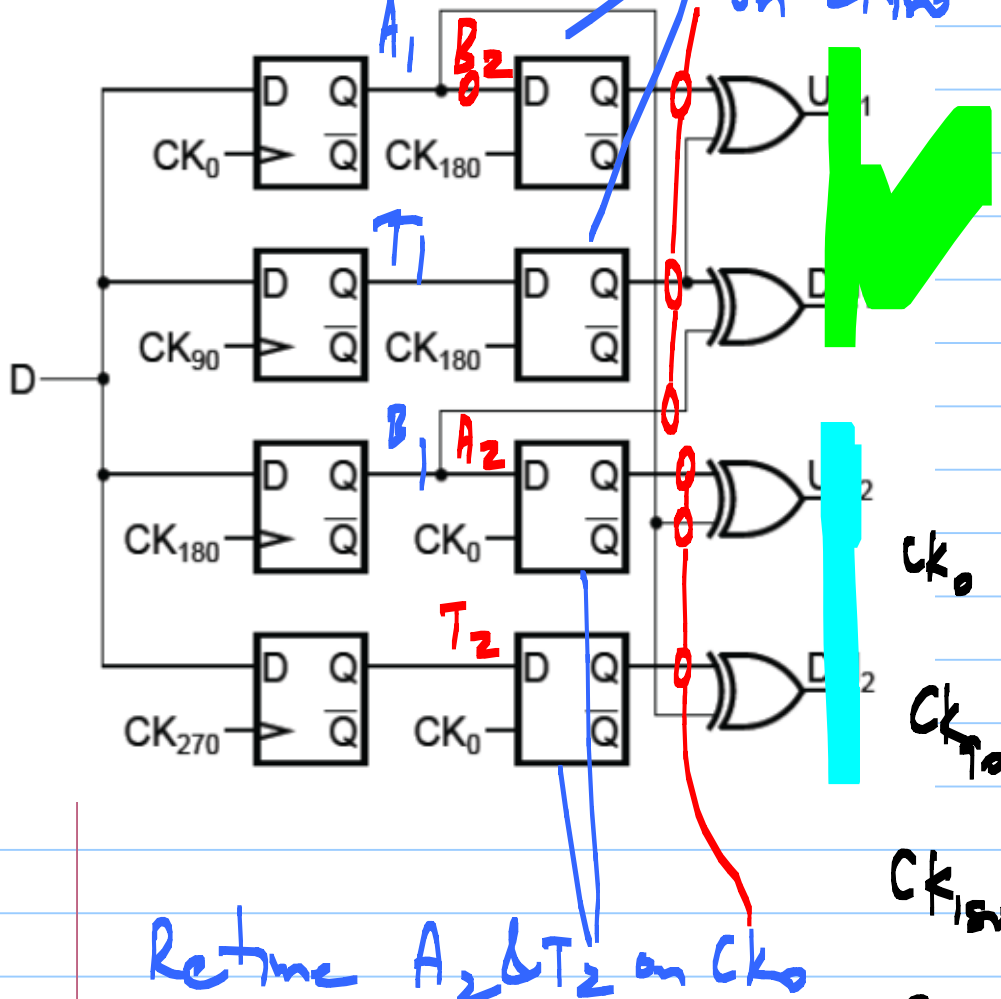

A
T
B
A1
T1
B1
A2 T2 B2
0°
A1
B1
90°
T1
T2
full rate clock
half rate clock
half rate clock (90°)

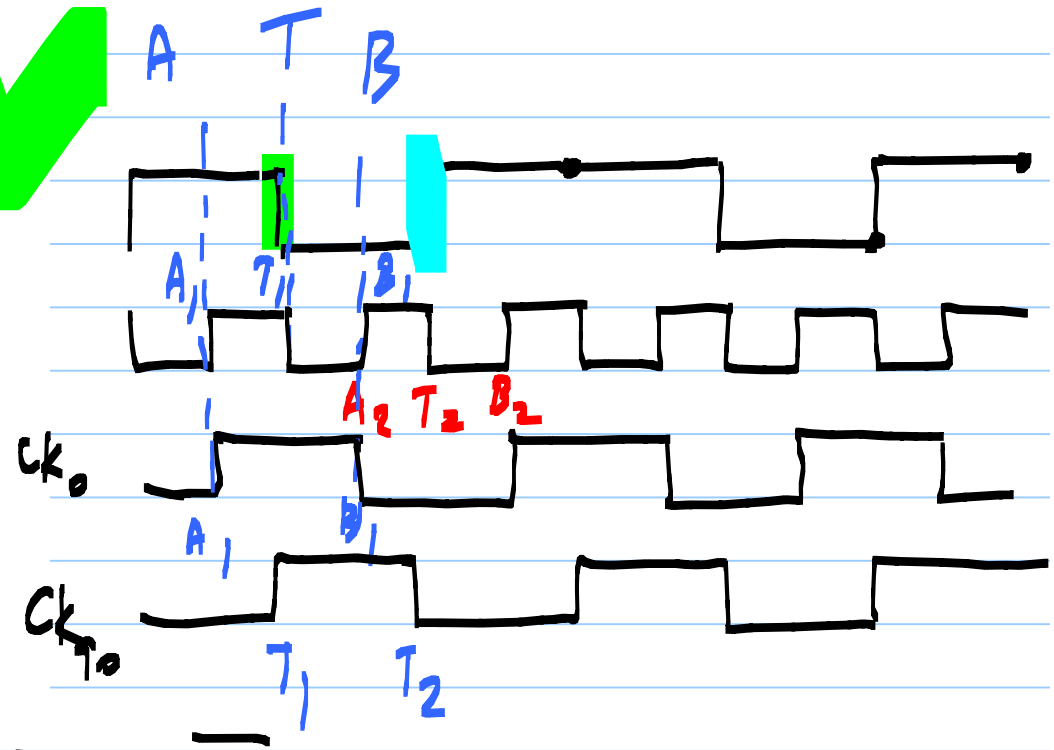

Power dissipation (FF, freq. divider)
f
f_1

CK_{90} Lags CK_0 by 90° Retimes A_1 & T_1 on CK_{180}

$UP = A \oplus T$

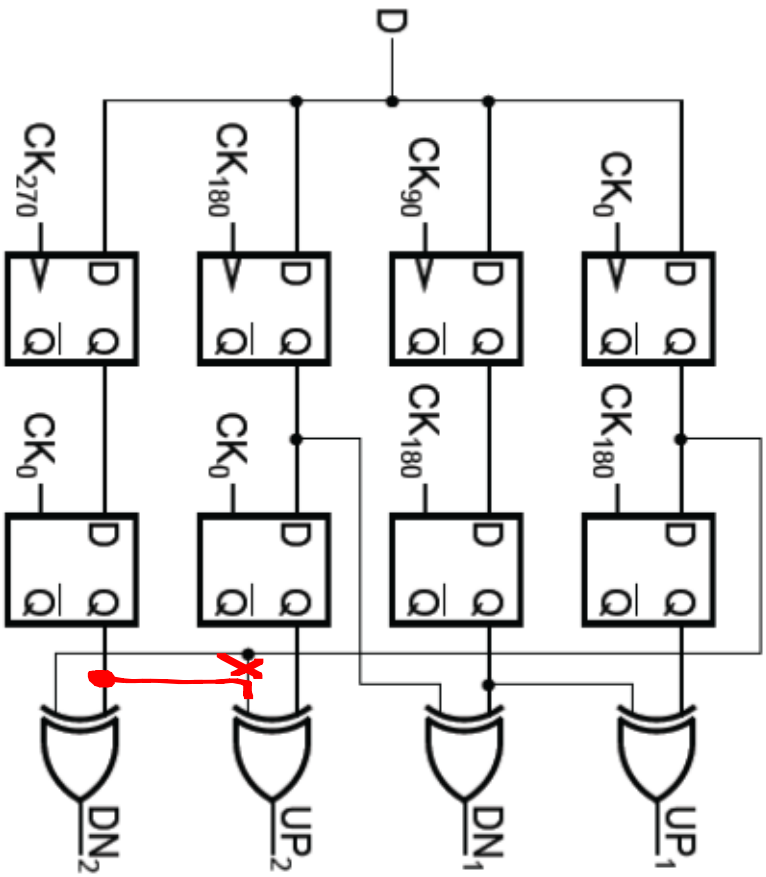
$DN = B \oplus T$





$CK_{180} = \overline{CK_0}$

$CK_{270} = \overline{CK_{90}}$


D
CK270
CK180
CK90
CK0
D
Q
CK0
CK0
CK180
CK180
DN2
UP2
DN1
UP1