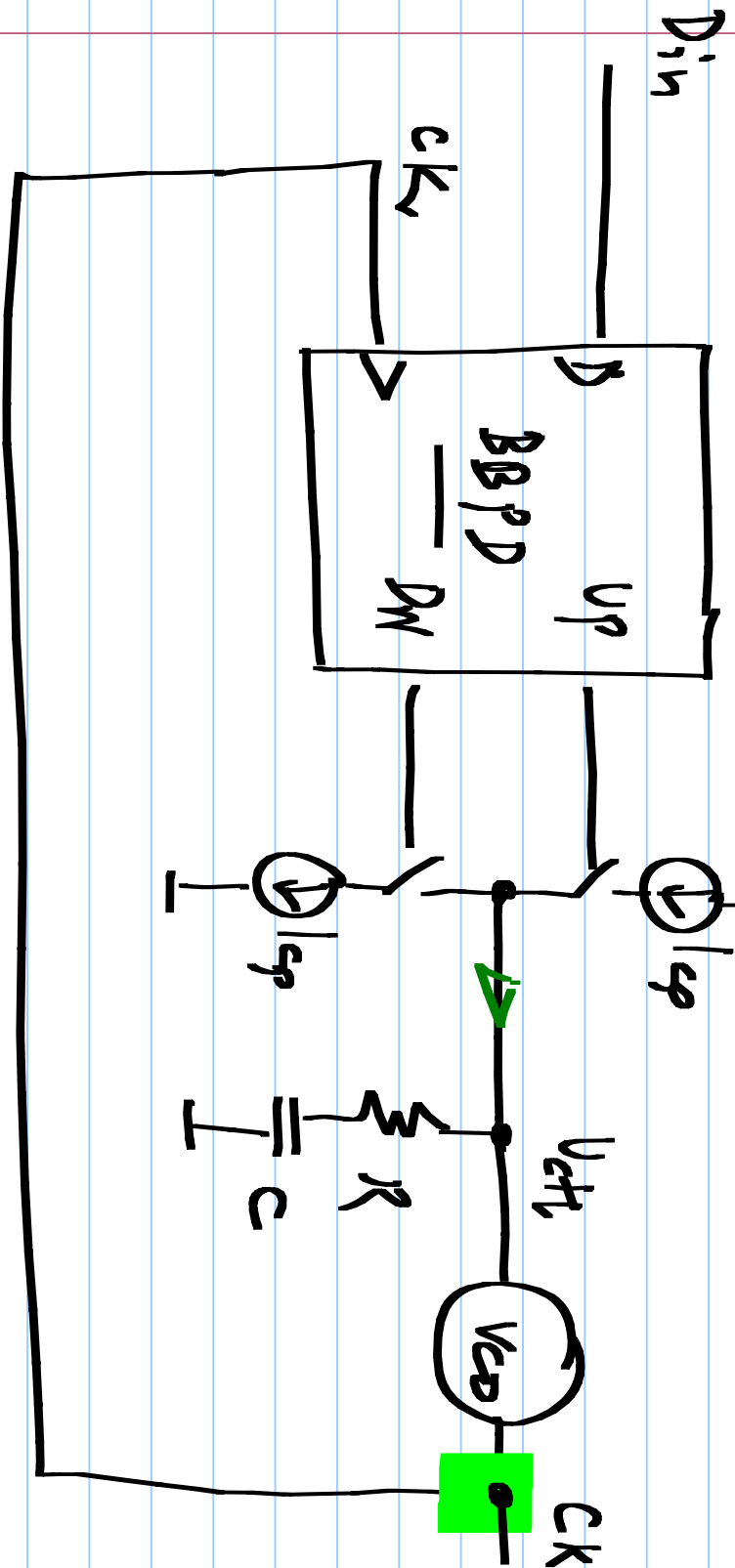
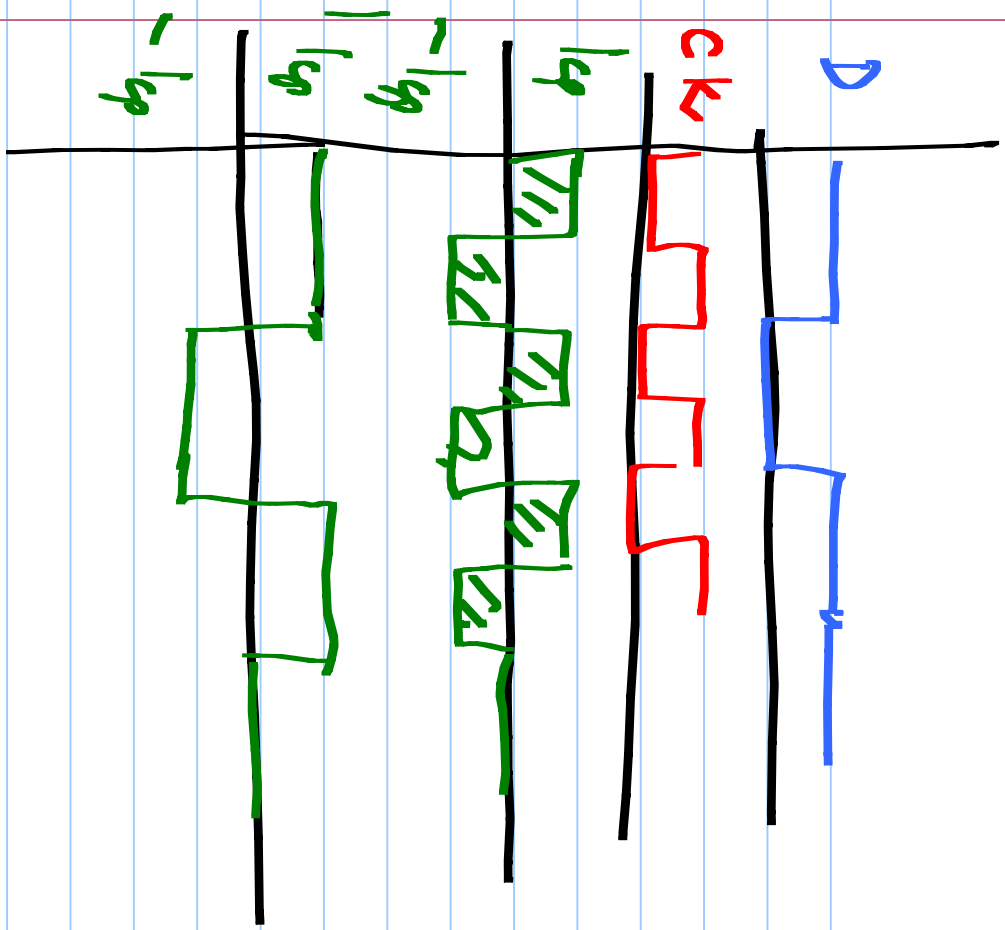


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Bang-Bang jitter

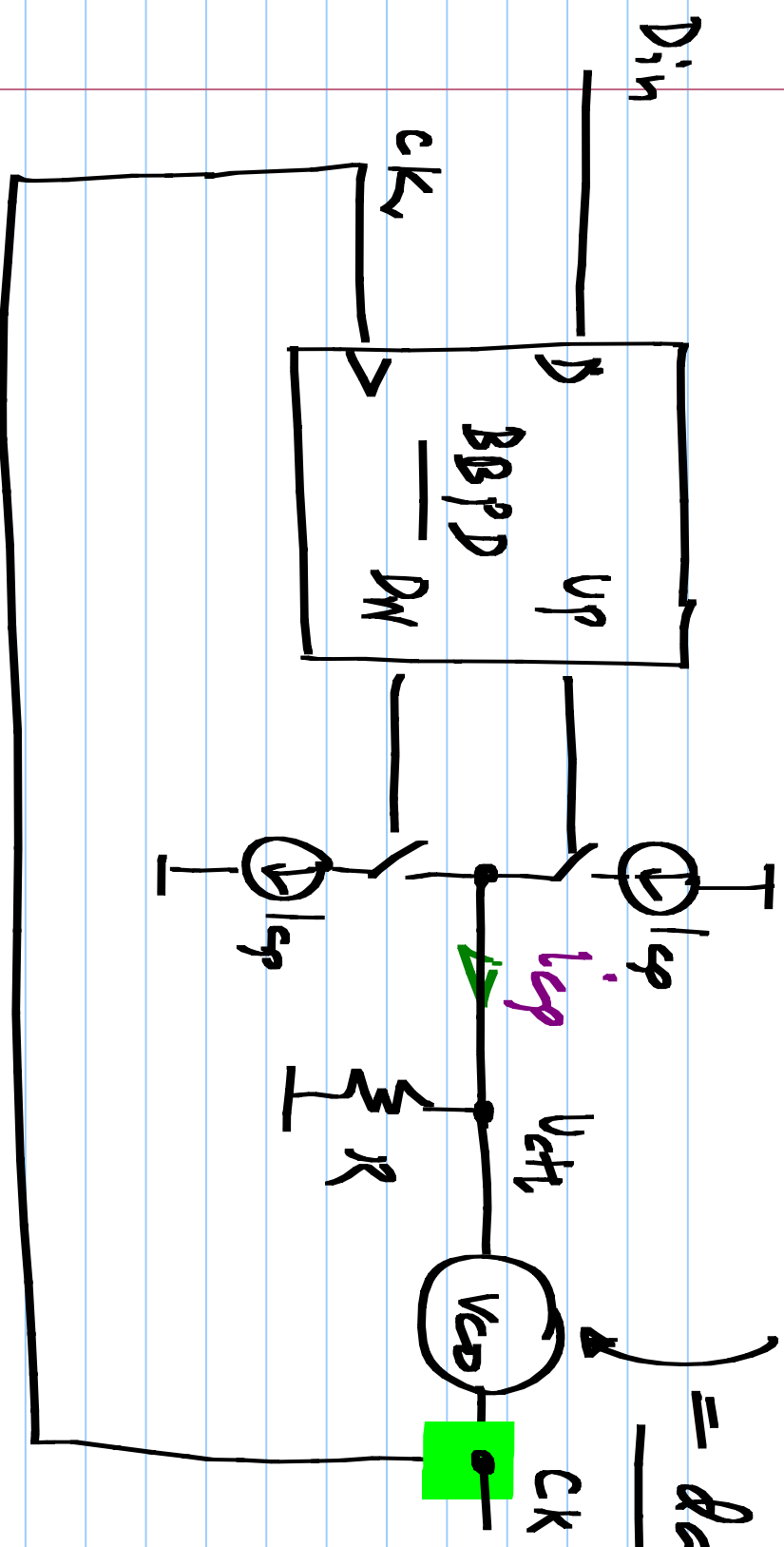
23/2/2018





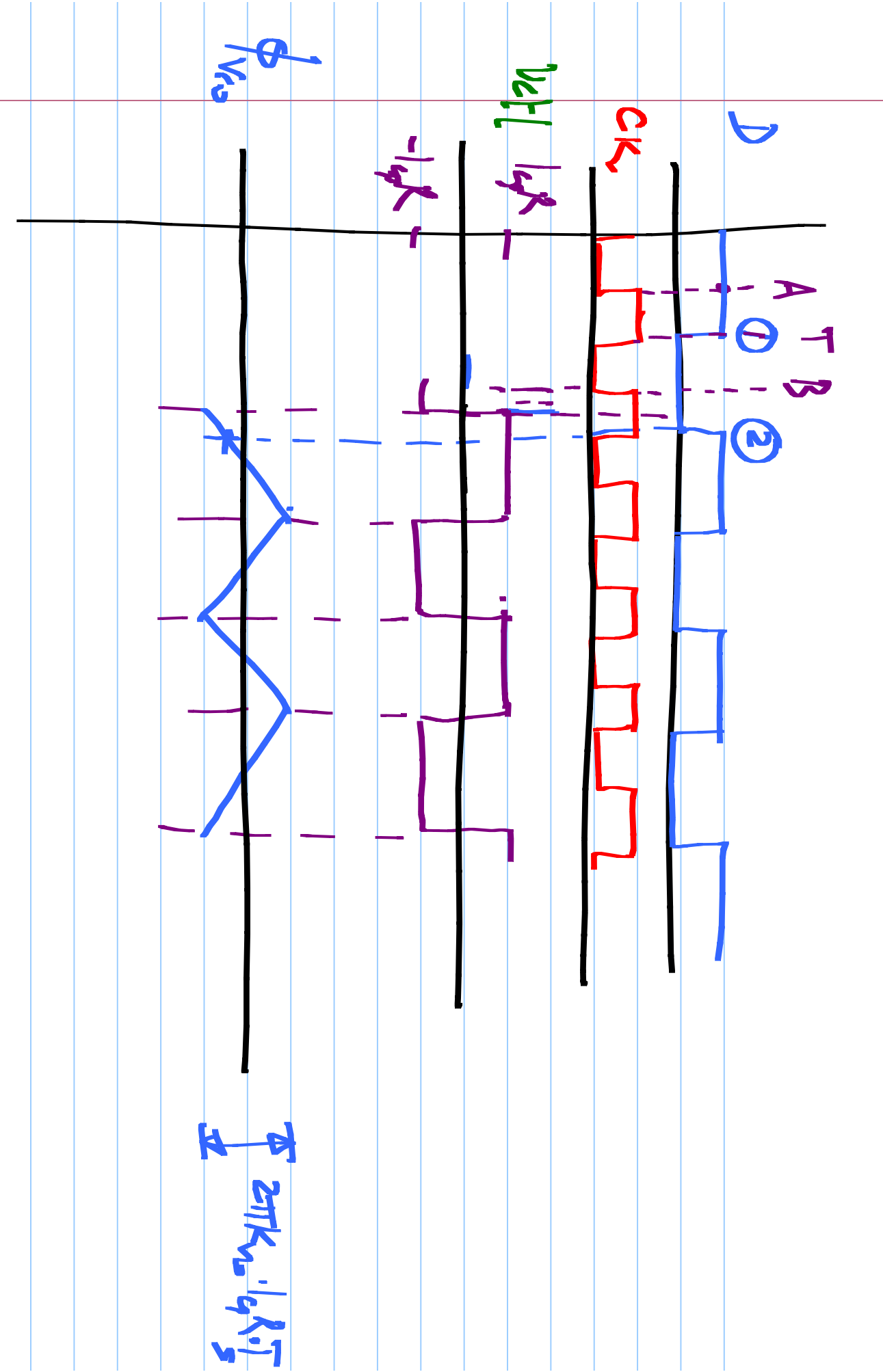
lim PD output, zero average @ every transition

BB PD output. Full with 0% (+ve or -ve) @ every transition

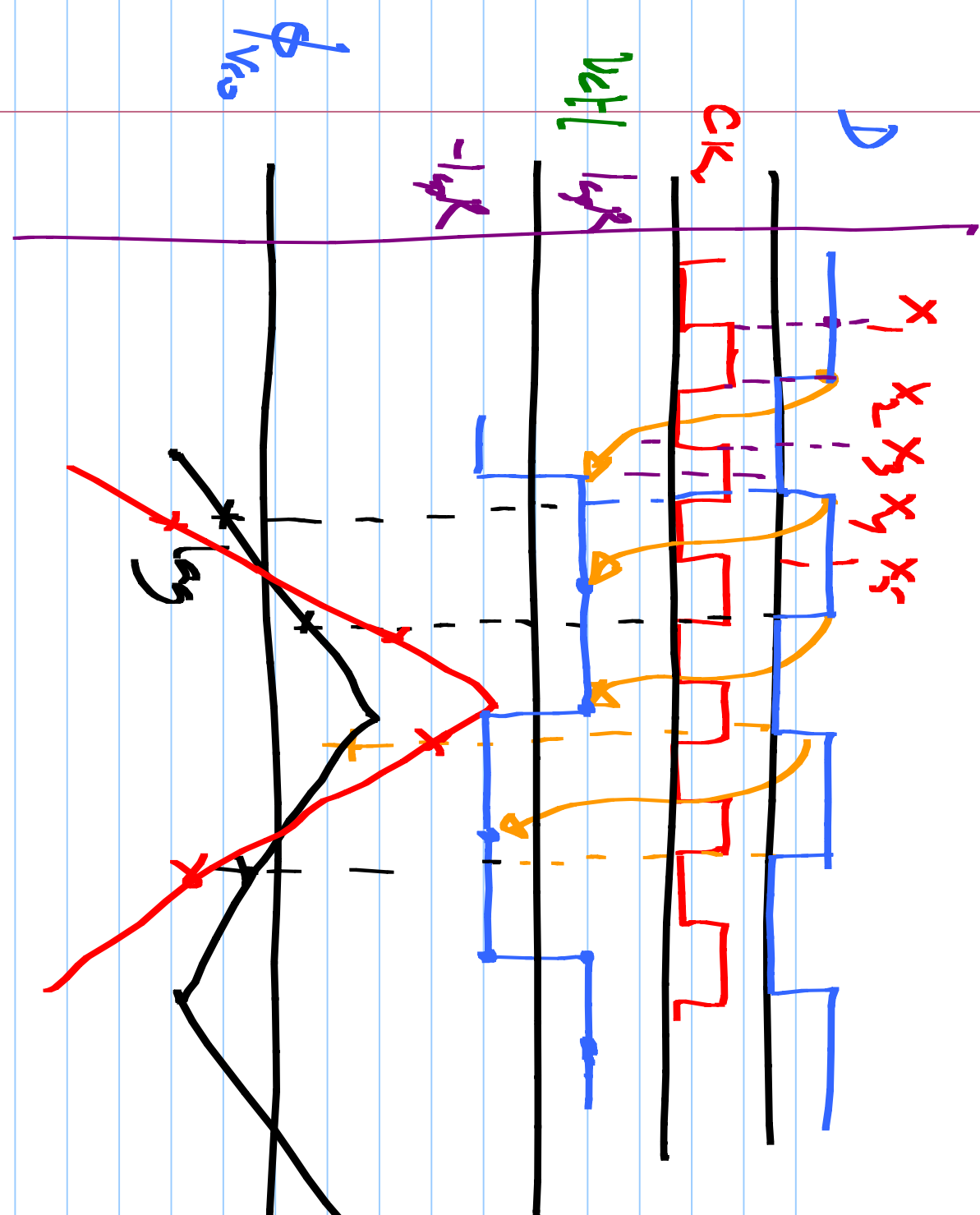


free running freq.

= data rate

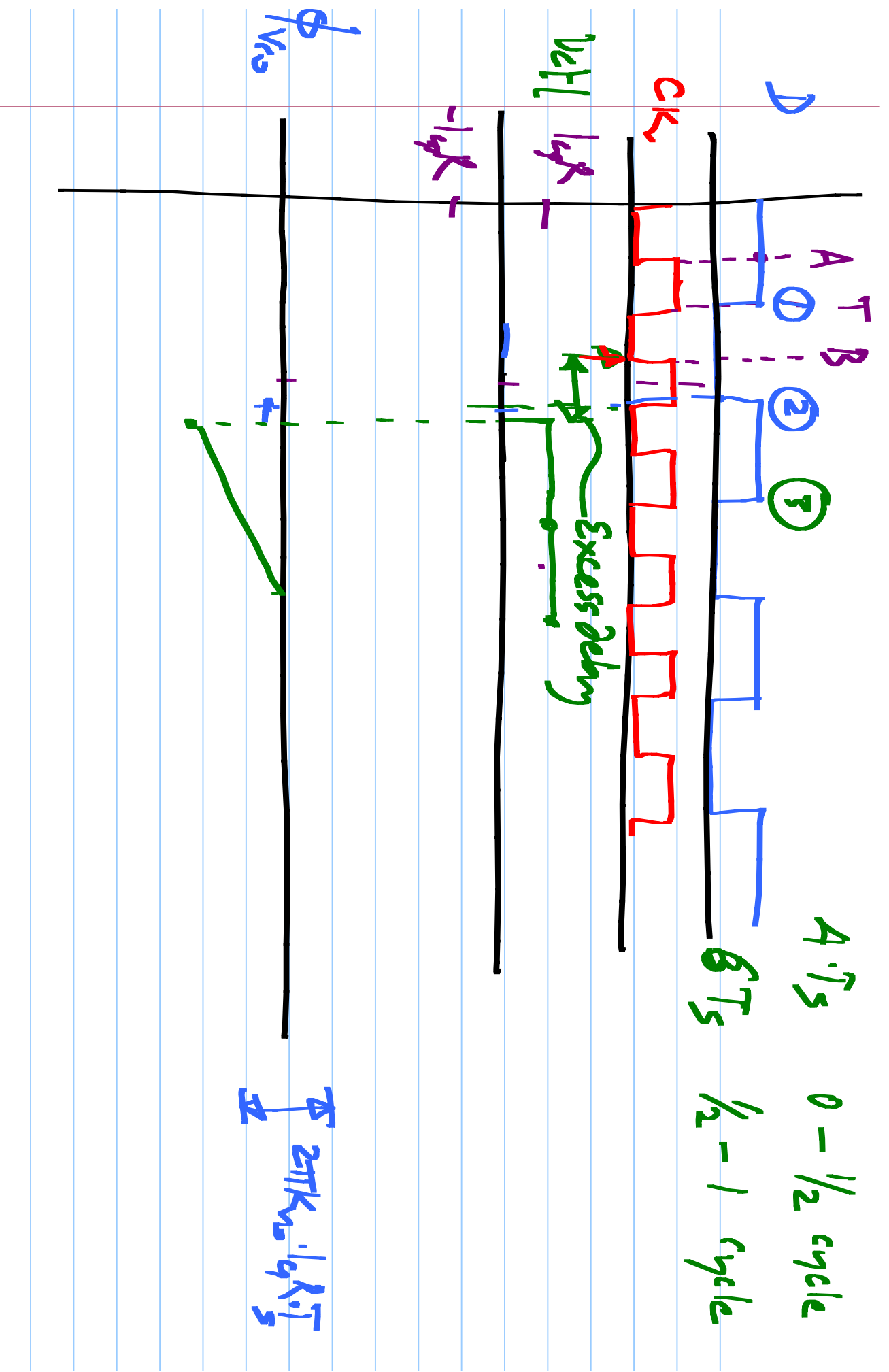


2VP, 2VN :-



$27\text{ns}$

$\Delta$



# Bang-bang CDR: (alternating input)

\* (UP-DN) is a periodic signal

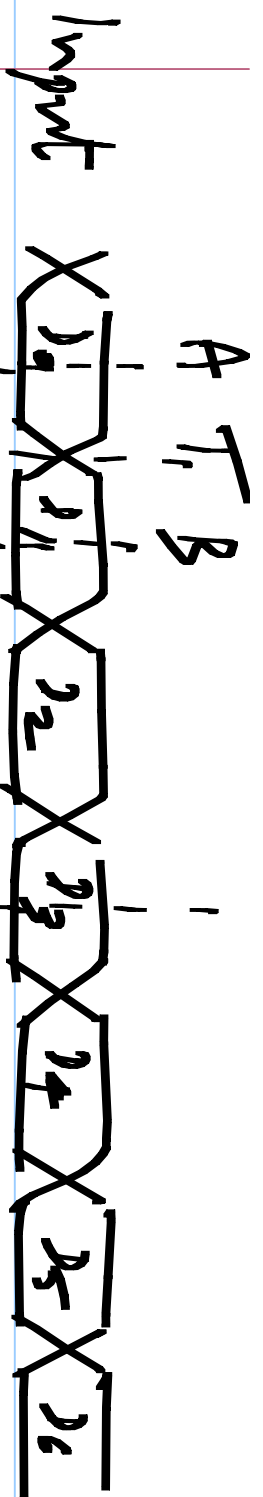
\* +1 for  $N$  cycles & -1 for  $N$  cycles

$N \geq 2$   
CDR BW  $\propto \log R_{k0}$ : have to reduce this to reduce BB jitter  $\Rightarrow$  worsen  $J_{N1}$

\*  $N$  increases  $\Rightarrow$  delay increases  $V_{OPN}$  contribution

pp. phase jitter:  $2\pi R_{k0} \cdot \log R_{k0} \cdot N \cdot T_s$

\* Deserialization causes delay & increases  $N$ .  
 $\Rightarrow$  BB jitter increases



Description

by 2x

