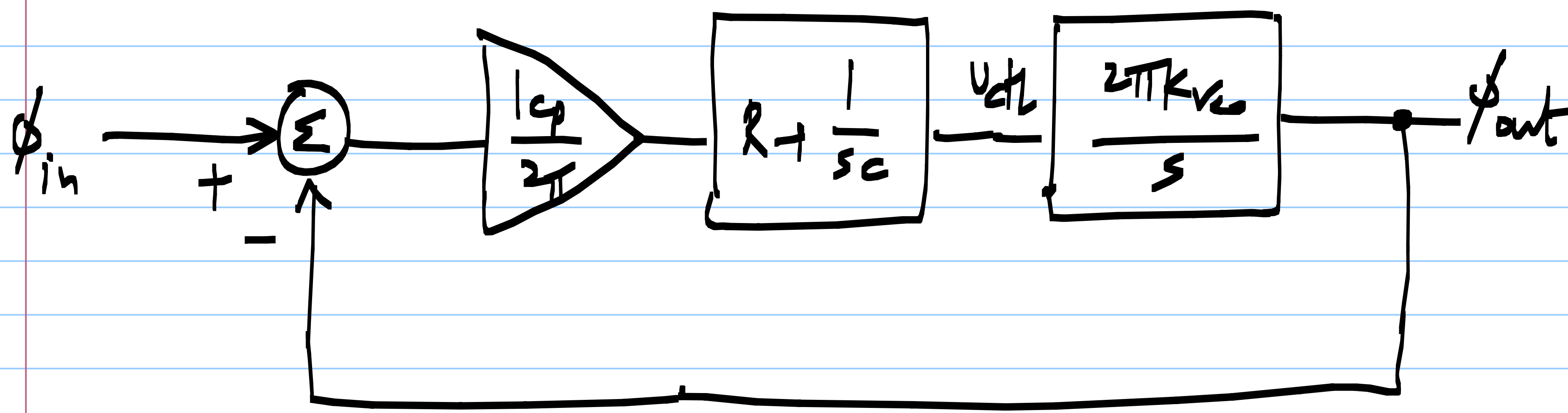
EE 6322 7/2/2018

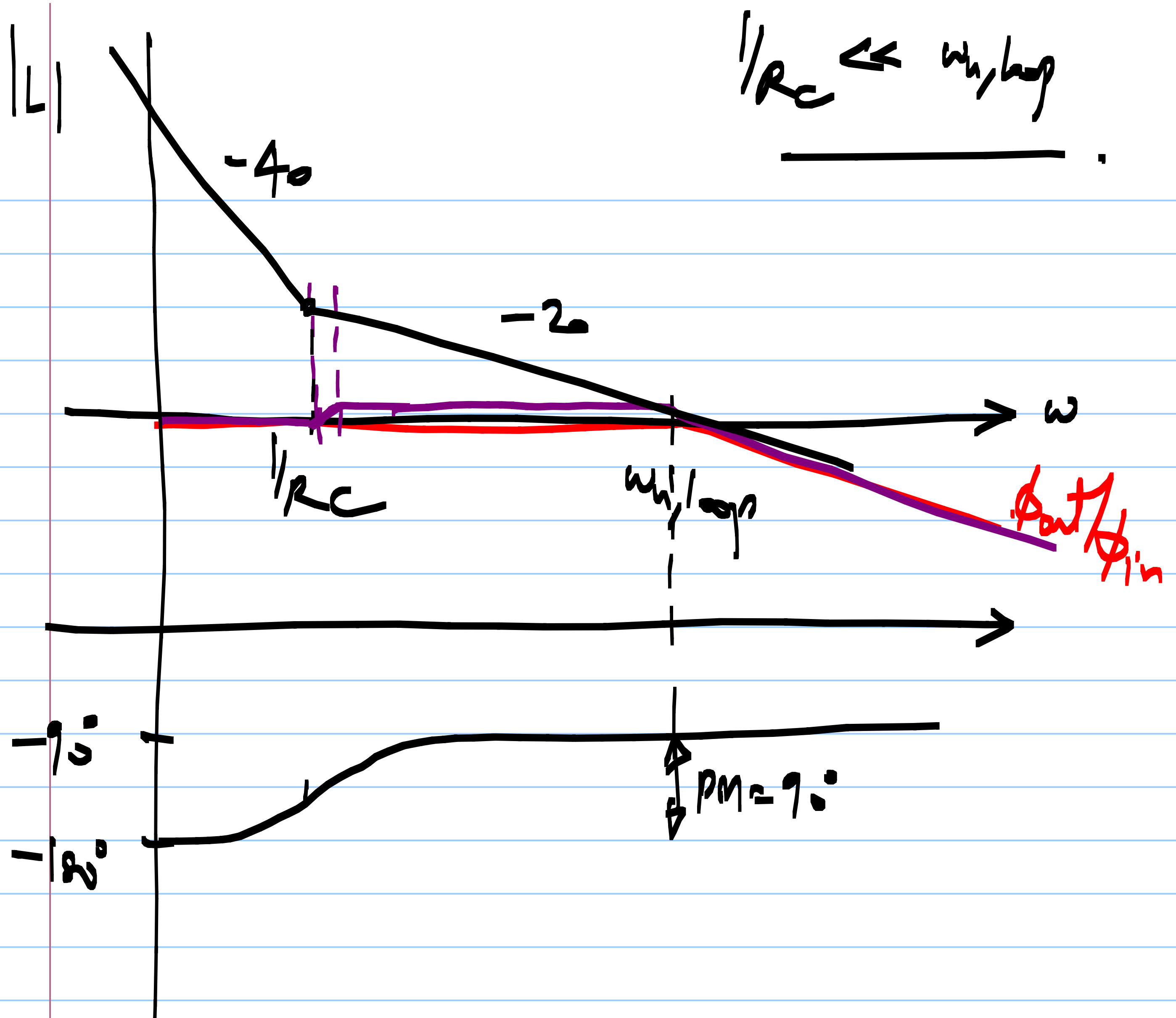


$$\frac{\phi_{out}}{\phi_{in}} = \frac{1 + sCR}{1 + sCR + s^2 \cdot \frac{C}{K_{vco} \cdot I_{cp}}} \; ; \quad L(s) = \frac{I_{cp} K_{vco}}{s}\left(R + \frac{1}{sC}\right)$$

* For stability, zero $\frac{1}{RC} < \omega_{n,loop}$

$$\omega_{n,loop} \simeq I_{cp} R K_{vco} \quad (rad/s)$$

$$\frac{1}{RC} \ll \omega_{1,loop}$$



$$\frac{\phi_{out}}{\phi_{in}} = \frac{L}{1+L}$$

(1st order lowpass)

$$\frac{\phi_{out}}{\phi_{in}} = \frac{1 + sCR}{1 + sCR + s^2 \ldots}$$

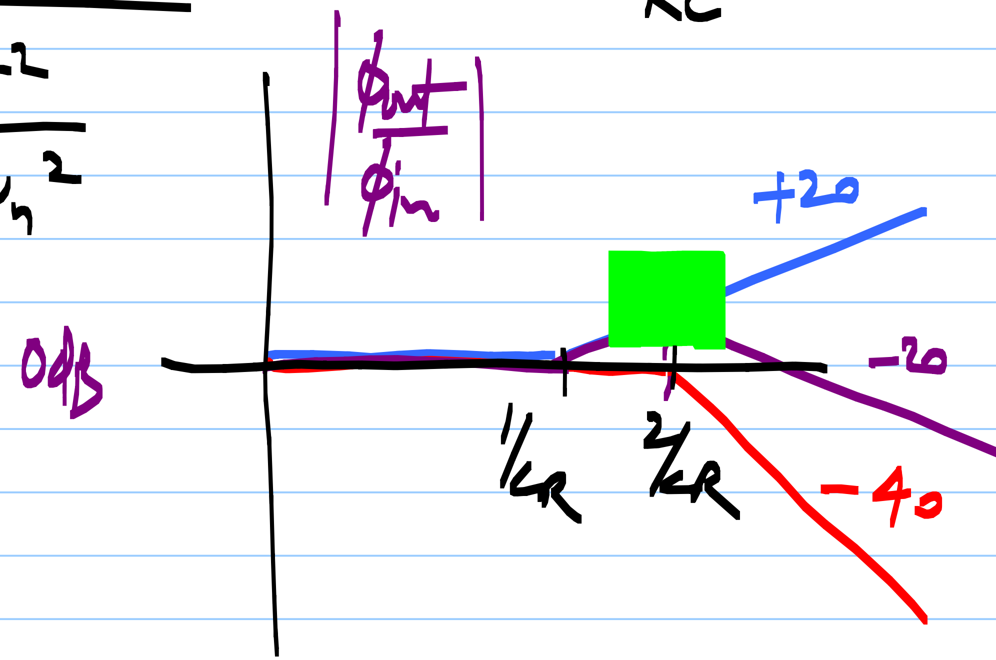
$$\frac{}{1 + 2\frac{s}{\omega_n} + \frac{s^2}{\omega_n^2}}$$

$$= \frac{1 + sCR}{\left(1 + s\frac{CR}{2}\right)^2}$$

$\zeta = 1$

2 identical poles @ $s = -\omega_n$

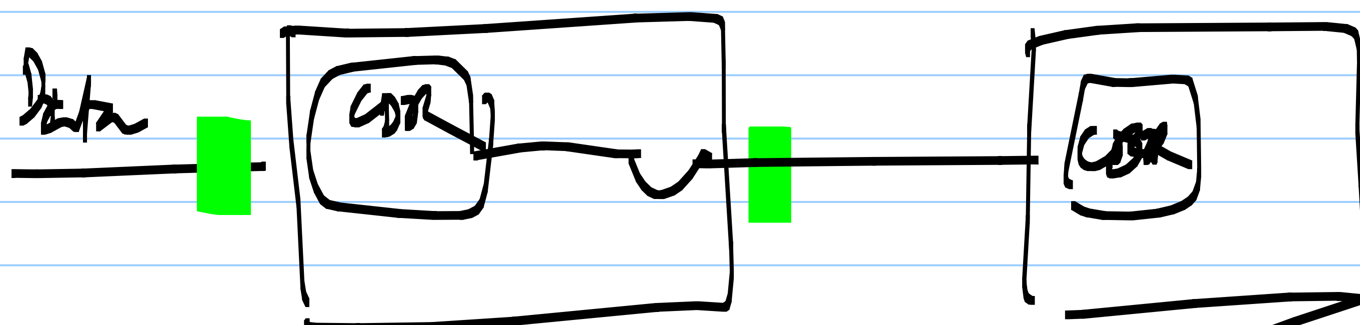
$$\omega_n = \frac{2}{RC}$$



Peaking in the transfer function

Smaller ζ ⇒ higher peaking

⇒ output clock jitters more than the input clock



jitter peaking < 0.1 dB

Very bad in systems like SONET – Data regenerated & transmitted using the recovered clock

Because of the zero, jitter peaking is worsened.

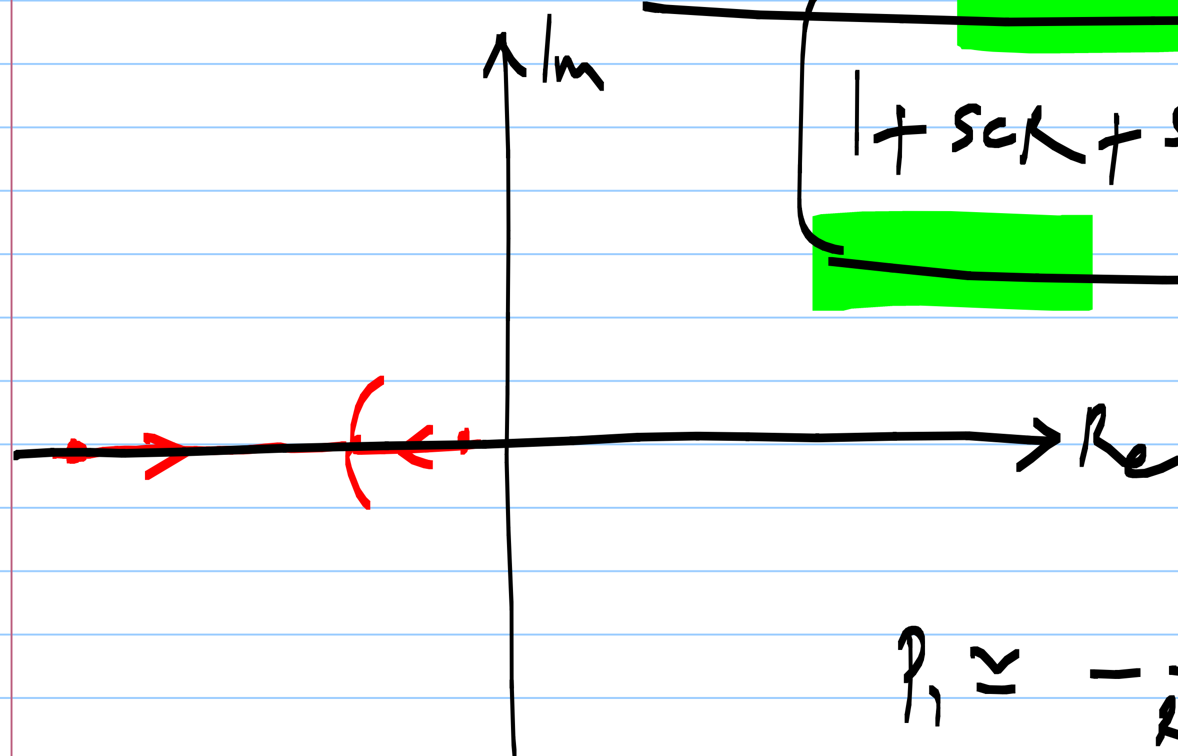
$\Rightarrow$ Have to design with ζ much more than 1

$$\zeta \sim 5$$

Large ζ

$$1 + 2\zeta\frac{s}{\omega_n} + \frac{s^2}{\omega_n^2}$$

$$1 + sCR + s^2\frac{C}{K_{vco} \cdot I_{cp}} \quad D(s)$$



p_1, p_2

$$p_1 \simeq -\frac{1}{RC}$$

$$p_2 \simeq -I_{cp} R K_{vco}$$

$$ax^2 + bx + c = 0 \qquad x_1 , x_2$$

$$a x_1^2 + b x_1 \simeq 0 \qquad |x_1| \gg |x_2|$$

$$b x_2 + c \simeq 0$$

$$x_1 \simeq -\frac{b}{a}, \quad x_2 \simeq -\frac{c}{b}$$

$$\frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

$$\frac{\phi_{out}}{\phi_{in}} = \frac{1 + sCR}{1 + sCR + s^2 \frac{C}{K_{VCO} \cdot I_{cp}}}$$

$z_1 = -1/CR$

$p_1 \simeq -1/CR$

$p_2 \simeq -I_{cp} R \cdot K_{VCO}$

Poles separated large from each other

@ p_1 slightly higher freq. than $1/CR$

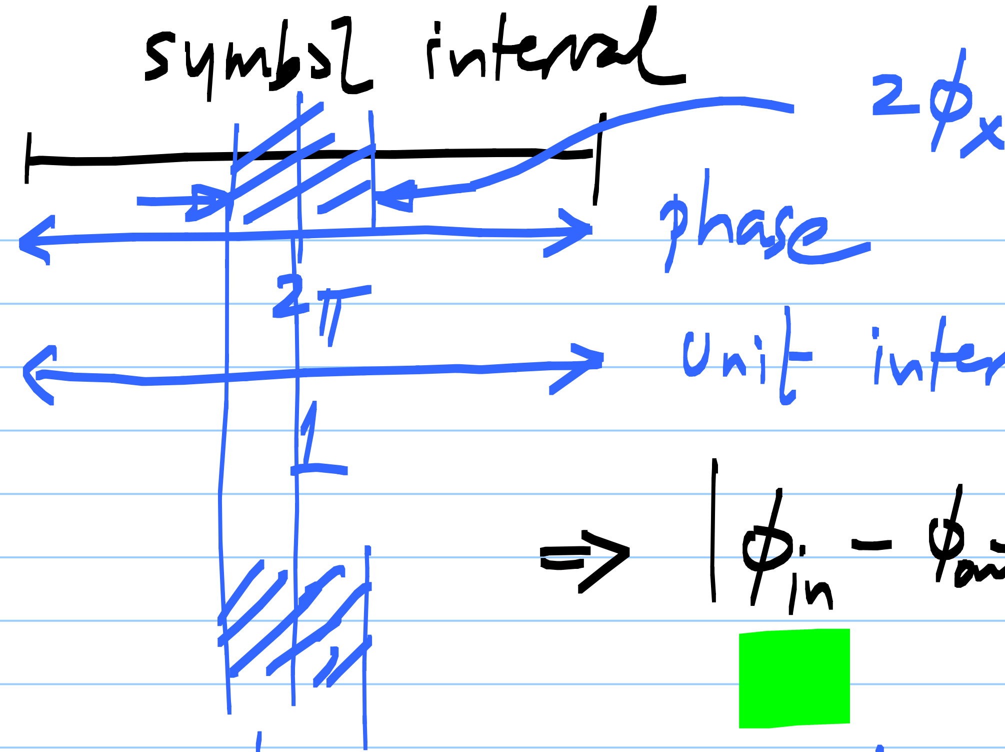
⇒ peaking

Closed loop bandwidth: $\omega_{u,loop} = I_{cp} R K_{VCO}$

Jitter transfer JTRAN . $\dfrac{\phi_{out}}{\phi_{in}}$

Jitter tolerance JTOL :

Amount of jitter that can be tolerated while maintaining the performance (BER < specification)



$$\Rightarrow \left|\phi_{in} - \phi_{out}\right| < \phi_x$$

clock has to be within this interval ($\pm\,\phi_x$ from the center) to meet BER specifications

$|\phi_{in}|$ such that $|\phi_{in} - \phi_{out}| < \phi_x$

$$|\phi_{in}| \underbrace{\left|1 - \frac{\phi_{out}}{\phi_{in}}\right|} < \phi_x$$

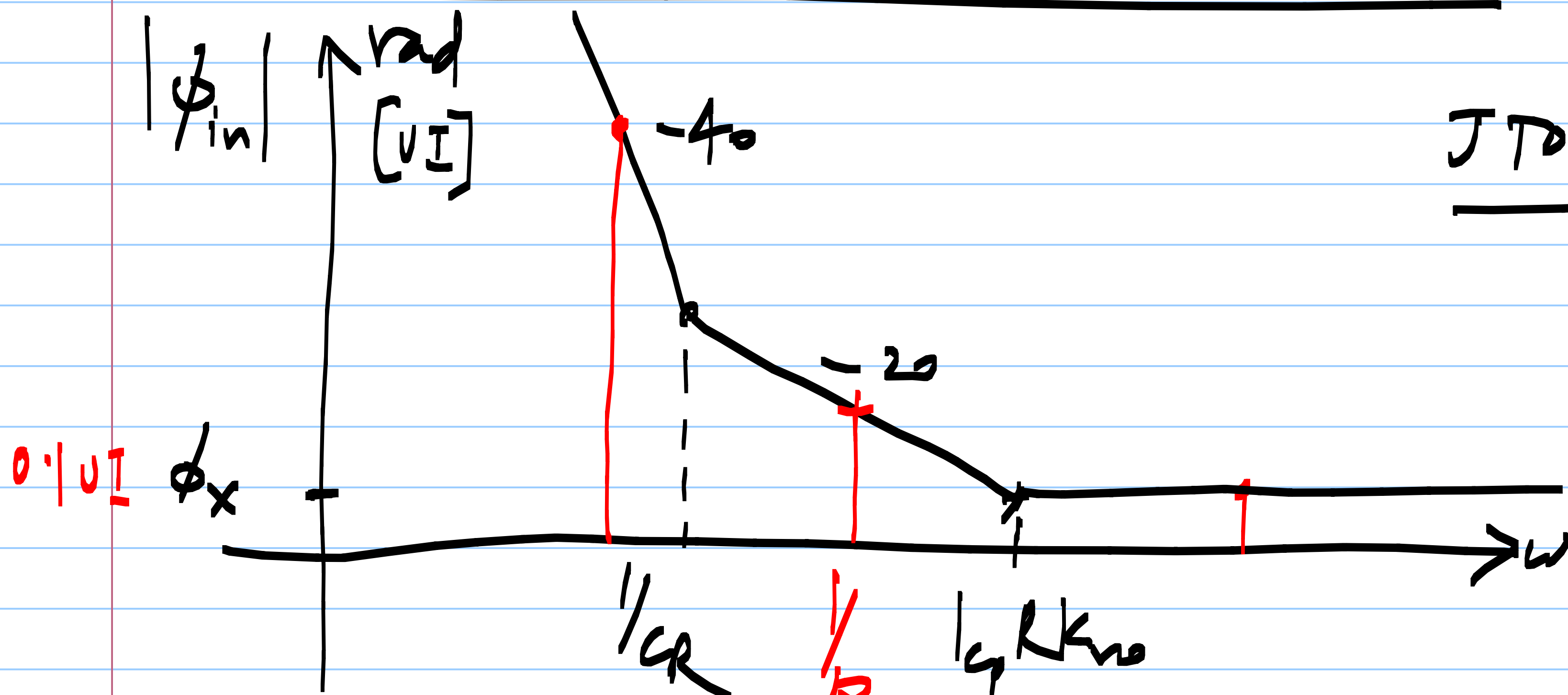
$$|\phi_{in}| < \frac{\phi_x}{\dfrac{s^2 C / I_{cp} K_{vco}}{1 + sCR + \dfrac{s^2 C}{I_{cp} \cdot K_{vco}}}}$$

$$1 - \frac{\phi_{out}}{\phi_{in}} = \frac{\dfrac{s^2 C}{I_{cp} K_{vco}}}{1 + sCR + s^2 \dfrac{C}{I_{cp} K_{vco}}}$$

$$\frac{1 + sCR + s^2 C / I_{cp} K_{vco}}{\dfrac{s^2}{I_{cp} K_{vco}}}$$

$$\frac{sCR}{s^2 \cancel{C} / I_{cp} K_{vco}}$$

$$|\phi_{in}| < \phi_x \left| \left[1 + \frac{I_{cp} R K_{vco}}{s} + \frac{I_{cp} K_{vco}}{s^2 C} \right] \right|$$



JTOL