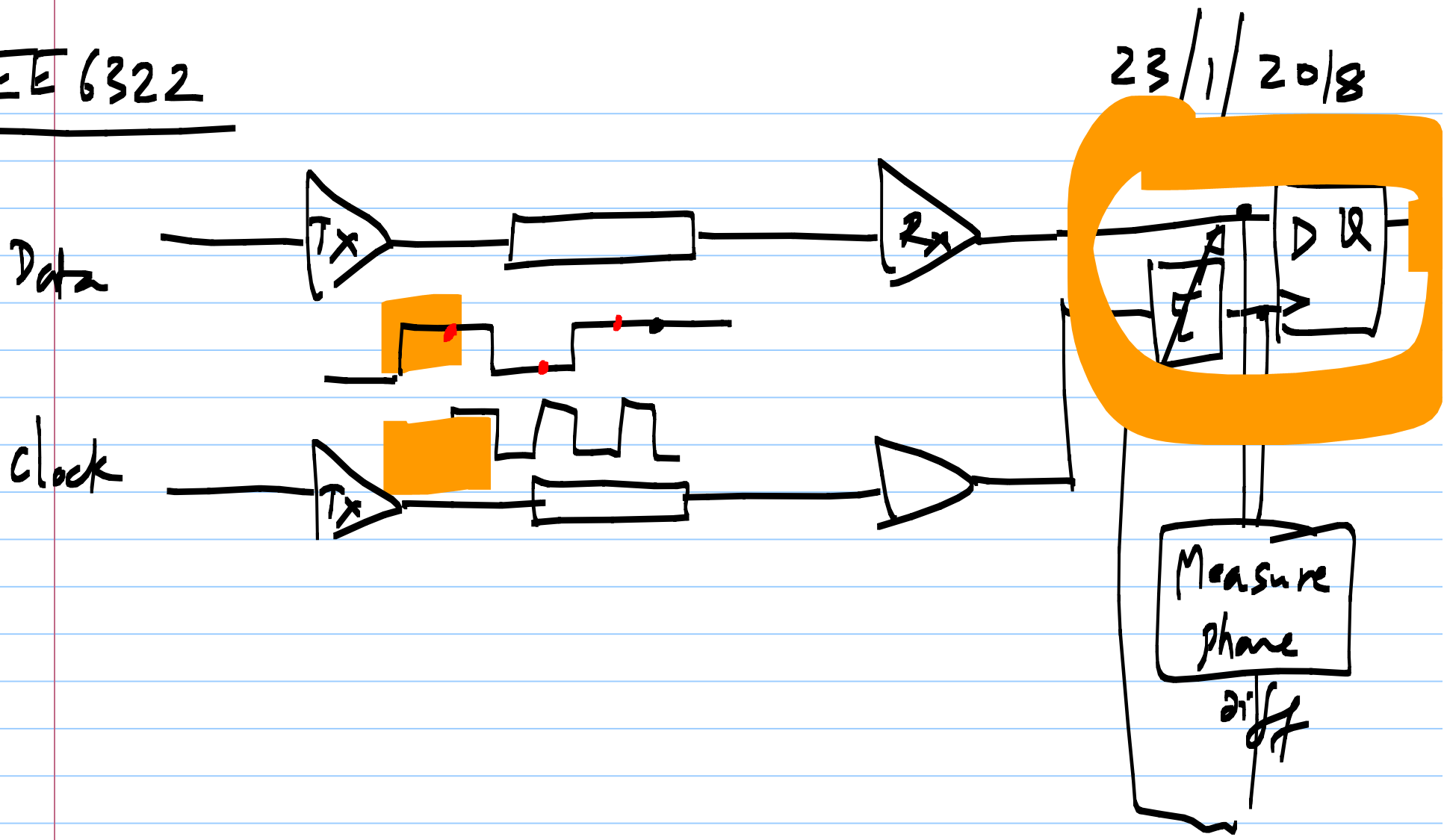
EE 6322

23/1/2018



10Gb/s

100ps

AIR/VACUUM

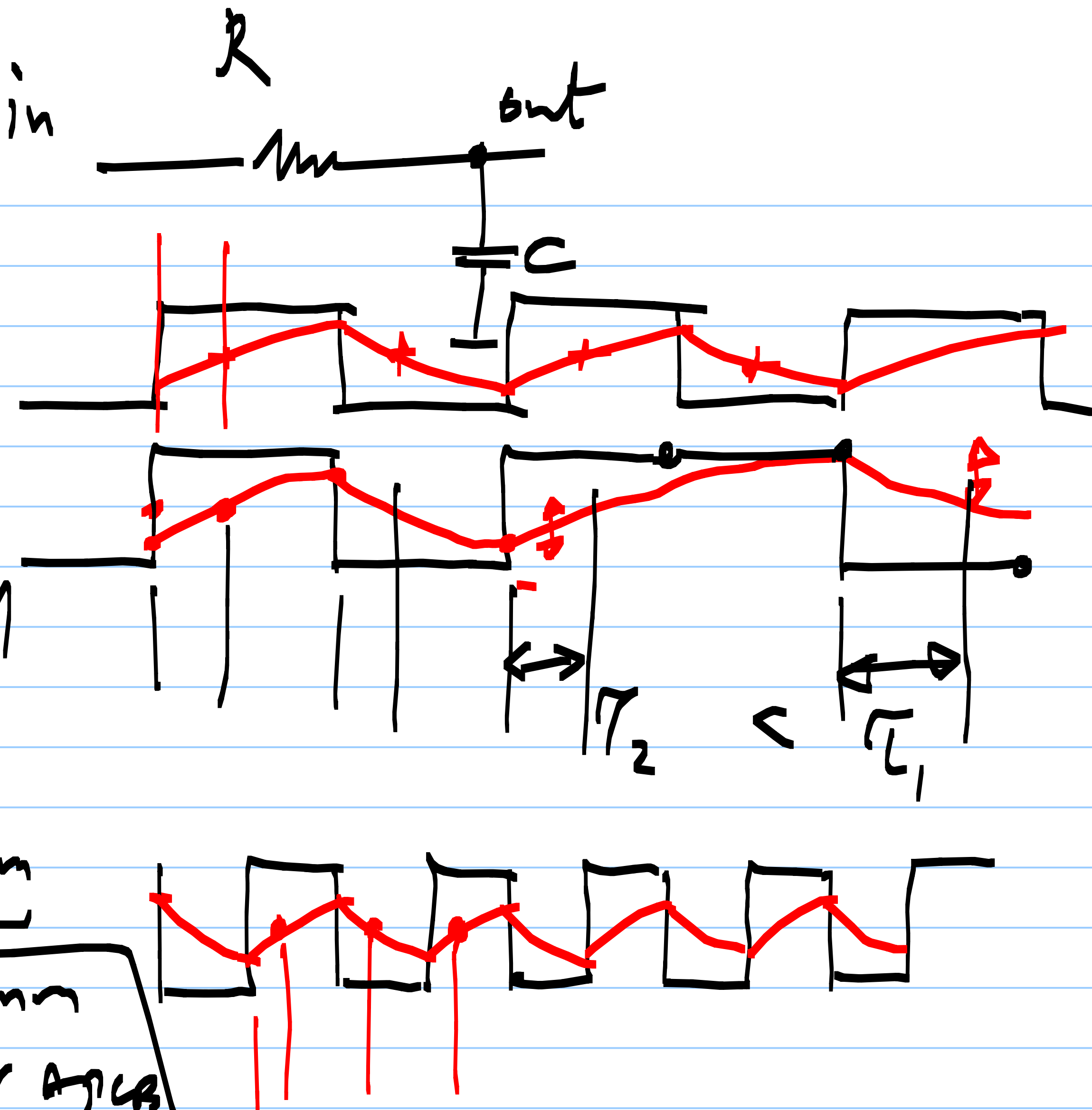
300m/μs

300mm/ns

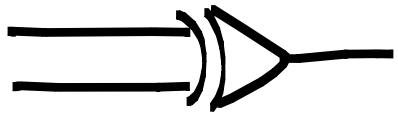
300μm/ps

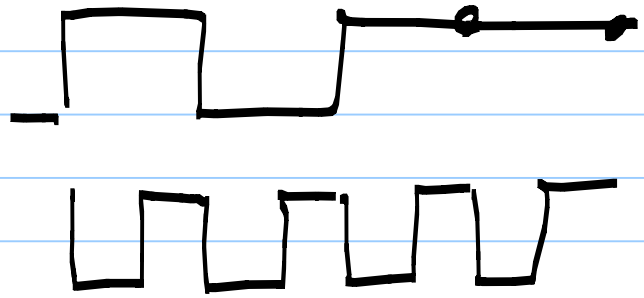
30mm

15mm on A PCB



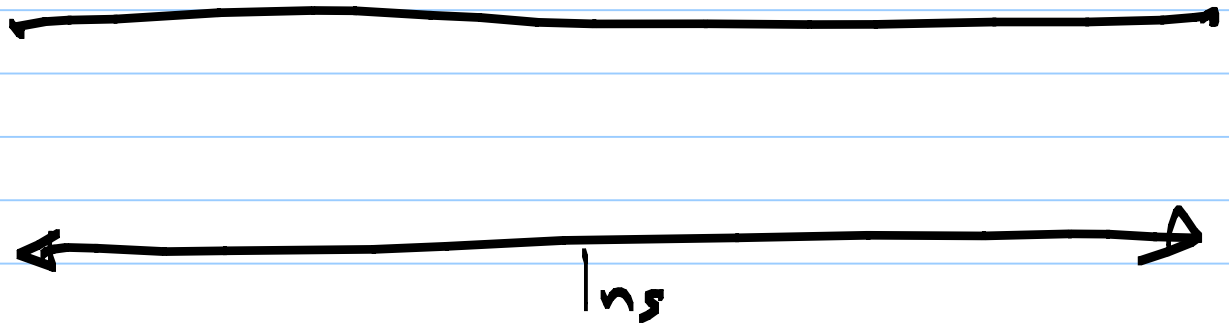
XOR gate

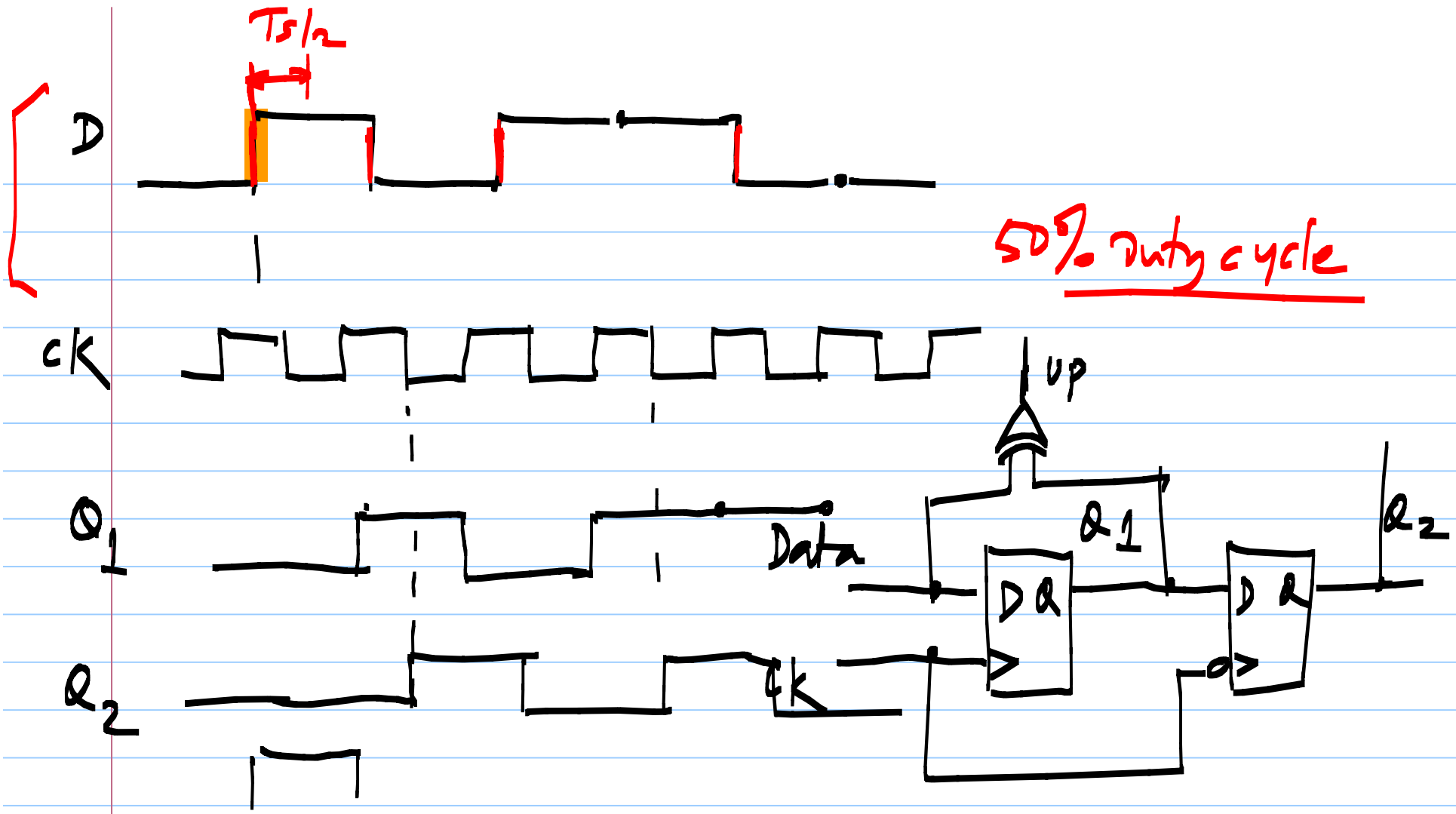


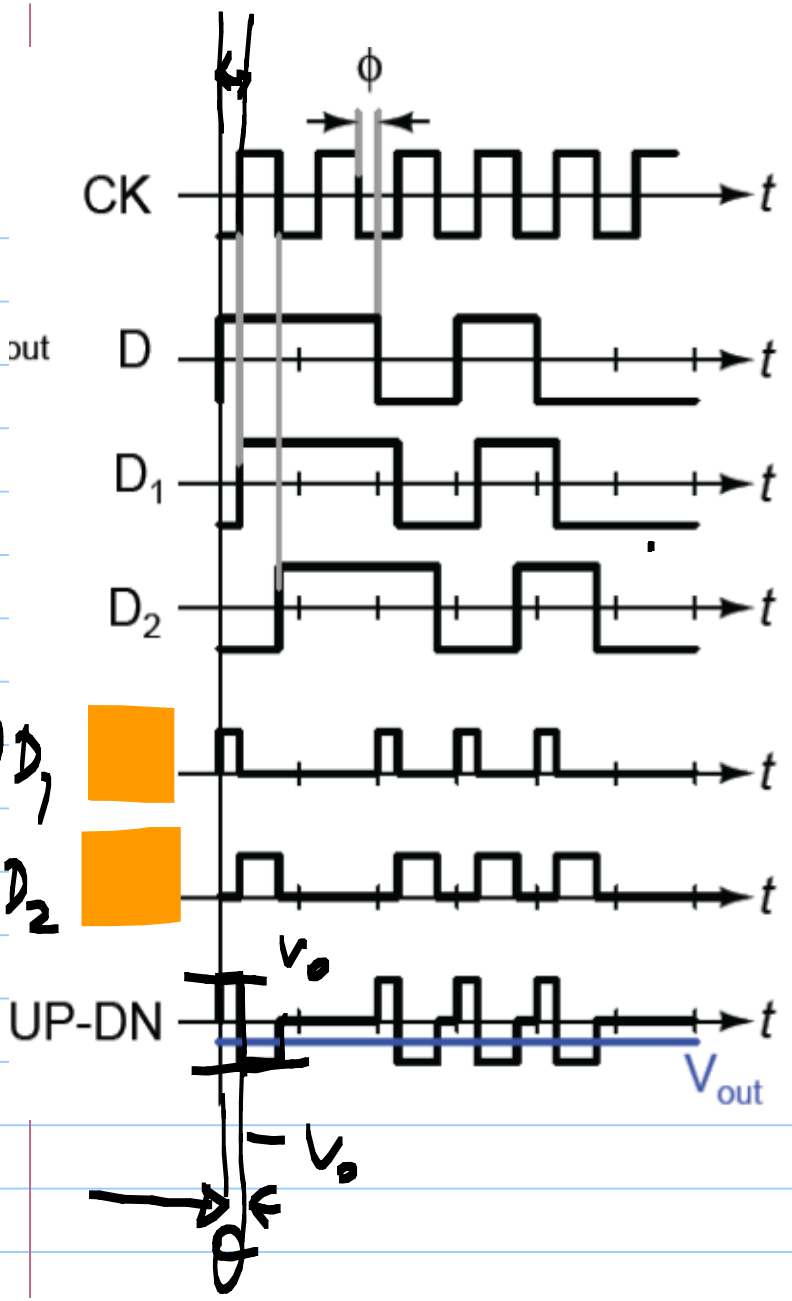


Multiplier

3-state



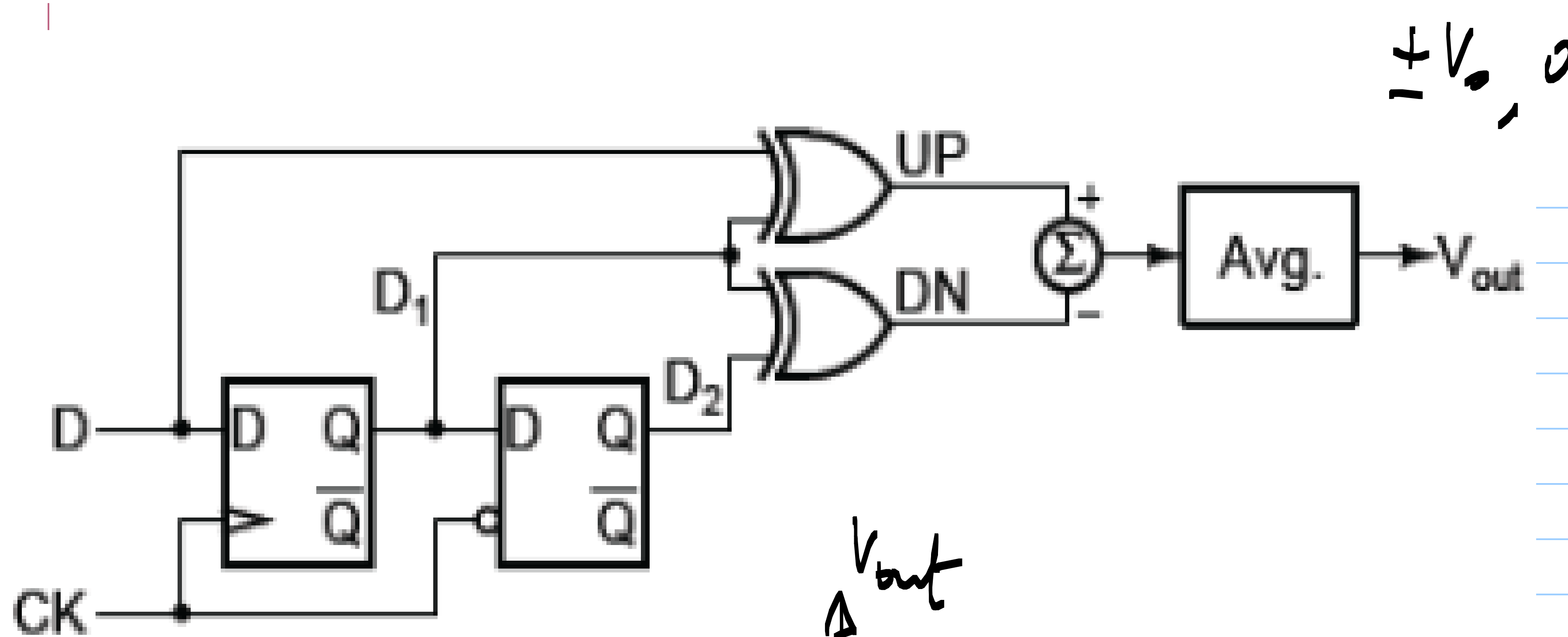

Ts/2
D
50% Duty cycle
CK
up
Q1
Data
Q1
Q2
D Q
D Q
Q2
CK



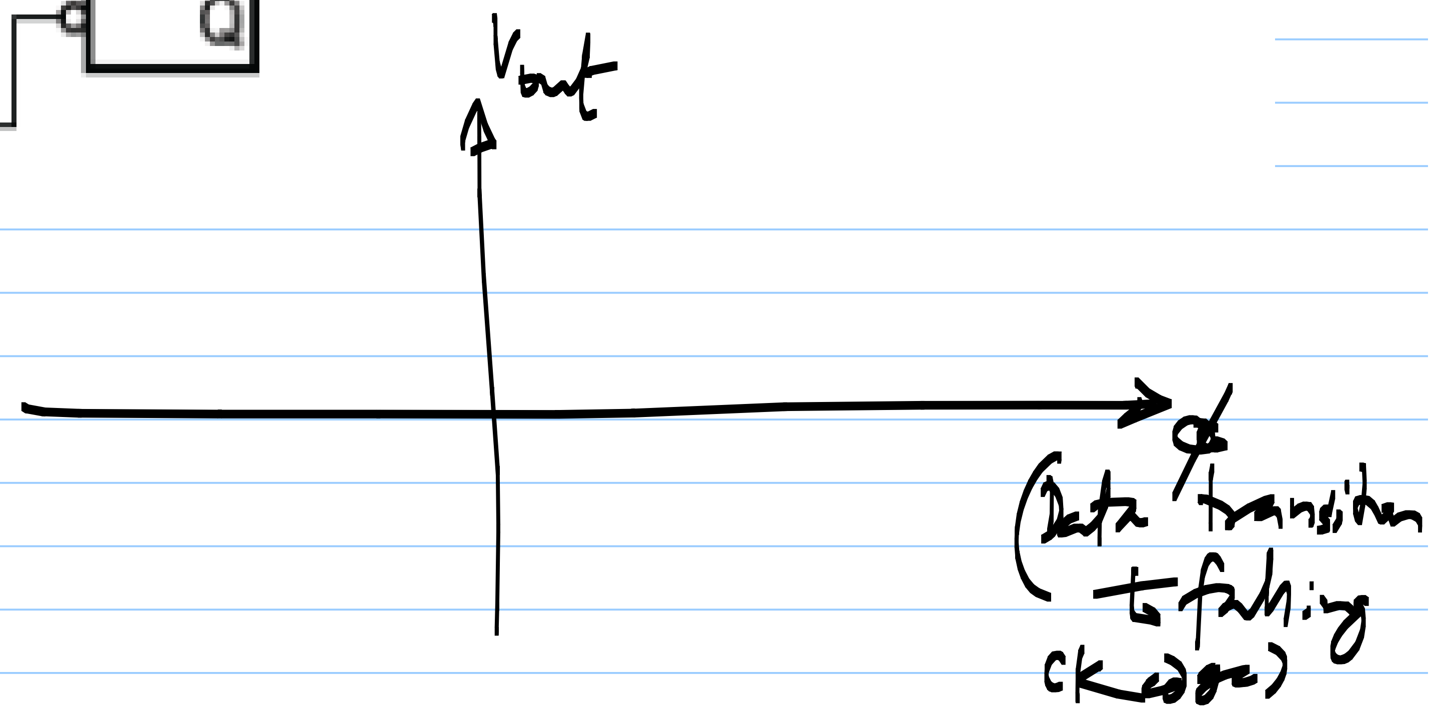
If Area(UP) > Area(DN)

pulses of width = data transition interval between & rising edge

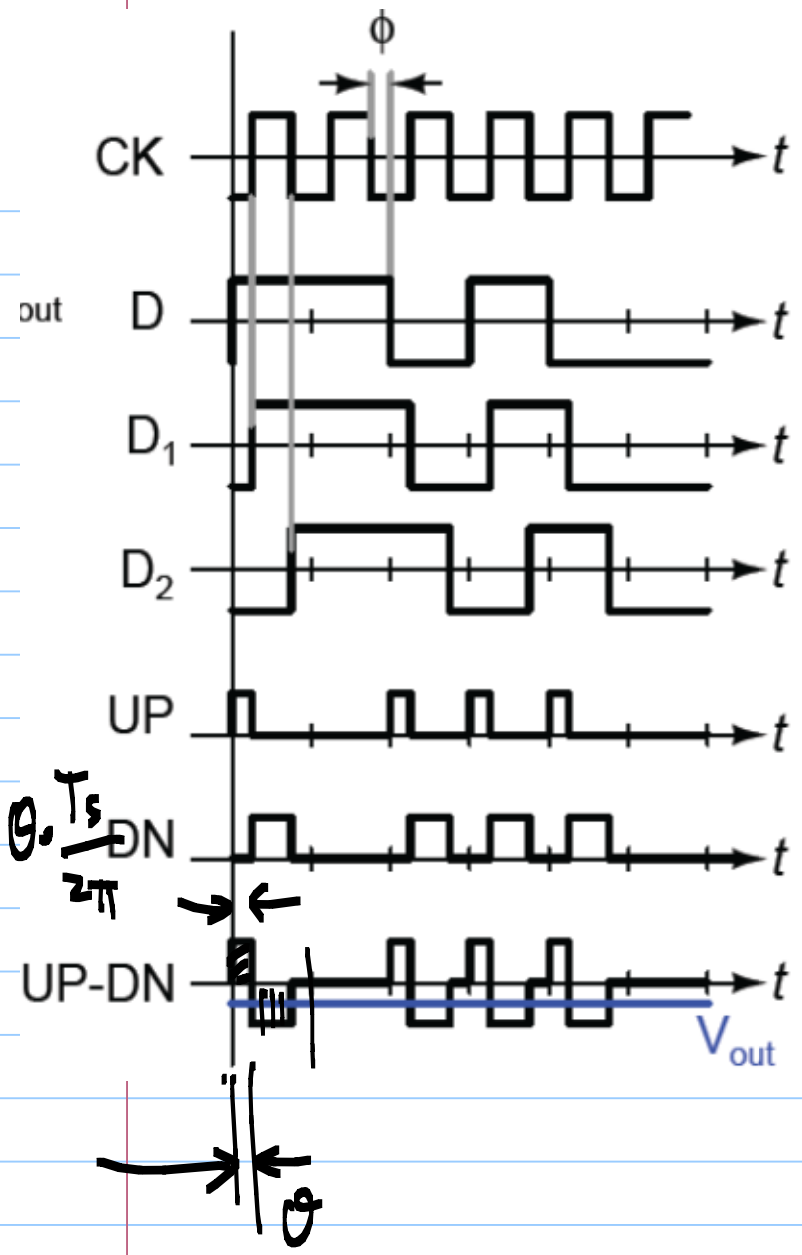
pulses of width $T_S/2$



D
CK
D
Q
Q
D₁
D
Q
Q
D₂
UP
DN
+
−
Σ
Avg.
Vout
±V₀, 0



Vout
φ
(Data transition to falling CK edge)



$$\frac{V_0 \cdot \theta - V_0 \cdot \pi}{2\pi} = V_0 \cdot \frac{\theta - \pi}{2\pi}$$

avg. when there is a transition

$$\frac{V_0 \cdot \theta \cdot \frac{T_s}{2\pi} - V_0 \cdot \frac{T_s}{2}}{T_s} = V_0 \cdot \frac{\theta - \pi}{2\pi}$$

$\theta = \phi + \pi$

P(transition) × avg : $V_0 \cdot \frac{\phi}{2\pi}$

Perfectly aligned: $\theta = \pi$ or 0 (DF)

Ans.