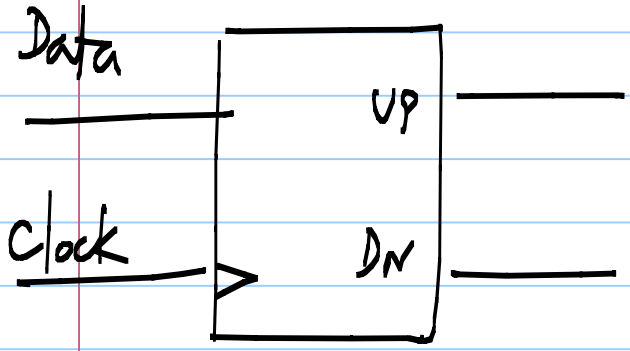
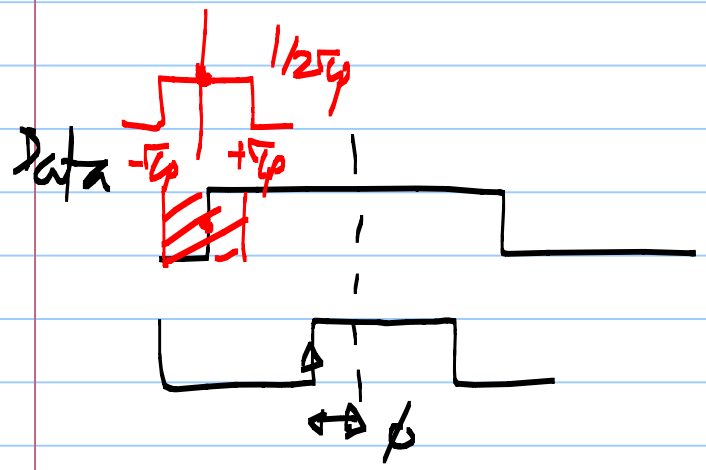
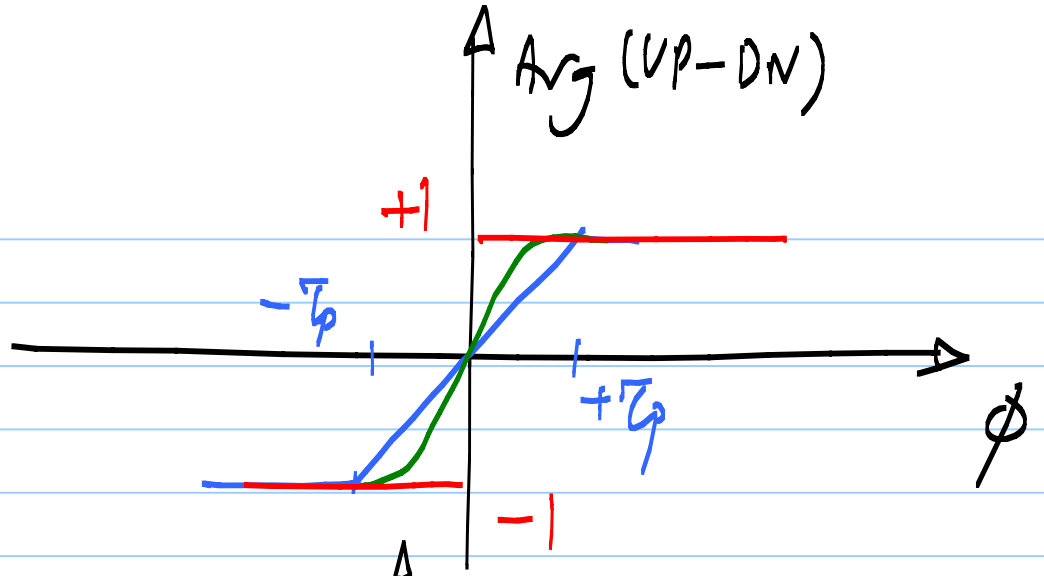
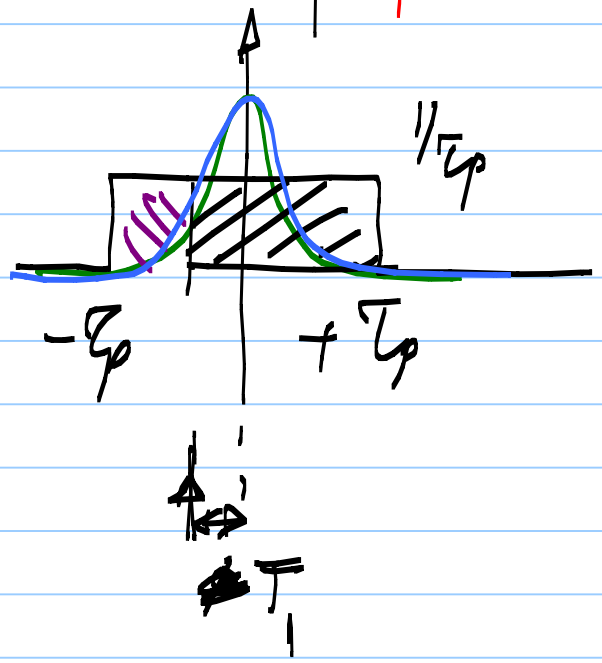
Lecture 26

BB phase detector





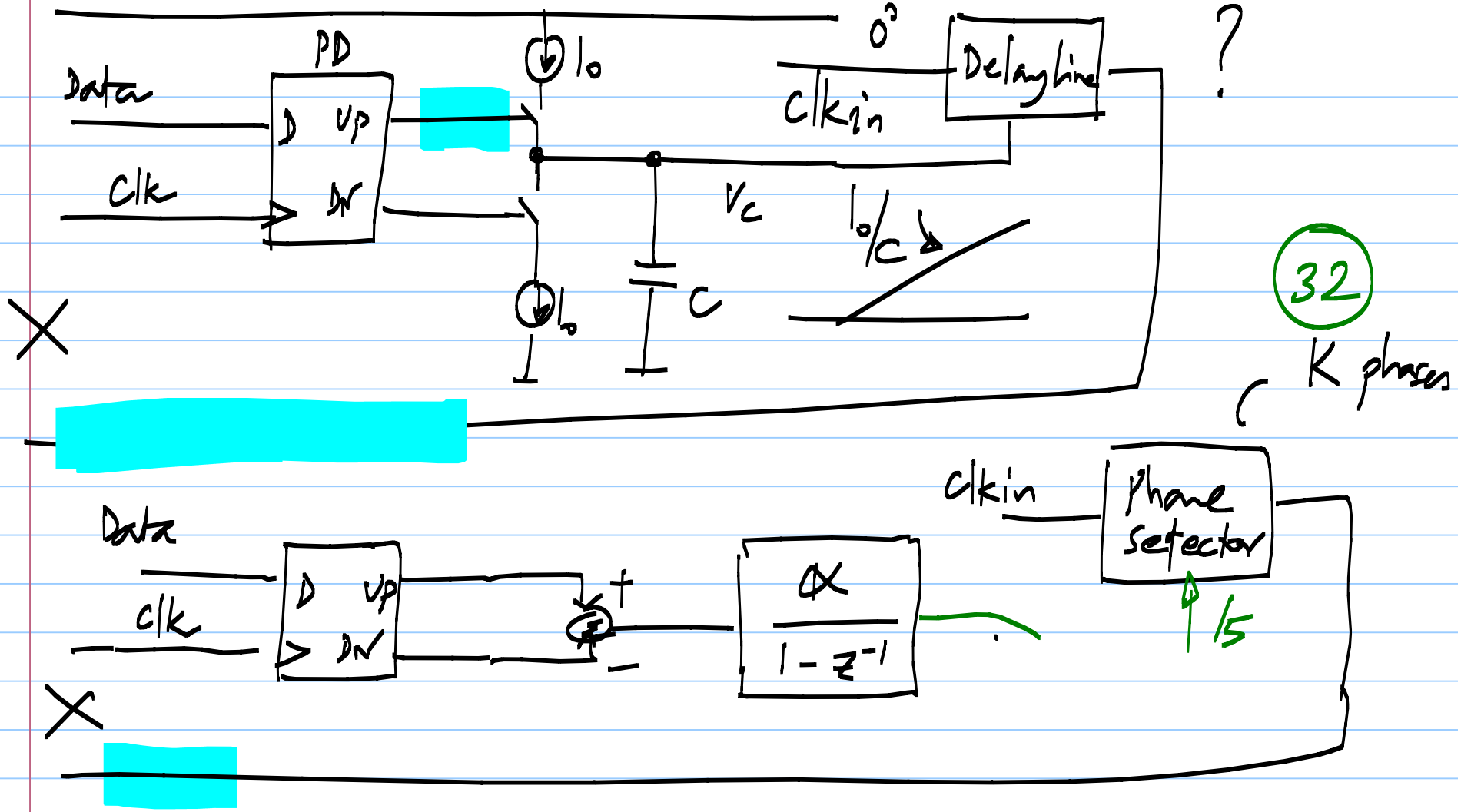


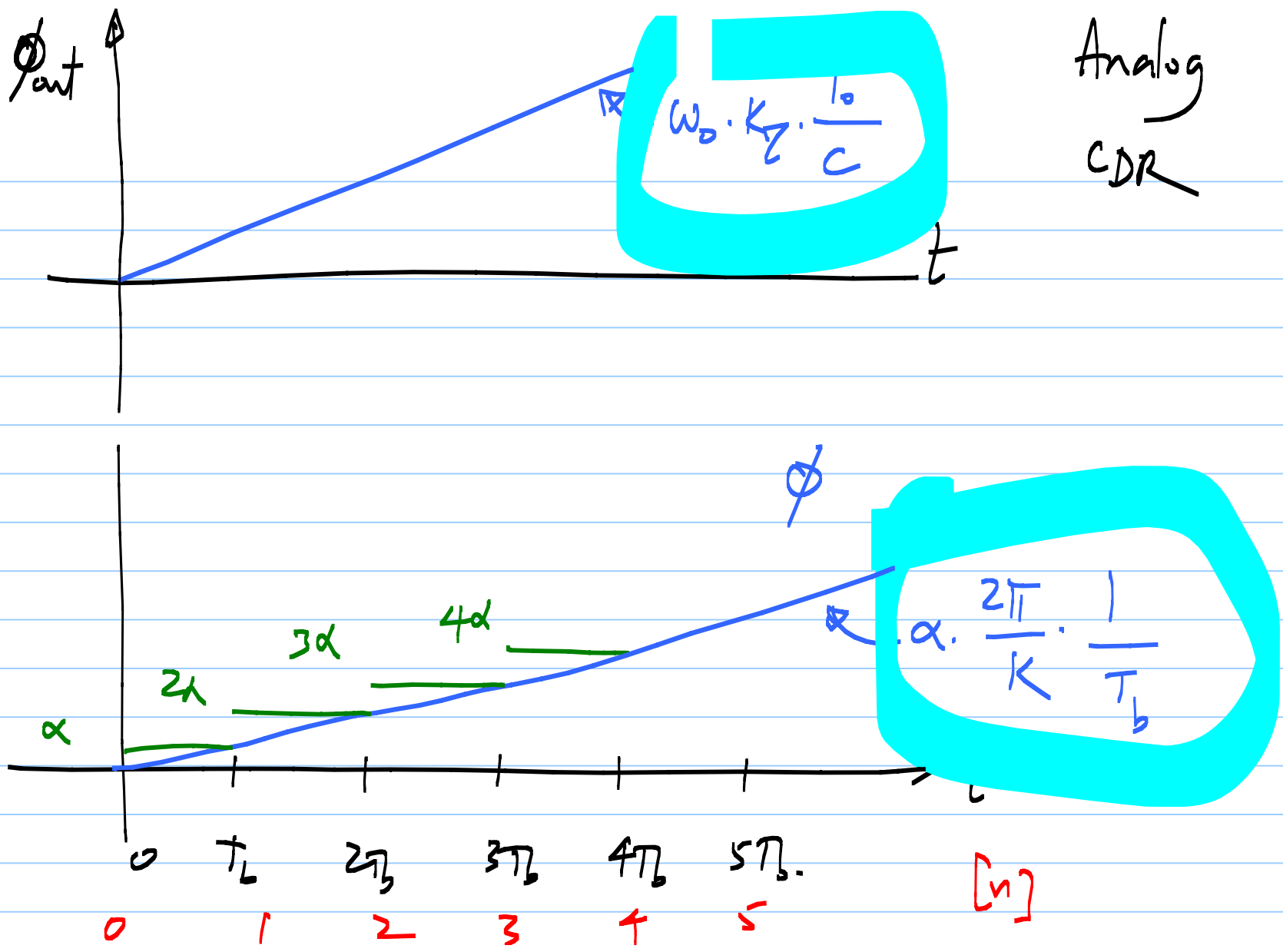


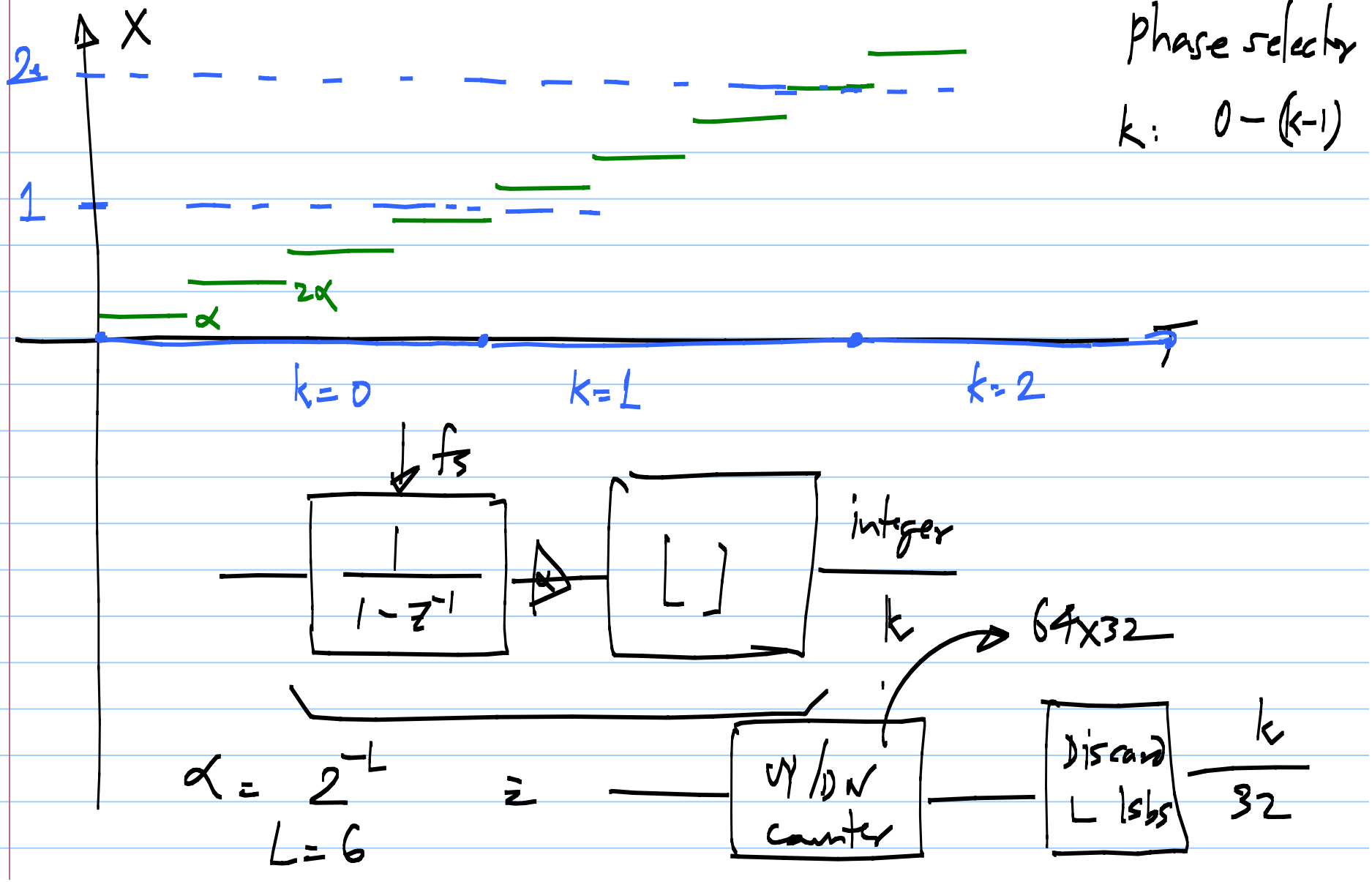
- Gain of the BB PD depends on input jitter
- Must characterize CDR (JTOL, BW) for a given input jitter

	Linear PD	BB PD
Gain:	$\frac{1}{2\pi} \cdot DF$	$\propto \frac{1}{2\pi} \frac{T_b}{T_{j,rms}} \cdot DF$

BB CDR with forwarded clock




ϕ_{out}
$\omega_0 \cdot K_{VCO} \cdot \frac{1}{C}$
t
Analog
CDR
ϕ
α
2α
3α
4α
$\alpha \cdot \frac{2\pi}{K} \cdot \frac{1}{T_b}$
0
T_b
$2T_b$
$3T_b$
$4T_b$
$5T_b$
t
0
1
2
3
4
5
[n]


X
2
1
α
2α
k=0
k=1
k=2
phase selector
k: 0 – (k-1)
fs
1
1 - z^-1
⌊ ⌋
integer
k
64x32
W/DN counter
Discard L lsbs
k
32
z
α = 2^-L
L=6

Analogy between digital & analog CDR

Phase increments (with broken loop) same in the two cases (continuous approximation to the quantized phase)

Digital CDRs / PLLs

* Smaller area
* Avoid large, leaky loop filter capacitor
* Portability to different technologies
* Easy to set the initial state

- Power hungry
- Spurious signals

CDR without a forwarded clock