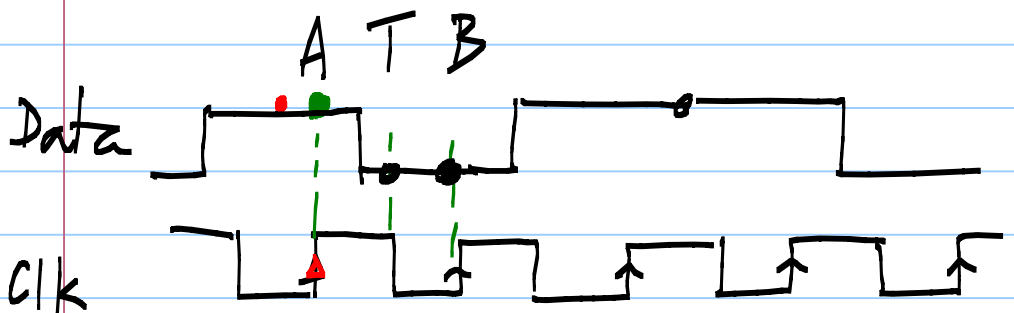
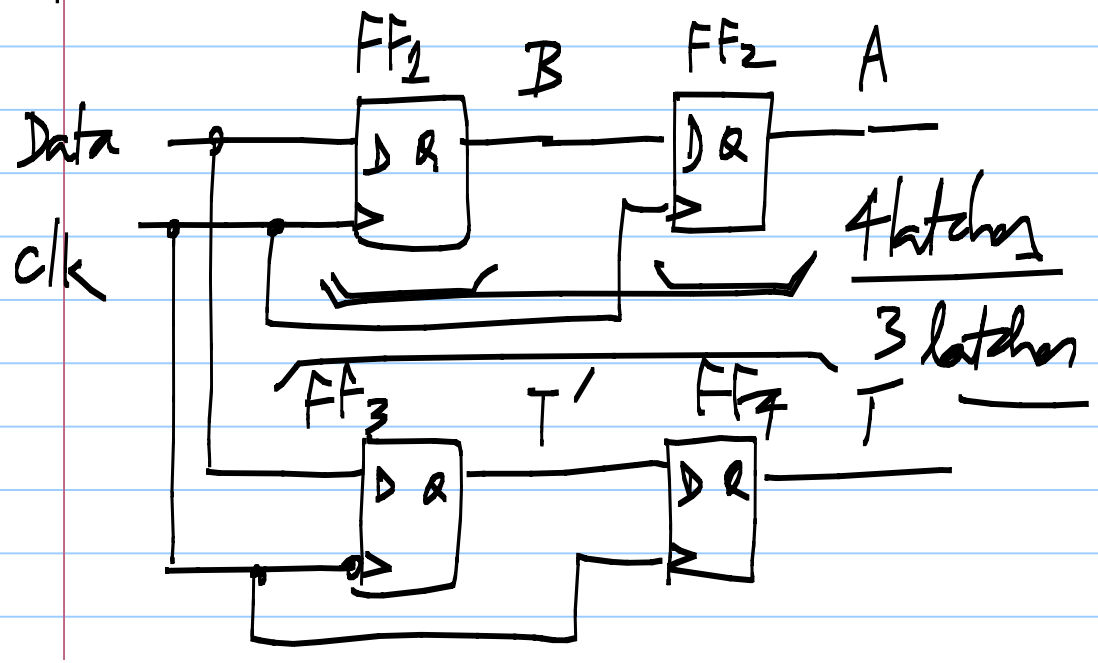
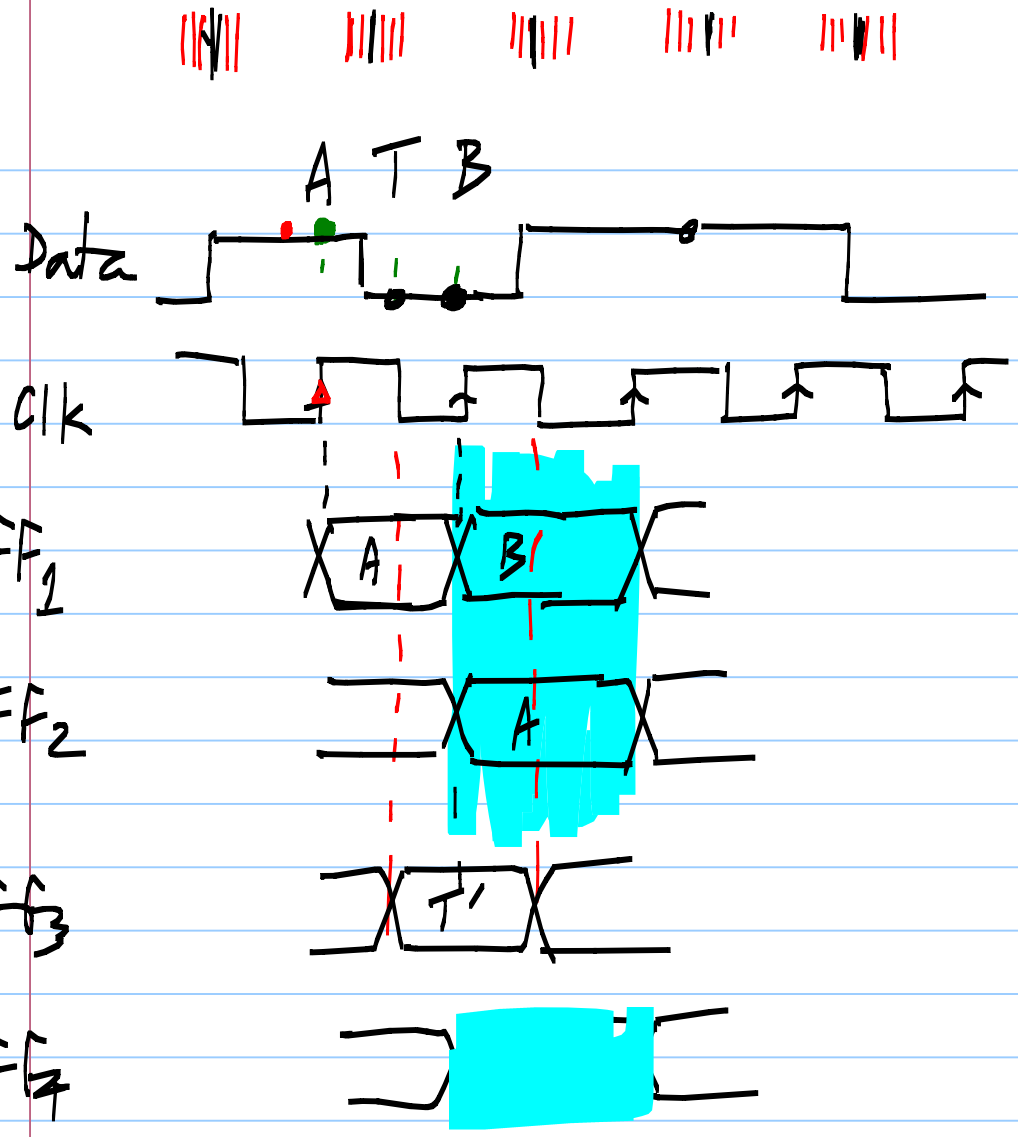
Lecture 6.

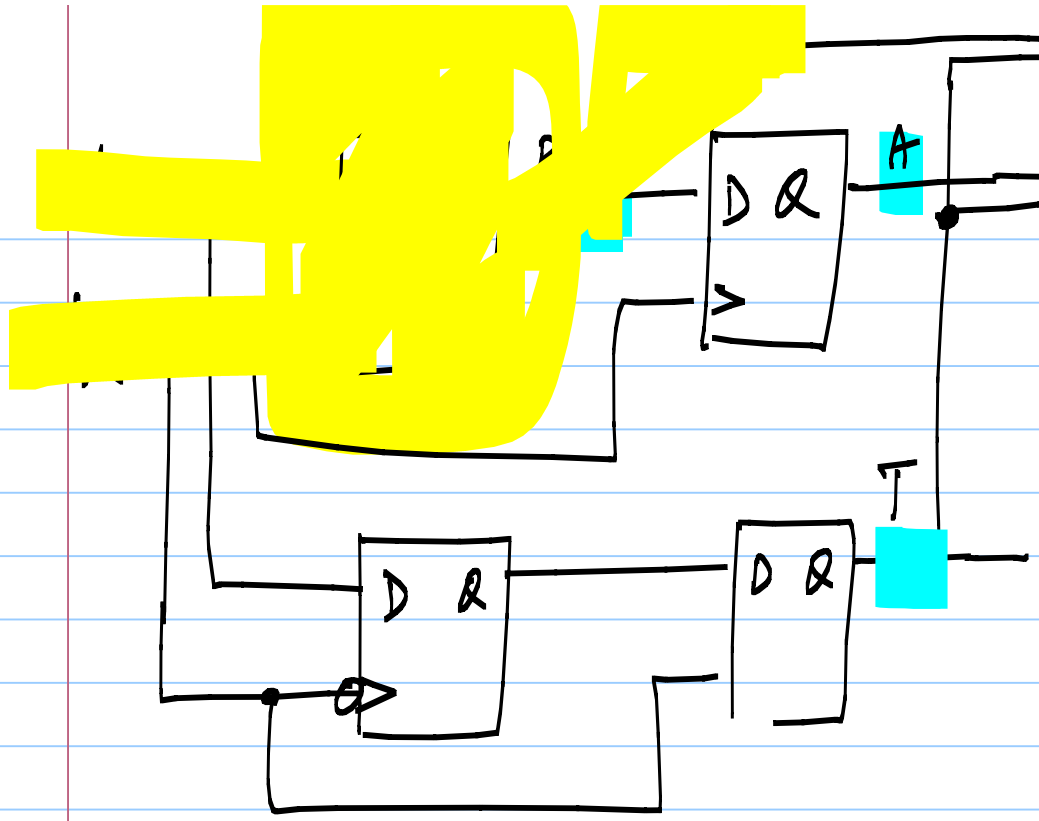


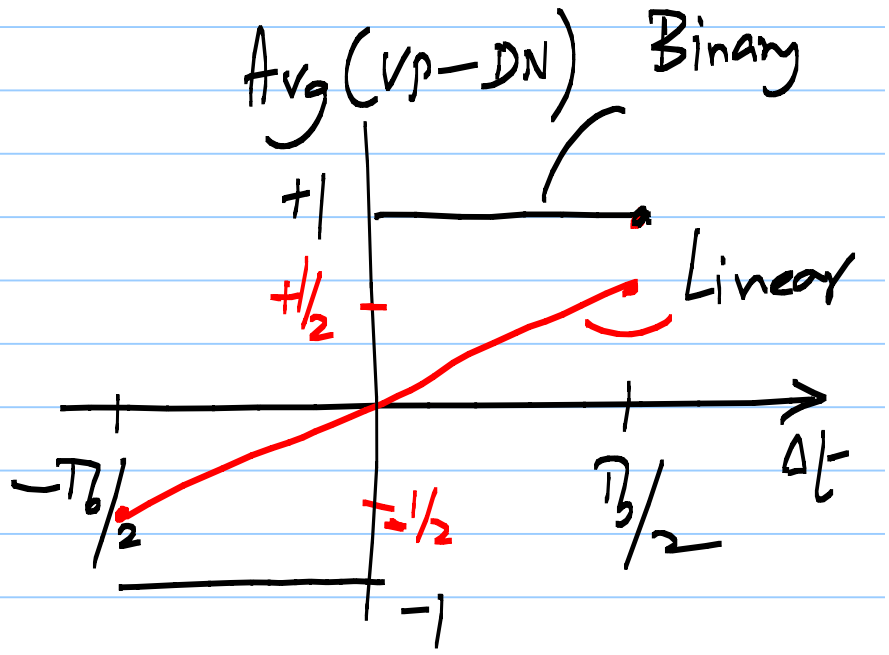


A	T	B	
0	0	0	no transition
0	0	1	Early
0	1	0	X
0	1	1	Late
1	0	0	Late
1	0	1	X
1	1	0	Early
1	1	1	no transition



A	T	B	Late UP	Early DN
0	0	0	0	0
0	0	1	0	1
0	1	0	x 1	x 1
0	1	1	1	0
1	0	0	1	0
1	0	1	x 1	x 1
1	1	0	0	1
1	1	1	0	0
			A⊕T	B⊕T



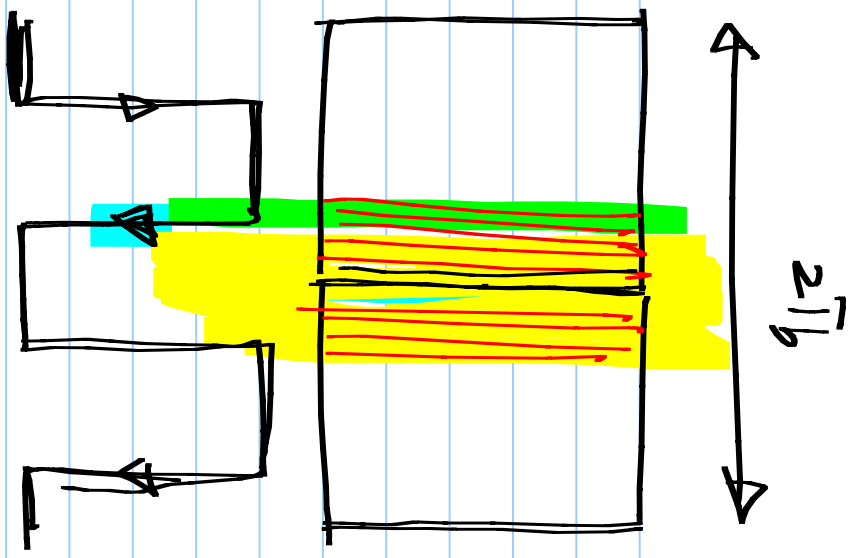


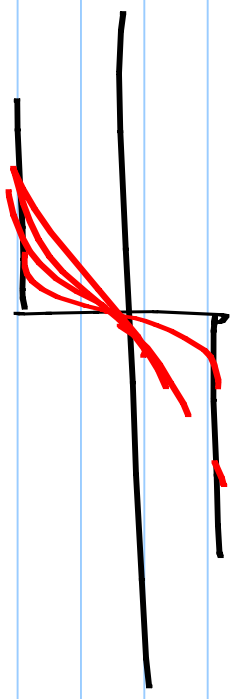
Binary phase detector

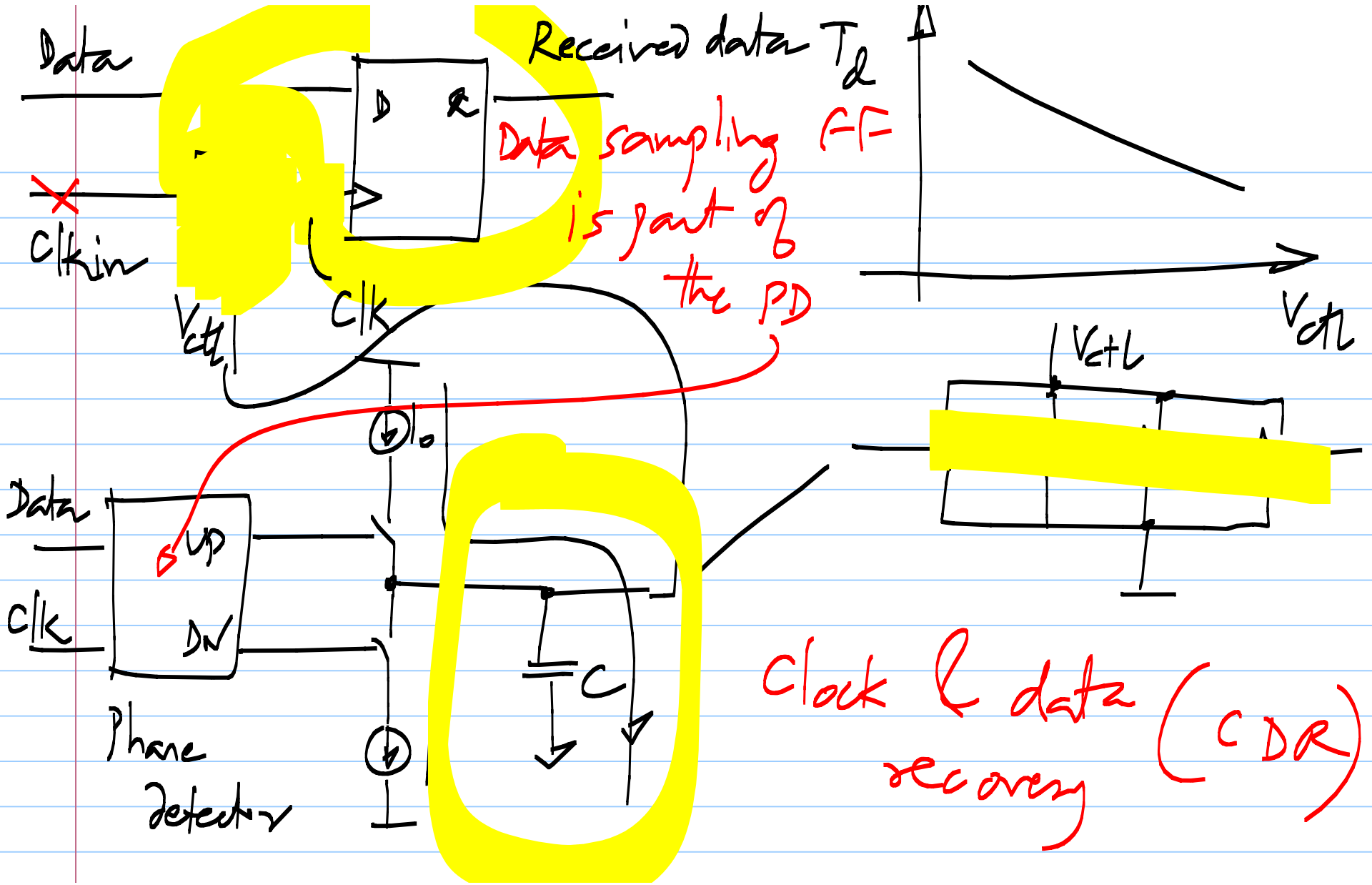
JDH

Alexander PD

Linear (Hogge) PD	Binary (Alexander) PD
2 FFs (4 latches) 2 XOR gates 1 delay (gate)	7 latches 2 XOR gates
(Locked condition) UP, DN: width of $\frac{T_b}{2}$	UP, DN: width of T_b
offset: $t_{ckq} - t_d$ (input ref.)	0


h=2




Data
Received data
D
Q
Data sampling FF
is part of
the PD
clk_in
clk
V_ctl
I_0
Data
UP
clk
DN
C
Phase
detector
T_d
V_ctl
V_ctl
clock & data
recovery
(CDR)