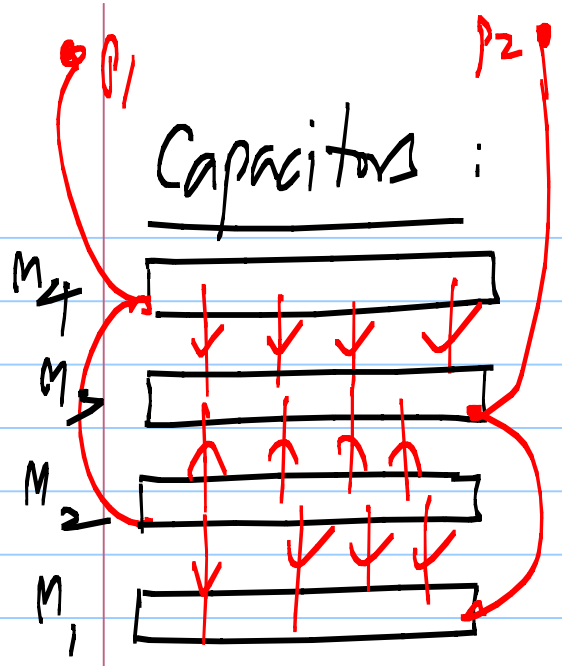
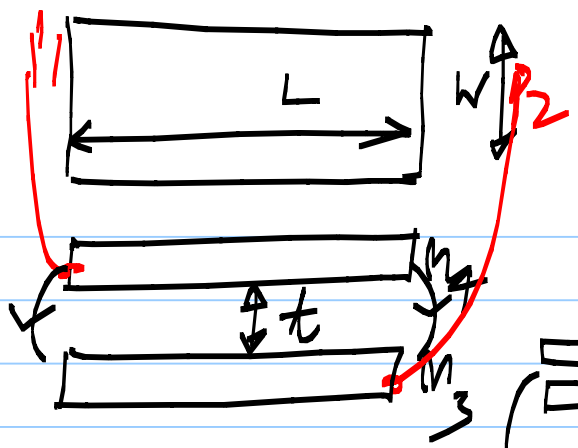
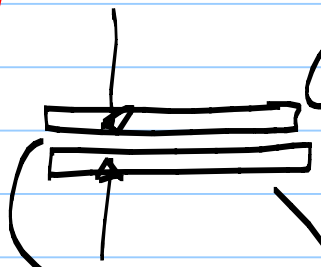




$\left(\frac{\epsilon}{t}\right) WL$ — $C'_{M_3-M_4}$



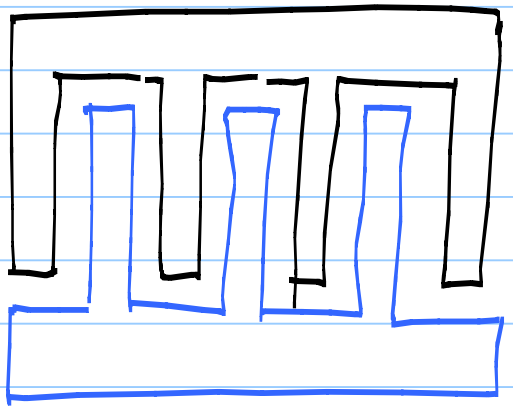
$C = C'_{M_3-M_4} \cdot WL + C''_{M_3-M_4}(2W+2L)$

thin dielectric

Special layers for a capacitor

p –

Interdigitated capacitors

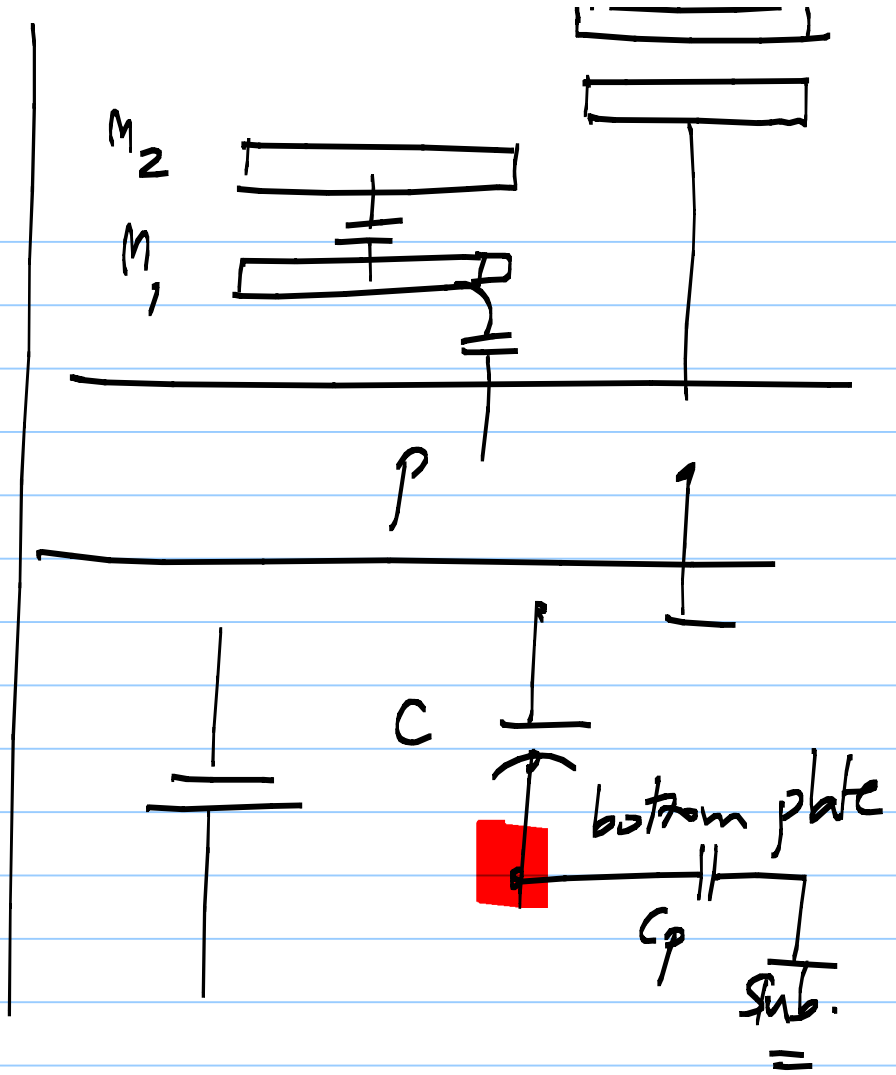


Random mismatch

$$\sigma\left(\frac{\Delta C}{C_0}\right) = \frac{A_c}{\sqrt{WL}}$$

mean

deviation from the mean

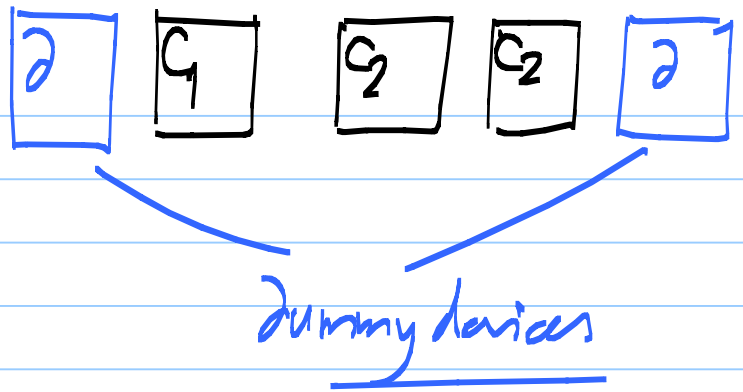


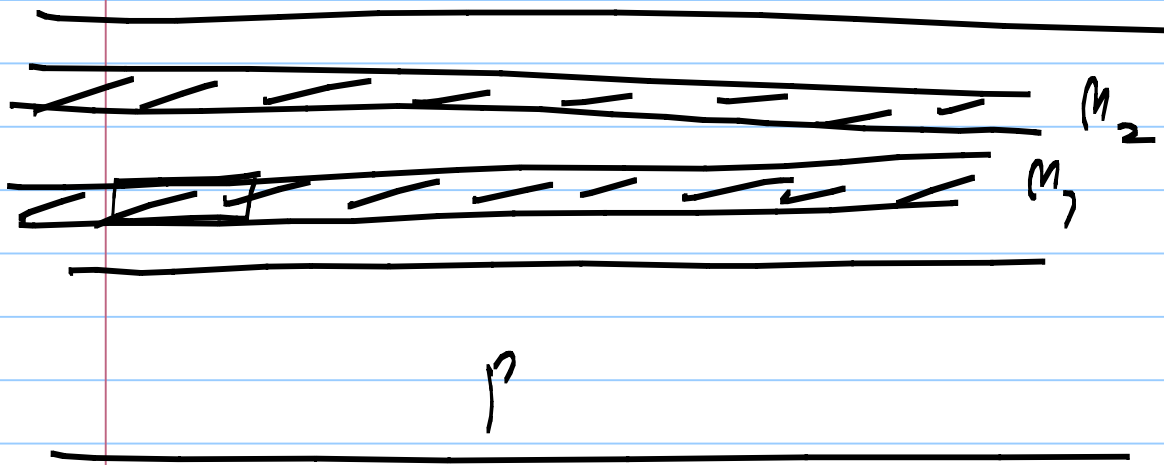
$$\frac{C}{C+C_p}$$

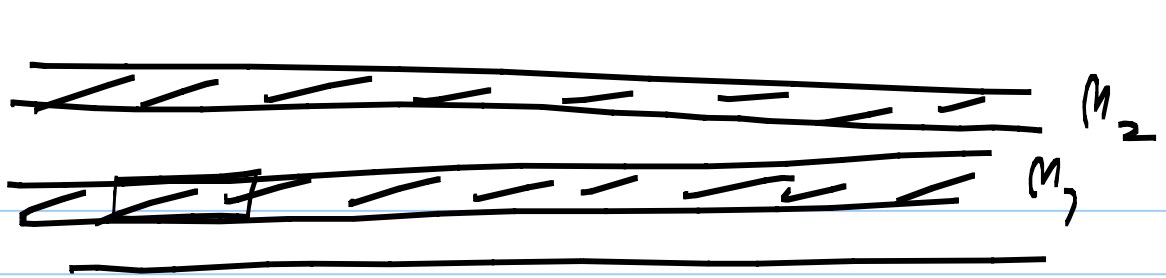
Systematic mismatch.

* Use unit elements

* Use dummy devices





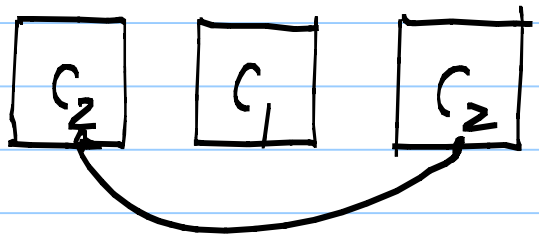


Layout cumbersome

P

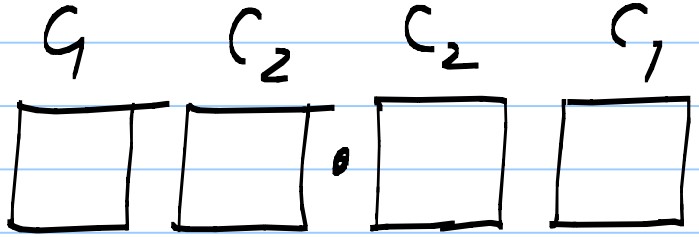
$1+\delta$

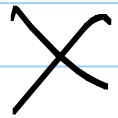
$\simeq 1-\delta$



$C_1 = C_0$

$C_2 = 2C_0 + 3\Delta C$

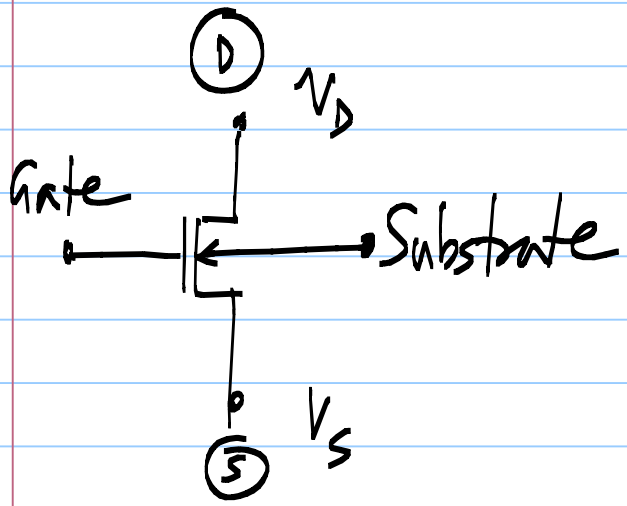


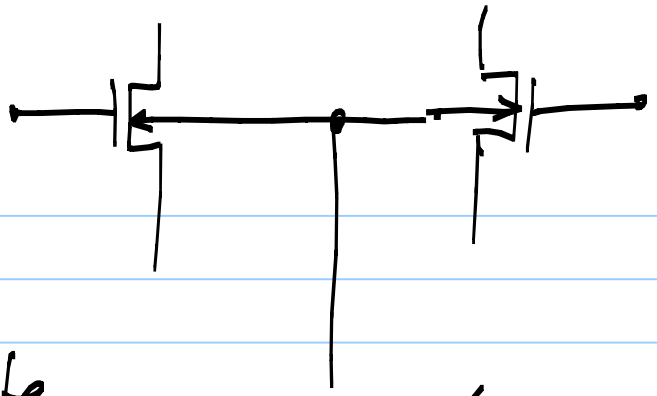


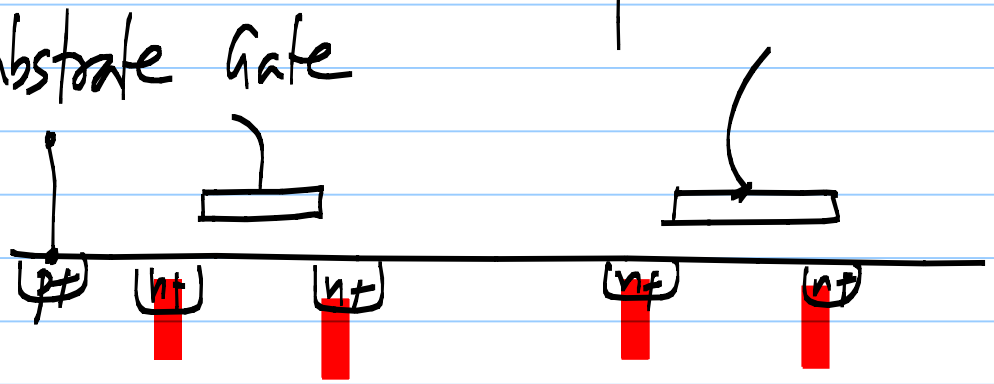
Common centroid layout

M2
M1
M1
M2

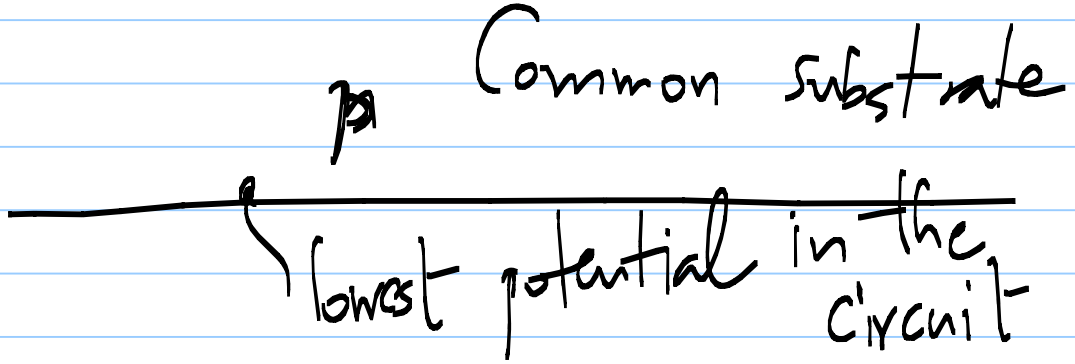
Mos transistor

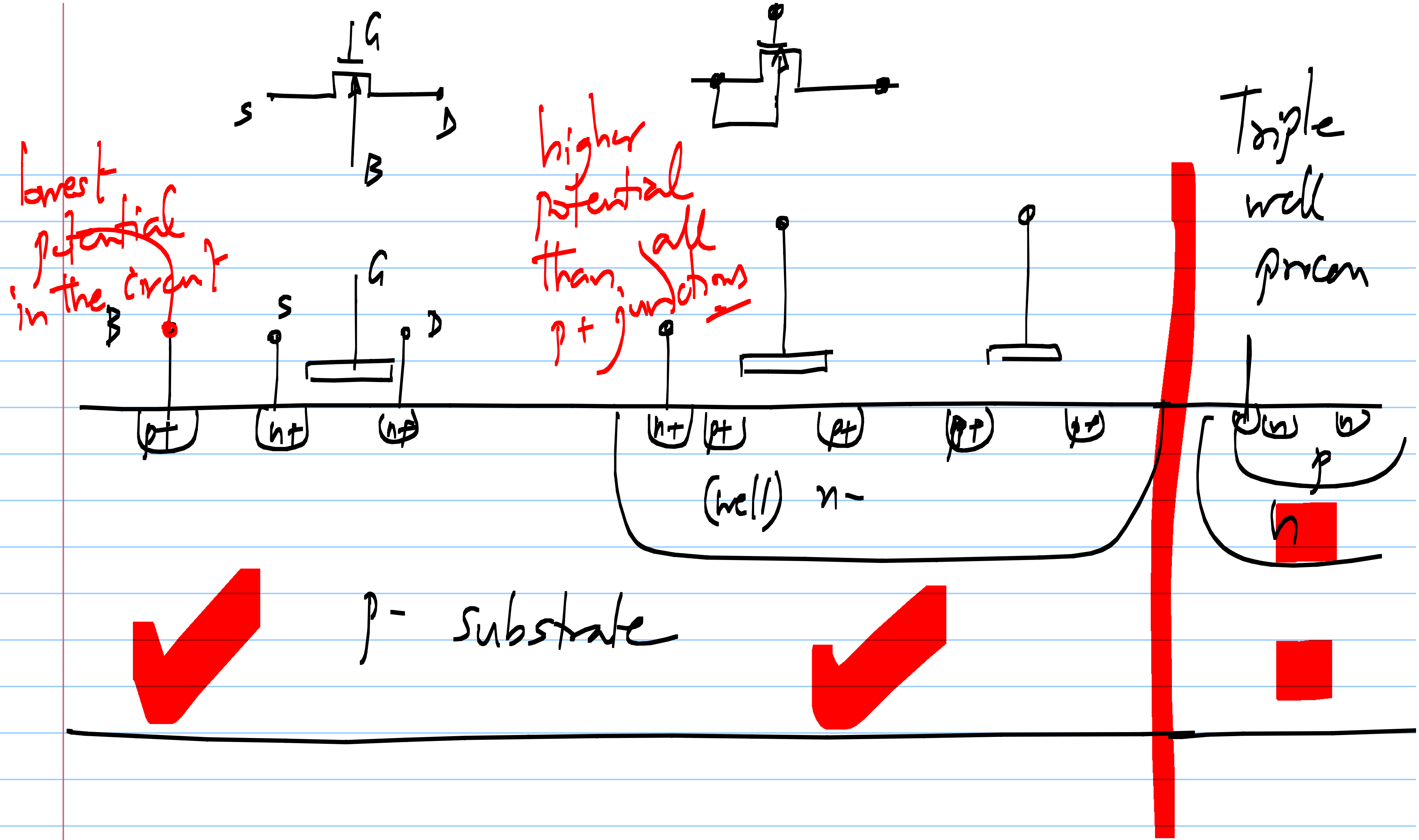






$V_D > V_S$





G
S
D
B
lowest potential in the circuit
B
S
G
D
p+
n+
n+
higher potential than all p+ junctions
n+
p+
p+
p+
p+
(well) n−
p− substrate
Triple well process
n
n
p
n