

EE539: Analog Integrated Circuit Design; HW8

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0.18 μm technology parameters: $V_{Tn} = 0.5\text{ V}$; $V_{Tp} = 0.5\text{ V}$; $K_n = 300\ \mu\text{A}/\text{V}^2$; $K_p = 75\ \mu\text{A}/\text{V}^2$; $A_{VT} = 3.5\text{ mV}/\mu\text{m}$; $A_\beta = 1\%$; $V_{dd} = 1.8\text{ V}$; $L_{min} = 0.18\ \mu\text{m}$, $W_{min} = 0.24\ \mu\text{m}$; Ignore body effect unless mentioned otherwise. Ignore $1/f$ noise unless mentioned otherwise.

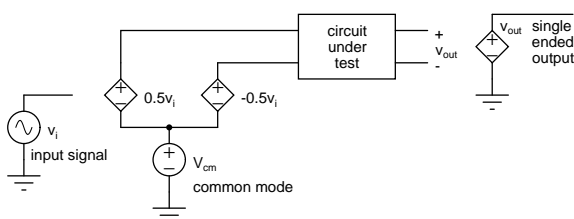


Figure 1: Test bench for differential circuits

Simulating fully differential circuits: For testing differential circuits, the circuit in Fig. 1 can be used to preserve symmetry and avoid errors (such as not driving the inputs symmetrically). v_i can be the desired signal (ac, dc, or transient). When v_i is the input source for noise analysis, the input referred noise refers to the differential input.

A similar test bench can be created for common mode input/outputs by appropriately changing the controlled sources.

For differential opamps in this assignment, you should not have redesign anything. You only need to turn the opamps already designed in previous assignments to fully differential versions and add common mode feedback circuitry. Use $V_{cm} = 0.9\text{ V}$

Do not use an ideal current source in the tail. You can use one ideal reference current source of $1/10^{\text{th}}$ the tail current for bias generation.

1. **Two stage opamp:** Design a two stage single ended opamp (Fig. 2) that has a dc gain of at least 500, and a

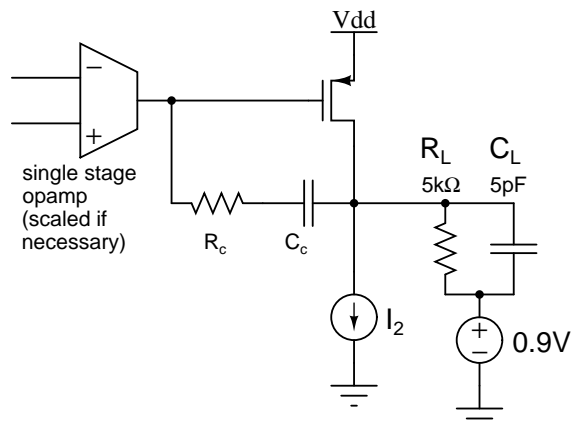


Figure 2: Two stage opamp

unity gain frequency of 100 MHz with a load of 5 pF and 5 k Ω in parallel. Design the second stage common source amplifier to have a sufficiently high dc gain while driving the desired load resistance and a sufficiently high second pole while driving the desired load capacitance. Use a scaled version¹ of your single stage opamp design from above for the input stage. Use a suitable compensation capacitor (Fig. 2). All parasitic poles and zeros should be at at least twice the unity gain frequency. Ensure that there is no systematic offset because of the second stage bias. Add a zero canceling resistor.

Report (a) through (j) above. Along with the open loop frequency response, plot the frequency response from the input to the first stage output.

2. **Fully differential folded cascode opamp:** Turn the folded cascode opamp designed in the previous assignment to a fully differential version. Use the circuit in Fig. 4 for common mode feedback. Use the

¹ You should not have to redesign this stage

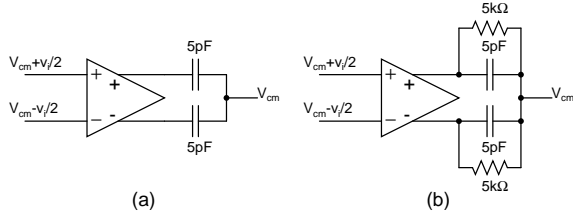


Figure 3: Test circuit for the two opamps

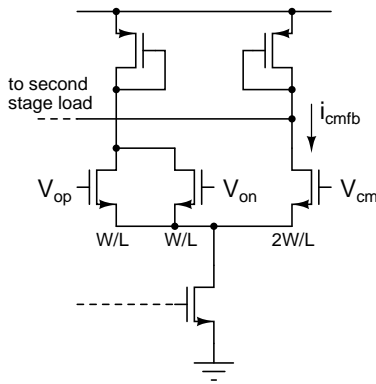


Figure 4: Common mode feedback structure for the folded cascode opamp

same type of differential pair (nMOS or pMOS) as at the input of your opamp, and the same tail current as in the input stage. Size the load devices of Fig. 4 to have the same current density as in the corresponding transistors in the opamp.

Report the following and show simulation results where appropriate. Tabulate the results neatly as in a data sheet.

- Input common mode range
- Output voltage range
- A_o , ω_u , and open loop poles/zeros
- Input referred noise spectral density-identify $1/f$ noise corner if applicable. Show relative contributions from different devices at 10 MHz.
- Input referred offset (For this, ignore current factor mismatch; Calculate σ_{VT} from the sizes, and use g_m values from the operating point; You can assume $g_m \gg g_{ds}$)
- Common mode response: Inject a common mode step of $1 \mu\text{A}$ to the output with the in-

put nodes held at V_{cm} . Plot the output common mode response.

- Power consumption
- Show a schematic with all sizes and operating points (g_m , g_{ds} , $V_{GS}-V_T$, I_D) of all transistors and the node voltages.

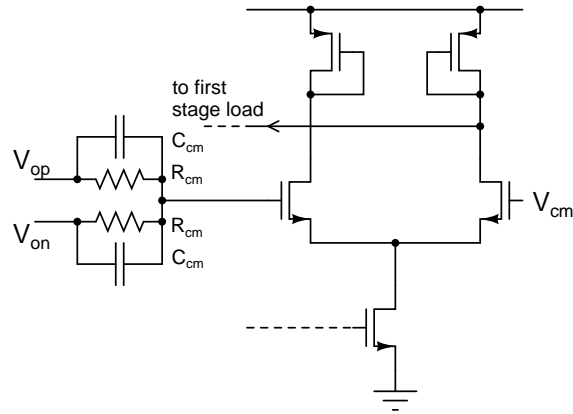


Figure 5: Common mode feedback structure for the two stage opamp

- Fully differential two stage opamp:** Turn the two stage opamp designed in the previous assignment into a fully differential version. Use the circuit in Fig. 5 for common mode feedback. Report (a) through (h) above.
- Bandgap reference:** Bias a 1x sized diode connected PNP² at $10 \mu\text{A}$ as shown in Fig. 6(a) and sweep the temperature from 0 to 100°C . Determine dV_{BE}/dT at 27°C .

Design the bandgap shown in Fig. 6(c). Choose R_1 for a quiescent current of $10 \mu\text{A}$ and R_2 to get zero temperature coefficient at V_{bg} . Choose $R_3 = R_2$. What is the role of R_3 ? Simulate the bandgap reference with the model of a single stage opamp designed in the previous assignment (Fig. 6(b)-model the g_m , and the pole zero doublet). Choose C_c for ringing $\leq 10\%$. Test the bandgap reference by sweeping the temperature from 0 to 100°C and plot V_{bg} . Test the transient response by applying a $1 \mu\text{A}$

²Use the model `ideal_pnp` in `ideal_diode.lib`

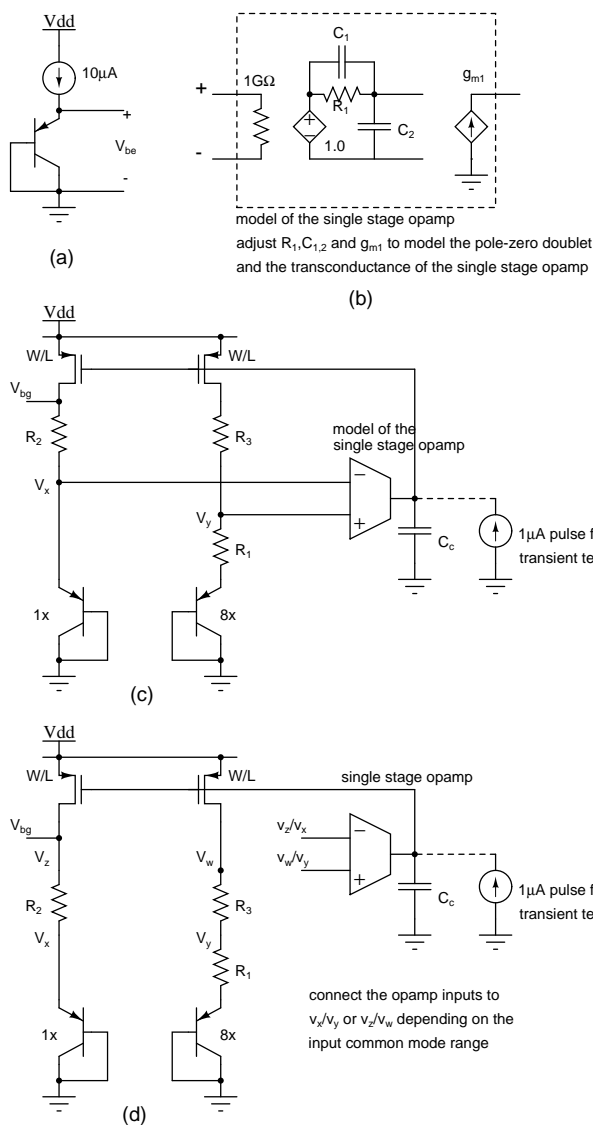


Figure 6: Bandgap reference

pulse to the output of the opamp. Adjust the values of R_1 , R_2 , $R_3 (= R_2)$ if necessary to get zero TC at 27°C .

Modify the circuit as in Fig. 6(d). How should V_x , V_y , and V_{bg} change? What is the purpose of this modification? Resimulate with the opamp model as before and test the temperature sensitivity, transient response and the loop gain.

Substitute the differential pair opamp designed in the previous assignment and simulate the temperature sensitivity of V_{bg} and the transient response to a current step at the output.

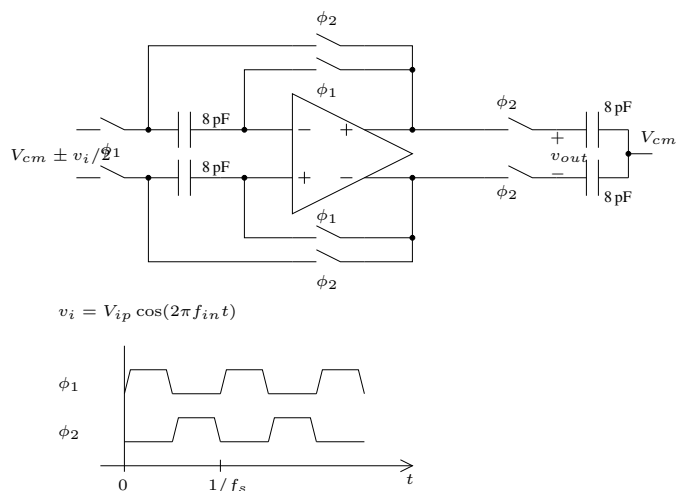


Figure 7: Sample and hold circuit

Opamp applications: Do any one of the following problems. You'll get bonus credit for doing both.

1. **Sample and hold:** Design the sample and hold circuit in Fig. 7 using the fully differential folded cascode opamp designed above. Use ideal switches with $1\text{ k}\Omega$ on resistance. Use $f_s = 4\text{ MHz}$ and $f_{in} = \{1/4, 9/4\}\text{ MHz}$ (sinusoidal input with 1.6 Vppd^3 amplitude) and plot the output waveforms. Provide a plot that shows the settling behavior of the opamp.
2. **Inverting amplifier:** Design the inverting amplifier in Fig. 8 using the fully differential two stage amplifier designed above. Show the output waveforms for a 1 V differential step and a 0.5 V common mode step.

³Vppd: volts, peak-peak differential

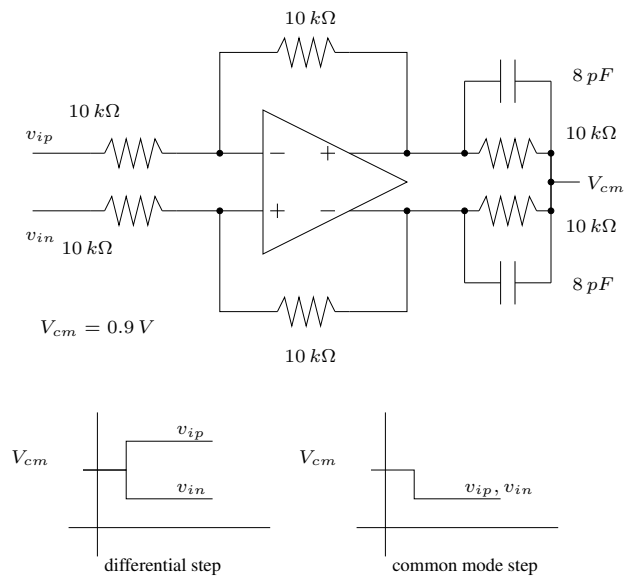


Figure 8: Inverting amplifier