EE539: Analog Integrated Circuit Design; Common mode feedback circuits

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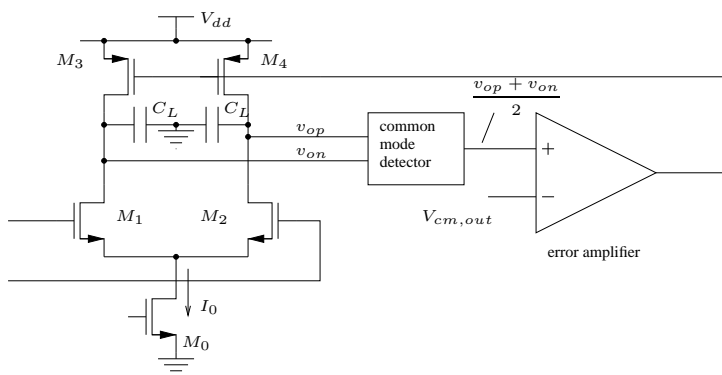

Figure 1: Principle of common mode feedback

- Adjust top current sources $(M_{3,4})$ via feedback to control the bottom current source (M_0).

- Detected common mode voltage equals $V_{cm,out}$ in steady state-assuming a large loop gain.
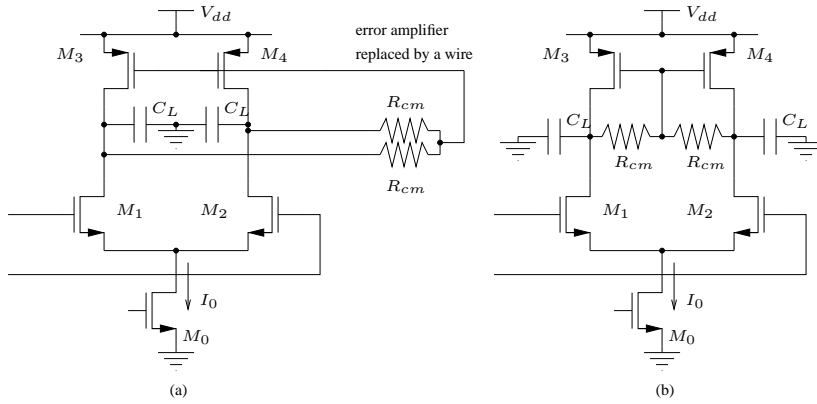
Figure 2: (a) CMFB circuit using common mode diode connection, (b) redrawn

- *Common mode diode connection*: output voltage adjusts itself to ensure that $I_3 + I_4 = I_0$.

- Resulting common mode equals $v_{cm,out} = V_{dd} - V_T - \sqrt{I_0/K_3}$. Cannot be set independently of device parameters

- Largest positive output swing $= V_T$, implying a largest differential peak-peak swing of $4V_T$, independent of the supply voltage.

- Common mode detector using resistors: loads the differential amplifier and reduces the gain.
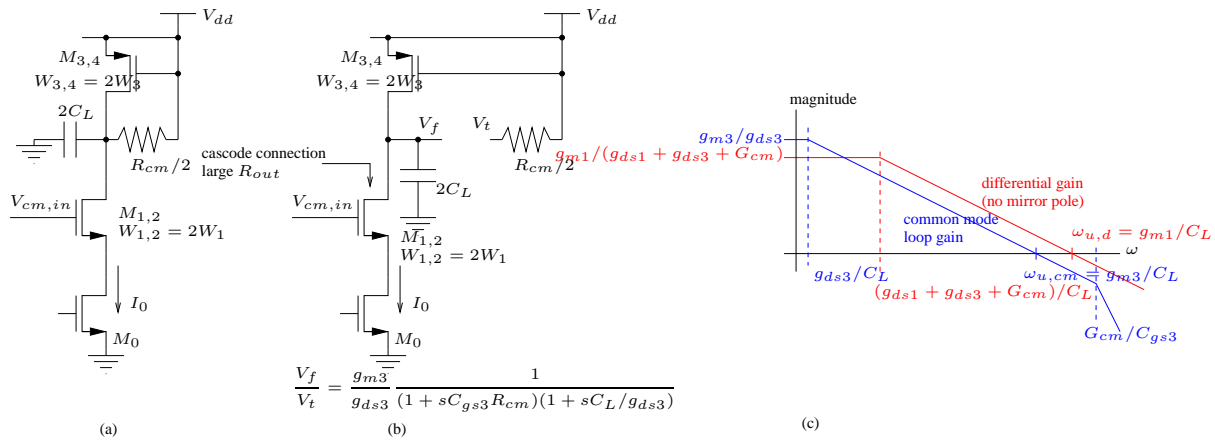
Figure 3: (a) Common mode equivalent ckt., (b) CMFB loop gain calculation, (c) Typical differential gain and CM loop gain magnitudes

- CMFB loop gain: Dominant pole at the output

- Second pole significant if a large R_{cm} is used

- Feedback around a single transistor $(M_{3,4})$. Typically stable.

- No mirror pole in the fully differential amplifier's response

$I_{10} = I_0/\alpha$
$W_{10} = W_0/\alpha$
$W_{11} = W_1/\alpha$
$W_{13} = W_3/\alpha$
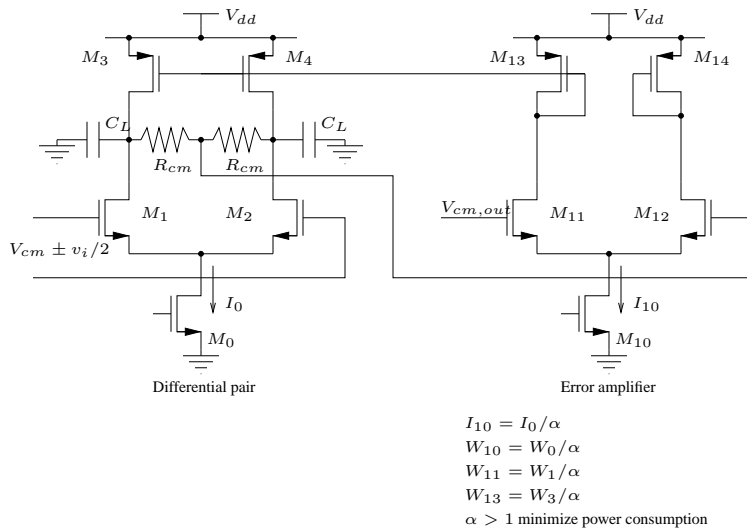$\alpha > 1$ minimize power consumption

Figure 4: CMFB circuit with explicit error amplifier

- A second differential amplifier used as an error amplifier. Its output current is mirrored to the opamp's load devices (M_3, M_4)

- To have no systematic error in the output CM voltage, aspect ratios of $M_{3,4,13,14}$ are in ratios of respective currents. i.e. without mismatches, the error amplifier operates with zero input voltage

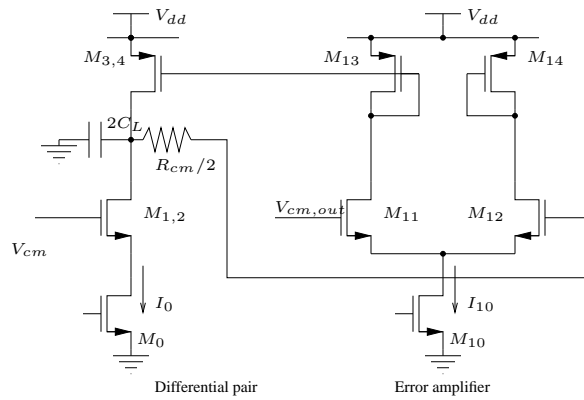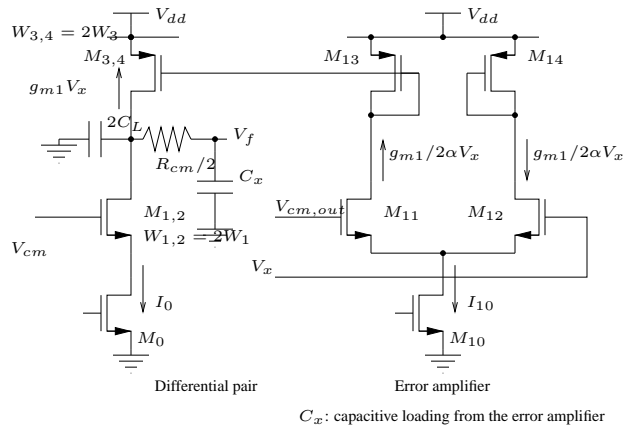- Error amplifier current can be scaled down to minimize power consumption.

Figure 5: CM equivalent

C_x: capacitive loading from the error amplifier

$$\frac{V_f}{V_t} = \frac{g_{m1}}{2g_{ds3}} \frac{1}{1 + sg_{ds3}/C_L} \frac{1}{1 + sC_x R_{cm}} \frac{1}{1 + sg_{m3}/\alpha C_{p3}}$$

(Assumed that $R_{cm}C_x << C_L/g_{ds3}$; C_{p3} is the parasitic capacitance at the drain of M_{13}

Figure 6: CMFB loop gain calculation

- Differential response: Single pole at the output.

- CMFB loop gain: Three poles; Approx. two poles with a small R_{cm}; Dominant pole at the output. C_L compensates both the common mode and differential loops.

- Using a large α (small current in the error amplifier) results in a lower frequency non dominant pole in CMFB loop gain.

$I_{10} = I_0/\alpha$
$W_{10} = W_0/\alpha$
$W_{11} = W_1/\alpha$
$W_{12} = W_{11}/2$
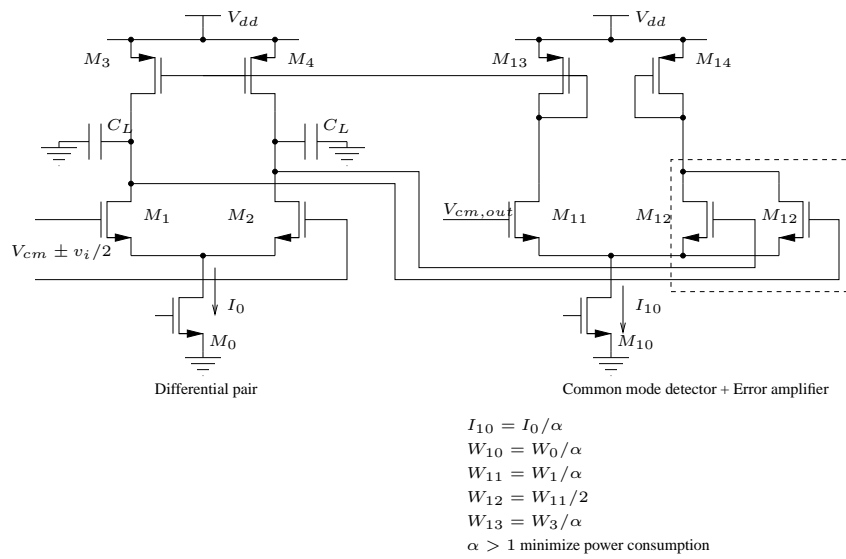$W_{13} = W_3/\alpha$
$\alpha > 1$ minimize power consumption

Figure 7: CMFB circuit using differential pair CM detector

- Split the transistor in the error amplifier differential pair into two halves and apply v_{op}, v_{on} to their gates. Current summation ensures common mode detection.

- Active CM detector does not load the opamp.

- Resistive CM detector: highly linear

- Active CM detector: Linearity, and consequently, the swing of the output signals, depends on the linearity of the error amplifier differential pair
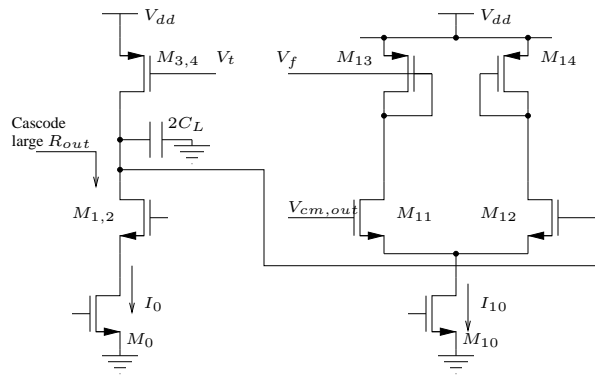
Figure 8: CMFB loop gain calculation using the common mode equivalent circuit

- Two pole response

$$\frac{V_f}{V_t} = \frac{g_{m3}}{g_{ds3}} \frac{g_{m11}}{2g_{m14}} \frac{1}{1 + sC_L/g_{ds3}} \frac{1}{1 + sC_x/g_{m14}}$$

- Non dominant pole g_{m14}/C_x moves to lower frequencies if a very small current is used in the error amplifier.
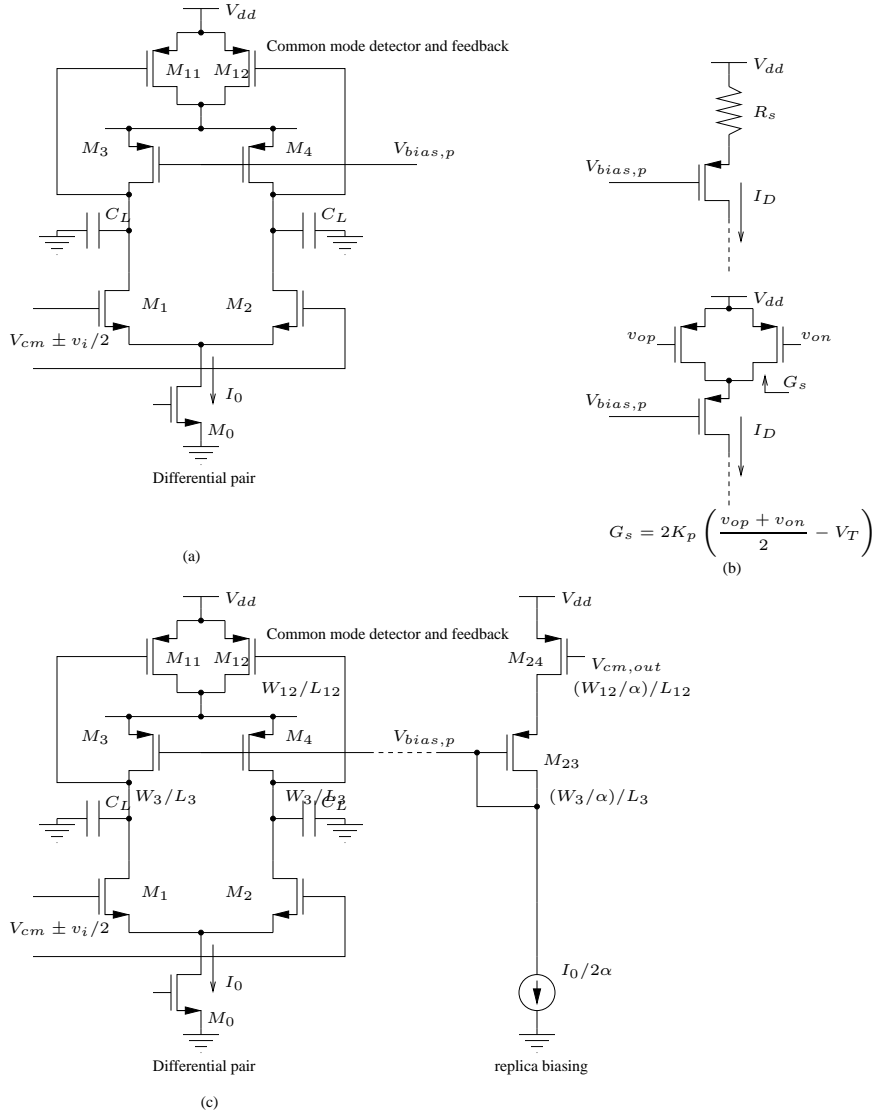
Figure 9: (a) Common mode feedback using transistors in triode region, (b) Degenerated resistor, Degeneration using MOS transistors whose resistance depends on the common mode voltage, (c) Replica biasing to set the output common mode voltage

- Parallel transistors in triode region with v_{op}, v_{on} as inputs realize a conductance as a function of the common mode

- Replica biasing with the gate of M_{24} at the desired common mode level

- Upper limit of v_{op}, v_{on} is $V_{dd} - V_T$. $M_{13,14}$ go into saturation region at a voltage slightly below this.
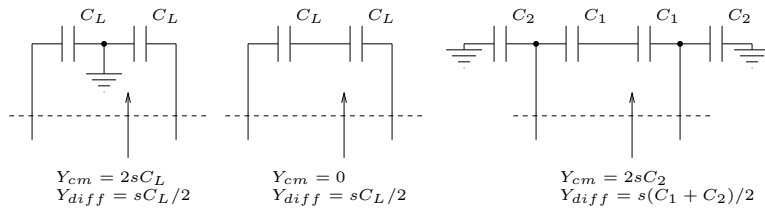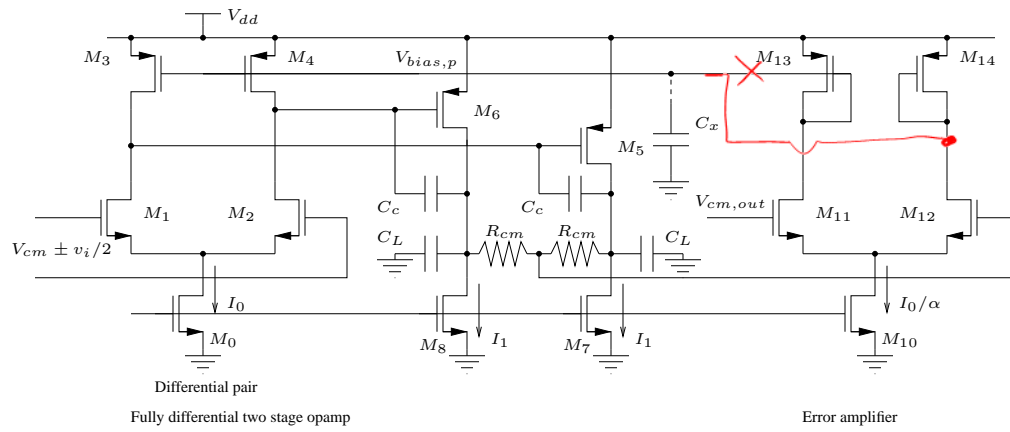
Figure 10: Differential and common mode loading

- Floating capacitors don't contribute to common mode loading

- There should be suffi cient common mode loading to compensate the CMFB loop

Figure 11: Two stage opamp with common mode feedback

- Output common mode voltage is measured and common mode feedback applied to the first stage load.

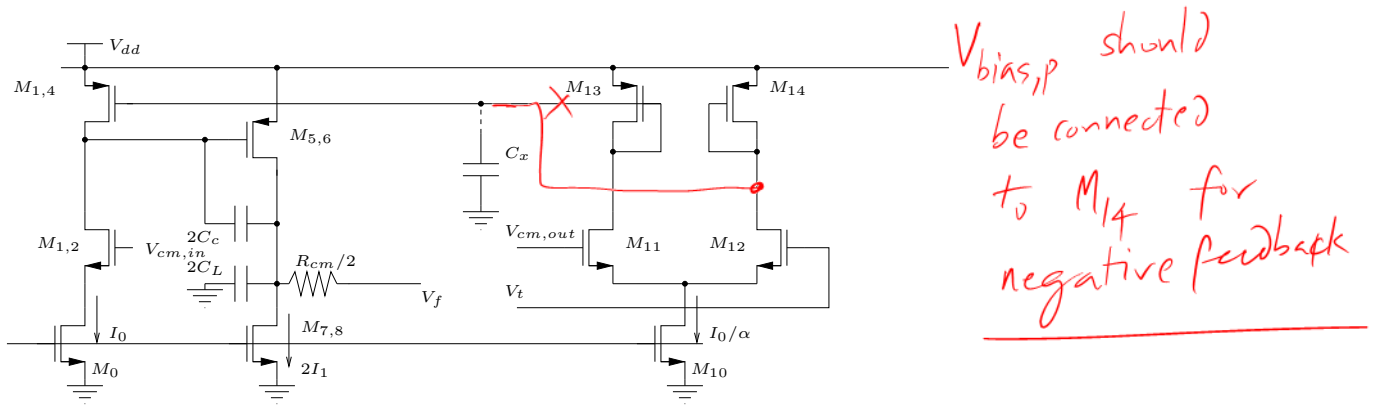- Can use separate common mode feedback for each stage

Figure 12: Common mode equivalent circuit of the two stage opamp

- Common mode feedback: Negative feedback around two stages

- Compensation through C_c

- Differential response

$$A_d(s) = \frac{g_{m1}}{g_{ds1} + g_{ds3}} \frac{g_{m5}}{g_{ds5} + g_{ds6} + G_{cm}} \frac{1 - sC_c/g_{m5}}{(1 + s/p_1)(1 + s/p_2)}$$

$$p_1 \approx \frac{g_{ds3}}{C_3 + C_c(1 + g_{m5}/g_{ds5})}$$

$$p_2 \approx \frac{g_{m5}\frac{C_c}{C_c + C_3}}{C_L + \frac{C_c C_L}{C_c + C_L}}$$

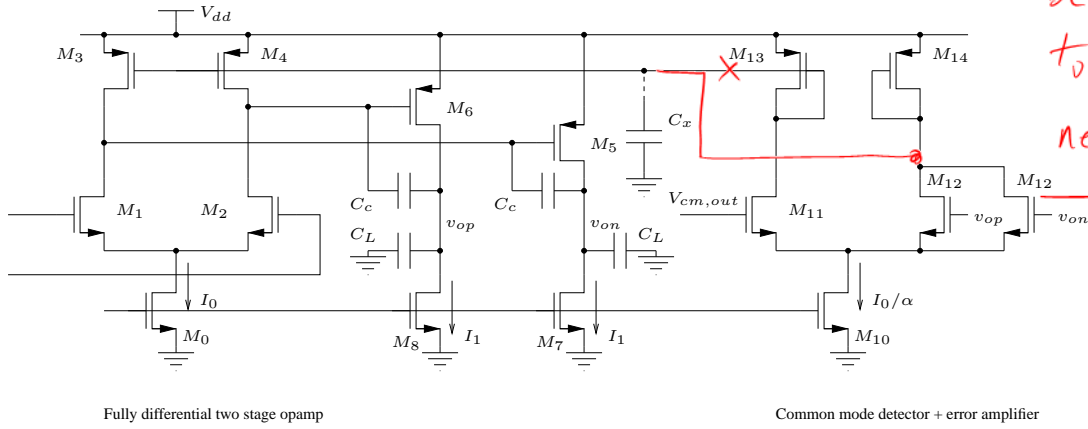C_3 is the parasitic capacitance at the drain of M_3.

- Common mode loop gain

$$A_{cmloop}(s) = \frac{g_{m3}}{g_{ds3}} \frac{g_{m5}}{g_{ds5} + g_{ds6}} \frac{g_{m11}}{2g_{m13}} \frac{1 - sC_c/g_{m5}}{(1 + s/p_1)(1 + s/p_2)(1 + s/p_3)}$$

$$p_1 \approx \frac{g_{ds3}}{C_3 + C_c(1 + g_{m5}/g_{ds5})}$$

$$p_2 \approx \frac{g_{m5}\frac{C_c}{C_c + C_3}}{C_L + \frac{C_c C_3}{C_c + C_3}}$$

$$p_3 = \frac{g_{m13}}{C_x}$$

Figure 13: Two stage fully differential opamp with split transistor common mode detector
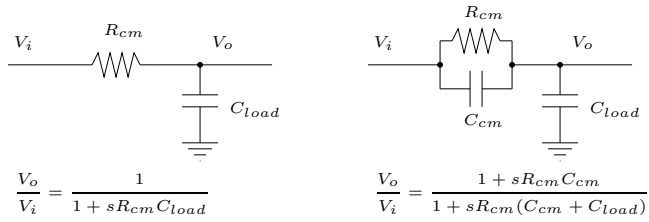
Figure 14: (a) Resistive common mode detector, (b) Introducing a zero to reduce phase lag

- To minimize loading, increase R_{cm}.

- R_{cm} with parasitic capacitance at the input of the error amplifier adds phase lag and degrades stability.

- Use a capacitor across R_{cm} to introduce phase lead and ensure stability of the common mode feedback loop.
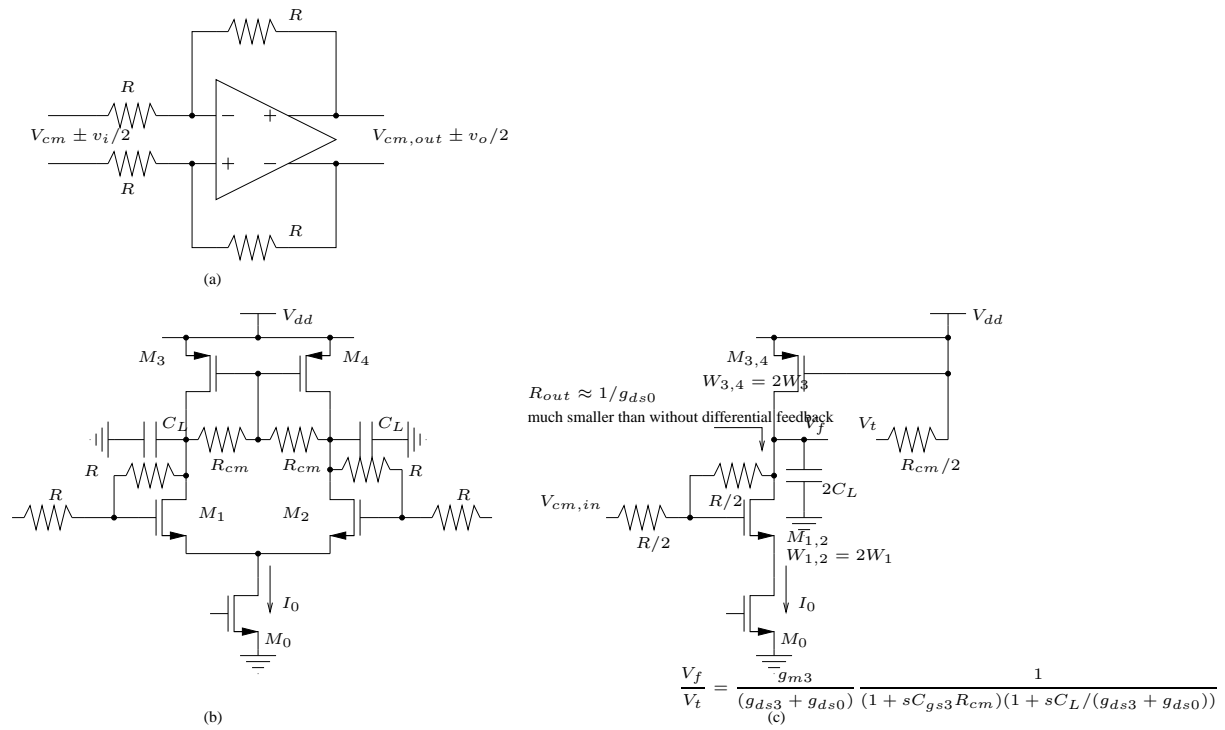
Figure 15: (a) Opamp with differential feedback, (b) Transistor level circuit, (c) Common mode equivalent circuit

- Differential feedback can change CMFB loop gain.

- CM loop gain needs to be evaluated with differential feedback in place.