EE539: Analog Integrated Circuit Design;

Nagendra Krishnapura (nagendra@iitm.ac.in)

07 April 2006

1 FREQUENCY RESPONSE OF TWO STAGE OPAMP

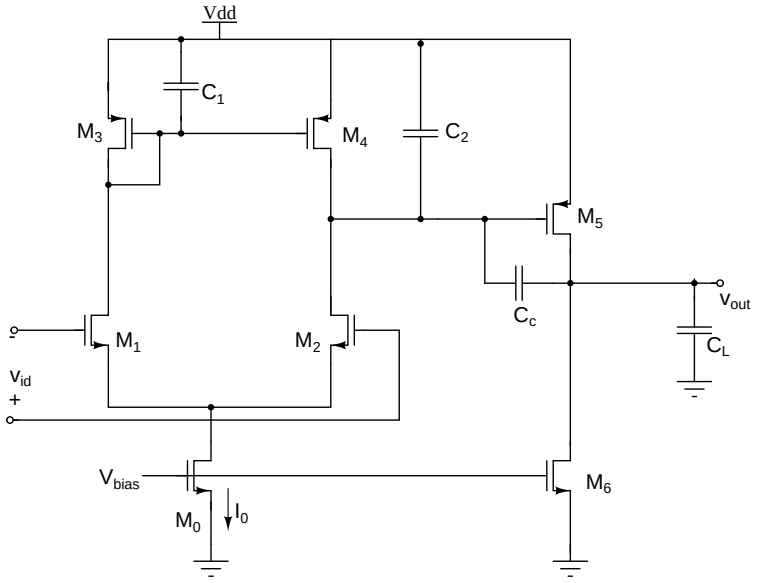

Figure 1: Two stage opamp

$$A_{dc} = \frac{g_{m1}}{g_{ds1}+g_{ds3}} . \frac{g_{m5}}{g_{ds5}+g_{ds6}+G_L} = \frac{g_{m1}}{G_1} . \frac{g_{m5}}{G_L}$$

$$P_1 = -\frac{G_1}{C_2 + (1+\frac{g_{m5}}{G_L})C_c}$$

$$P_2 = -\frac{g_{m5} \cdot \frac{C_c}{C_c+C_2}}{C_L + \frac{C_c . C_2}{C_c+C_2}} \approx \frac{g_{m5}}{C_L}$$

$$Z_1 = \frac{g_{m5}}{C_c}$$

$$Z_2 = -\frac{2g_{m3}}{C_1}$$

$$P_3 = -\frac{g_{m3}}{C_1}$$

$$w_u = -\frac{g_{m1}}{C_c}$$

1.1 DESIGN OF TWO STAGE OPAMP

Given G_L, A_{dc}, C_L, w_u

•Choose g_{m5}, I_5,C_c : $\frac{g_{m5}}{C_L} > w_u$

•Choose g_{m1} : small I_0 and, large W_1 but considering phase margin(PM) requirements.

Due to this Z_2, P_3 moves to lower frequencies.

•To improve phase margin(PM),introduce compensation resistor R_c as shown in fig(1).

Now

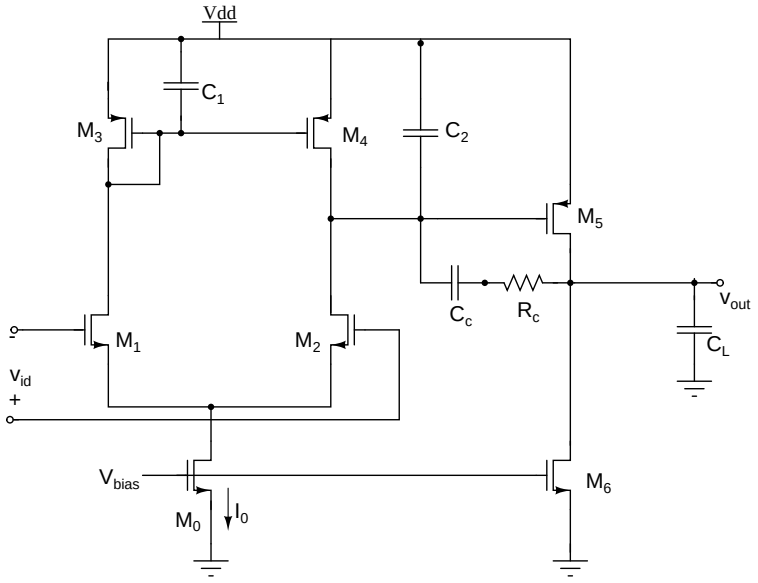

Figure 2: Two stage opamp

$$Z_1^{'} = \frac{g_{m5}}{C_c(1 - g_{m5}R_c)} = -\frac{1}{C_c(\frac{1}{g_{m5}} - R_c)}$$

•If $R_c = \frac{1}{g_{m5}}$,then $Z_1^{'}$ moves to ∞,and improves PM.

•If $R_c > \frac{1}{g_{m5}}$,further improvement in PM, since zero moves left half plane and cancels left half plane pole.

•But the problem here is R_c must be able to track g_{m5}

2 SLEW RATE OF TWO STAGE OPAMP

2.1 Positive slew rate

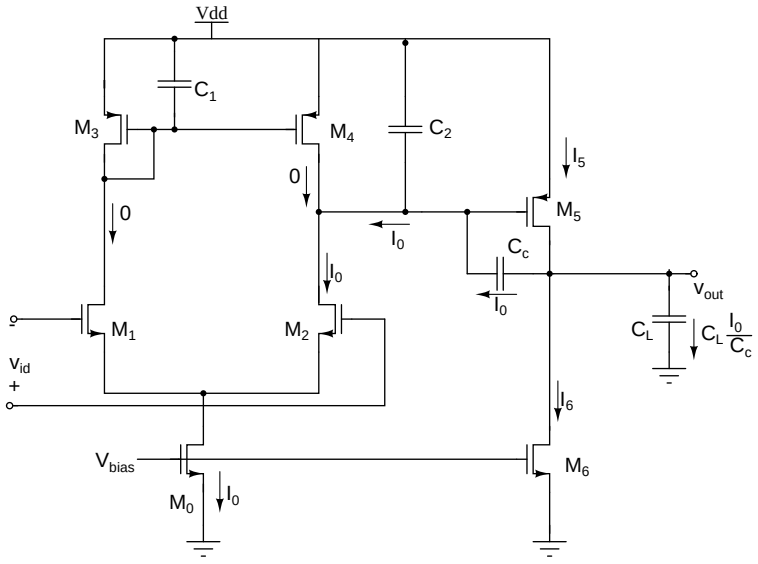

Figure 3: Two stage opamp

If we apply large positive voltage at input as shown in figure(3),then

$$SR_+ = \frac{I_0}{C_c}$$

This is correct if we assume that gate of M_5 can go low enough to support a current $I_0(1 + C_L C_c) + I_6$

2.2 Negative slew rate

If we apply large negative voltage at input as shown in figure(4),then

- $$SR_- = \frac{I_0}{C_c}$$

This is correct if we assume that $I_5 > I_0(1 + C_L C_c)$

- $$SR_- = \frac{I_0}{C_c + C_L}$$

This is correct if we assume that $I_5 < I_0(1 + C_L C_c)$

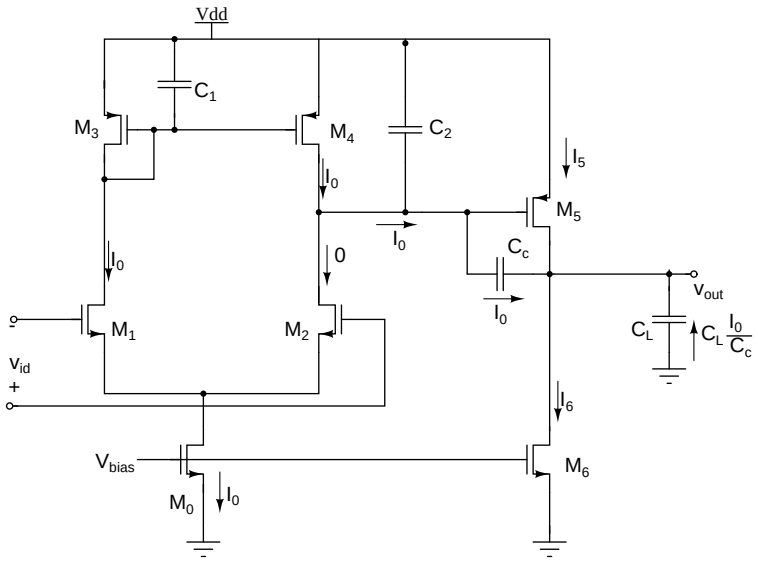

Figure 4: Two stage opamp