EE539: Analog Integrated Circuit Design; Lecture 1

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1 2-Stage op-amp

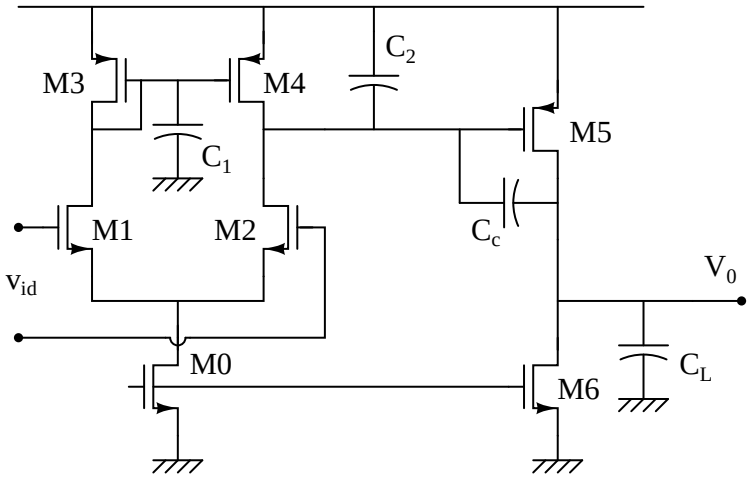

Figure 1: 2-stage Op-amp

$$A_{dc} = \frac{g_{m1}}{g_{ds1}+g_{ds3}}\frac{g_{m5}}{G_L} \qquad G_L = g_{ds1} + g_{ds3} + Load$$

$$z_1 = \frac{-g_{m5}}{C_c} \qquad p_2 = \frac{g_{m5}\frac{C_c}{C_c+C_2}}{C_L + \frac{C_c}{C_c+C_2}}$$

$$p_1 = -\frac{G_1}{C_c + (1+\frac{G_{m5}}{G_L})C_2}$$

in a well designed op-amp assume d.c gain*$p_1 = \omega_u$ (less than P_2).

$$A_{dc}p_1 = \frac{g_{m1}}{c_2\frac{G_L}{g_{m5}} + C_c(1+\frac{G_L}{g_{m5}})}$$

$$A_{dc}p_1 = \frac{g_{m1}}{C_c} = \omega_u$$

when we need to compensate, increase C_c such that ω_u is below the second pole;

$$z_2 = \frac{-2g_{m3}}{C_1} \qquad p_3 = \frac{g_{m3}}{C_1}$$

2

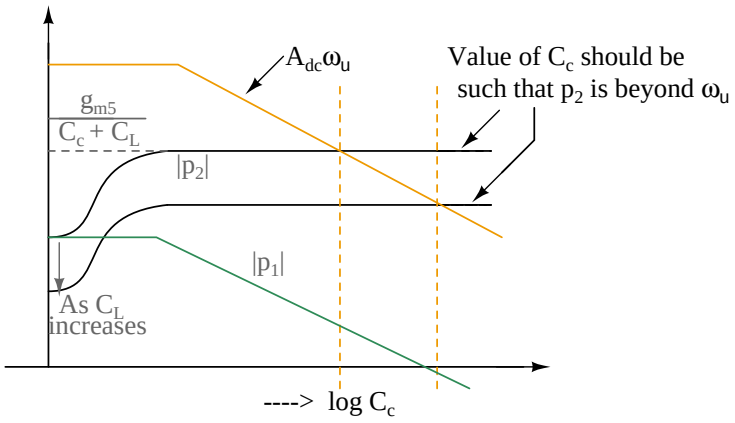

Figure 2: 2-stage Op-amp

if we increase C_L,

so the pole p_2 will come down, this deteriorates the phase margin.

$$\frac{g_{m5}}{C_c} < \frac{g_{m5}}{C_L + C_2}$$

the second pole should be away from ω_u.

for a given C_L, we design for g_{m5}

trade off between device size and current for g_{m5}.

3

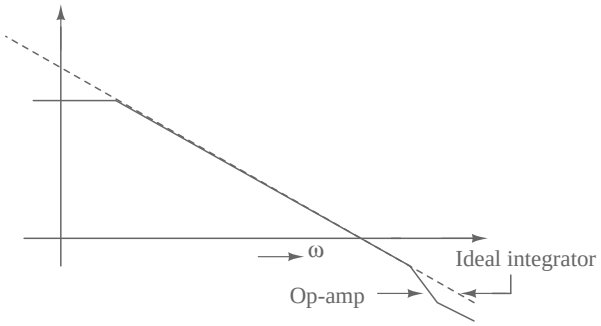

Figure 3: 2-stage Op-amp

what we want for an op-amp is ideally an integrator but we get other poles and zeros.