EE539: Analog Integrated Circuit Design;

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1 OUTPUT COMMON MODE FEEDBCK

To fix the output bias point, we can use the configuration shown in fig(1).

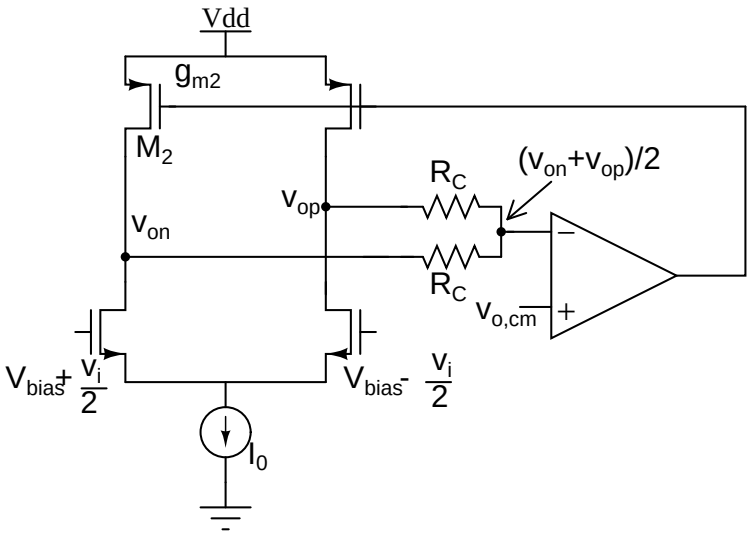

Figure 1: OUTPUT COMMON MODE FEEDBCK

If $\frac{V_{op}+V_{on}}{2} > V_{o,CM}$, then the gate voltage of M_2 increases such that the value of current flowing through the transistors remains constant and make the output voltage bias at $V_{o,CM}$
So,here we can connect $\frac{V_{op}+V_{on}}{2}$ directly to the gate of the transistor M_2.
Here the output bias point is

$$V_{o,CM} = V_{dd} - V_T + V_{Dsatp}$$

To find the common mode and differential mode loading,

$$R_{CM} = \frac{1}{g_m + g_{ds}}$$

$$R_{diff} = 2R_C || \frac{2}{g_{ds}}$$

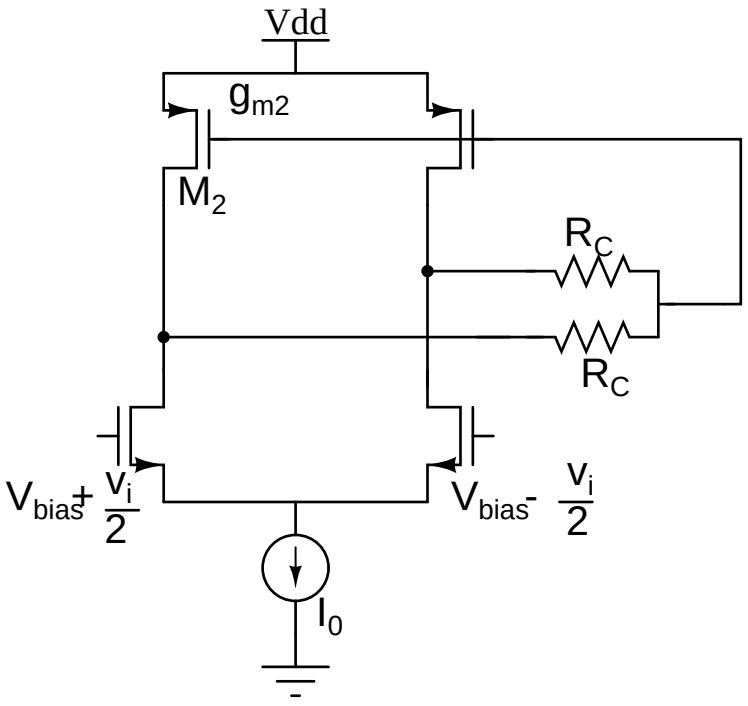

Figure 2: OUTPUT COMMON MODE FEEDBCK

If we observe the above two equations then,

$$R_{CM} \ll R_{diff}$$

That implies the configuration shown gives the fixed output bias point and very large gain.

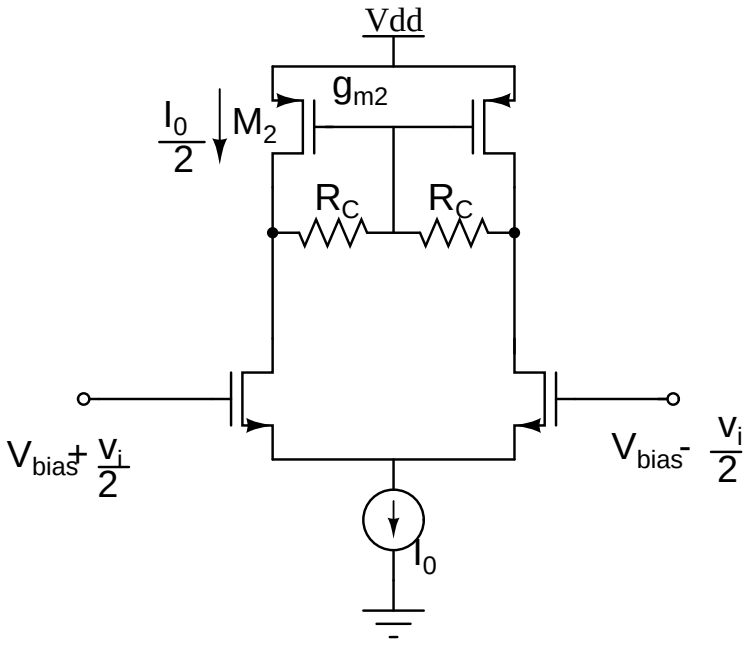

Figure 3: OUTPUT COMMON MODE FEEDBCK

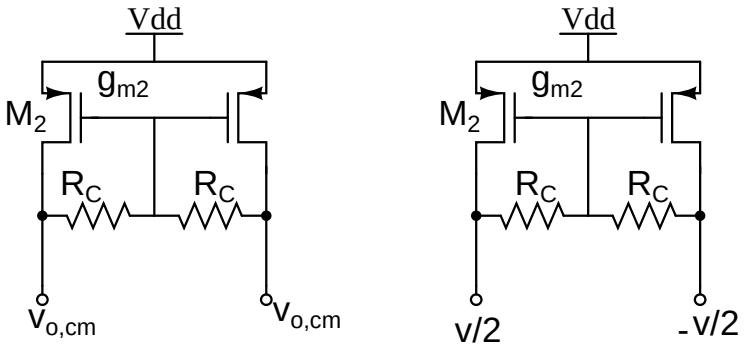

Figure 4: COMMON MODE AND DIFFERENTIAL LOADING

2 NEGATIVE FEEDBACK

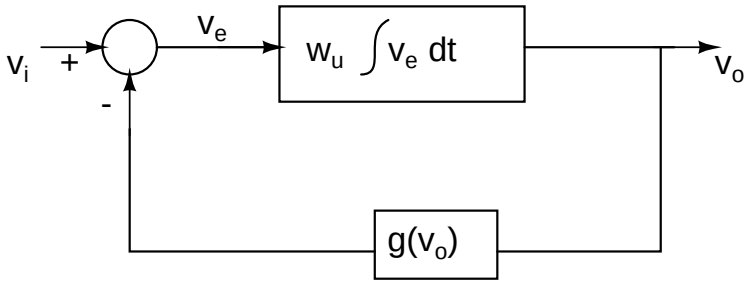

Figure 5: NEGATIVE FEEDBACK SCHEMATIC DIAGRAM

Stedy state integrator input(error) $= 0$

The frequency response of the integrator is shown in the below figure.

$$H(s) = \frac{w_u}{s}$$

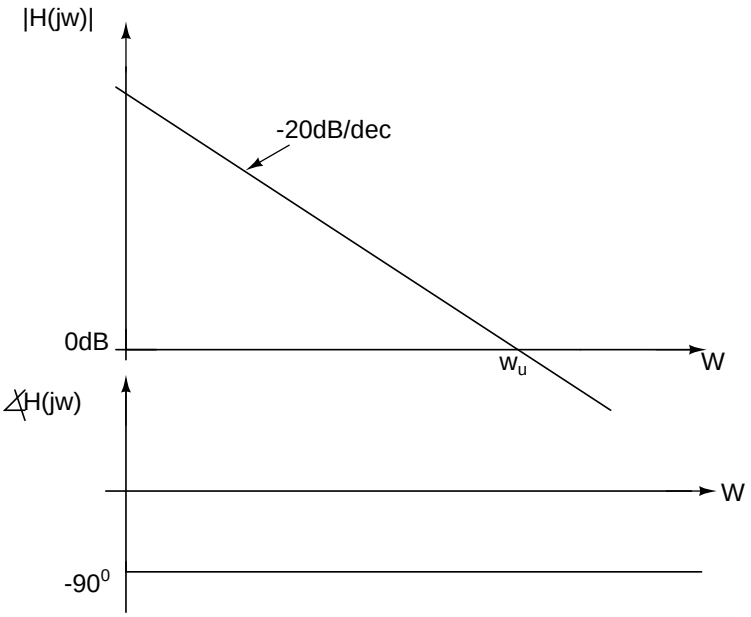

Figure 6: FREQUENCY RESPONSE OF THE INTEGRATOR