EE539: Analog Integrated Circuit Design; Lecture 1

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Current i can also be pushed in then upper limit of i is $|i| < I_0$ for both the transistors to be in saturation the limits on gate voltage V_G is given as

$$V_{Dsat0} + V_{Dsat1} + V_T < V_G < V_{DD} - I_0 R_L + V_T$$

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Figure 2:

for both the transistors to be in saturation the limits on gate voltage V_G is given as

$$V_{Dsat0} + V_{Dsat1} + V_T < V_{bias} + v < V_{DD} + V_T$$

But in practice the upper limit on V_{bias} + v is only V_{dd} . To get max. signal swing place V_{bias} at the middle.

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Figure 3:

differential input \Rightarrow differential output. it also gives flexibility in biasing the transistors.

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Figure 4:

To maximize gain $\uparrow g_m \Rightarrow \uparrow W$ or $\uparrow I_D$.

$$gm = \frac{2I_0}{V_{GS} - V_T}$$
$$|gain| = \frac{2I_0 R_L}{V_{GS} - V_T} = \frac{2V_R}{V_{GS} - V_T}$$

so to increase gain $\Rightarrow \uparrow V_R$ or $\downarrow V_{GS}$ - V_T but max. value of V_R is V_{dd} - V_{Dsat} . This is a certain limitation in increasing gain. We can increase gain by increasing bias size of transistors or R_L .

$$Actualgain = \frac{g_m}{G_L + g_{ds}}$$

To set $G_L = 0$ the load should be a current source.

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Figure 5:

small changes in I_1 causes large change in V_{DS} for a fixed V_G , adjust I_1 by feedback.

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Figure 6:

We can terminate load R not only to V_{dd} but also to any other V_{bias} . (The intersection of the load line and the I_D vs V_{DS} characteristics gives V_0) To change Bias point without changing the gain; change I_0

But I_D is very sensitive to variations in V_G ; so to get correct value of V_G a current mirror is used



Figure 7:

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Figure 8:

$$gain = \frac{g_m}{2} v_{id}$$

$$n_i = \frac{ng_m}{2} v_{id}$$

$$v_0 = \frac{ng_m}{2} v_{id} R_L$$

$$Totalgain = \frac{v_0}{v_{id}} = \frac{ng_m}{2} v_{id} R_L$$

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To get a gain of g_m / g_{ds}

The problem here is, the output bias point keeps changing we can also have a problem with mismatch.



Figure 9: