

DIFFERENTIAL AMPLIFIERS USING TRANSISTOR LOADS.

Nagendra Krishnapura (nagendra@iitm.ac.in)

28/2/06

DIFFERENTIAL AMPLIFIER USING NMOS LOAD.

- ➡ The advantage over resistive load is that gain is a ratio of like components, so the variations are less.
- ➡ The gain is $\frac{g_{m1}}{g_{m3}+g_{mbs3}}$.

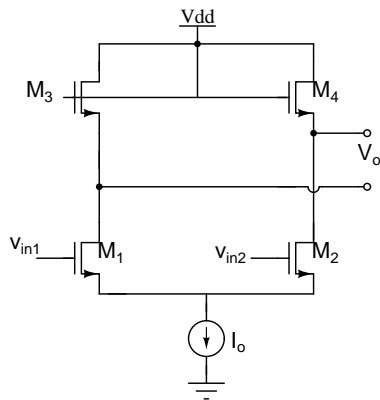


Figure 1: DIFFERENTIAL AMPLIFIER USING NMOS TRANSISTOR LOAD.

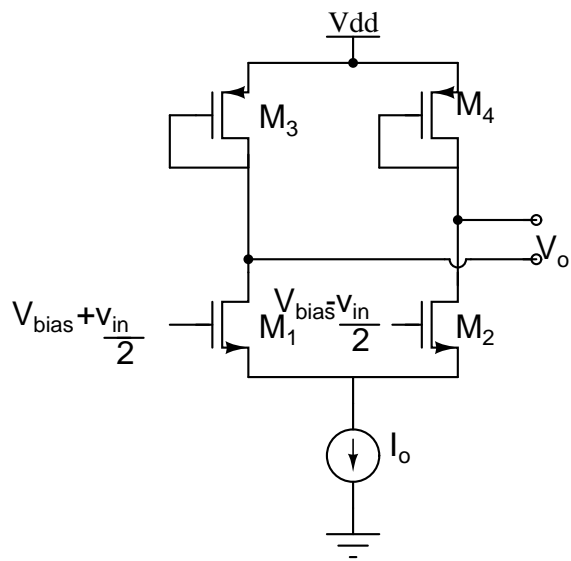


Figure 2: DIFFERENTIAL AMPLIFIER USING PMOS TRANSISTOR LOAD.

➡ To avoid the body effect we can use PMOS transistors. The gain is then

$$\frac{g_{m1}}{g_{m3}}$$

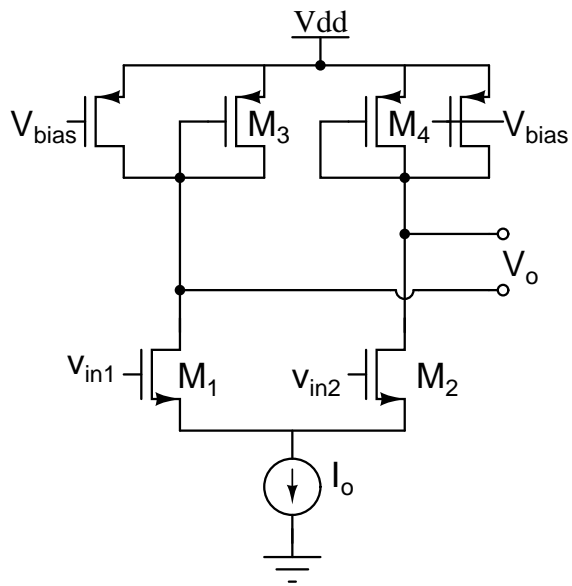


Figure 3: DIFFERENTIAL AMPLIFIER USING PMOS TRANSISTOR AND A PMOS CURRENT SOURCE AS LOAD.

- ✎ We can increase gain by reducing g_{m3} . This can be done by reducing the current through M_3 , so we connect a current source in parallel.

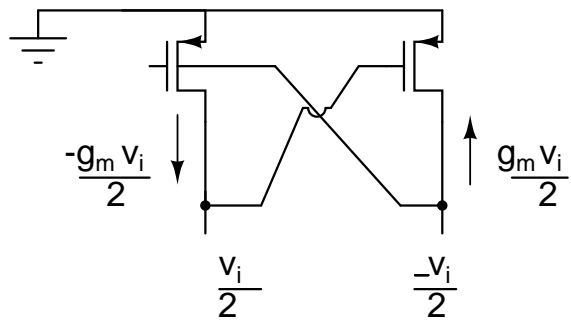


Figure 4: NEGATIVE RESISTANCE

- ➡ Another option to increase gain is by connecting negative resistance in parallel across the load.

Negative small signal resistance = $\frac{-2}{g_m}$

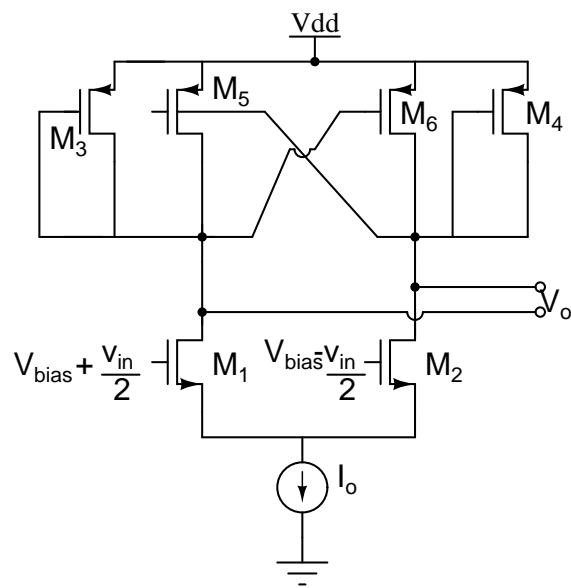


Figure 5: DIFFERENTIAL AMPLIFIER WITH NEGATIVE RESISTANCE IN PARALLEL AS LOAD

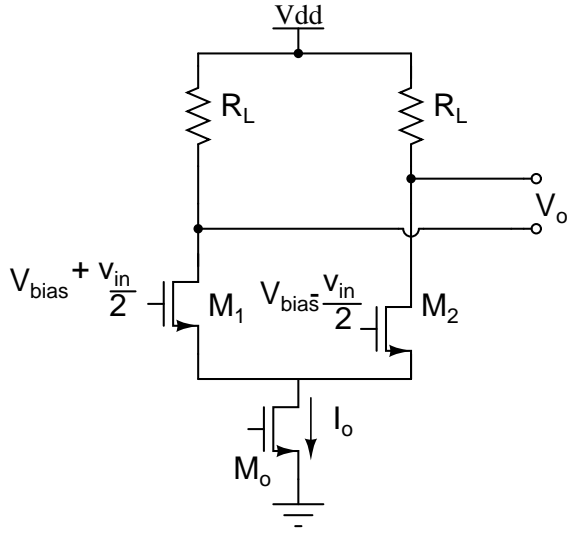


Figure 6: DIFFERENTIAL AMPLIFIER WITH RESISTANCE AS LOAD

✎ For a differential amplifier using R_L as load,

$$V_{bias} > V_T + \sqrt{\frac{2I_o}{\mu_n C_{ox} \frac{W}{L}}} + \sqrt{\frac{2I_o}{\mu_n C_{ox} \frac{W}{L}}} \quad (1)$$

Also,

$$V_{bias} + \frac{v_{in}}{2} - v_{th} < V_{DD} - \frac{I_o R_L}{2} - \frac{g_m v_{in} R_L}{2} \quad (2)$$

$$V_{bias} < V_{DD} - \frac{I_o R_L}{2} - (1 + g_m R_L) \frac{v_{in}}{2} + v_{th} \quad (3)$$

- ✧ V_{bias} should be such that the transistors M_0 and M_1 are kept in saturation.
- ✧ To maximise signal swing V_{bias} must be at the lowest possible value.
- ✧ With V_{bias} at the minimum value

$$V_{DD} > V_{DSAT1} + V_{DSAT0} + \frac{I_o R_L}{2} + (g_m R_L + 1) \frac{v_{in}}{2}$$

✎ For a differential pair using current sources as load the lower constraint is the same but the upper constraint is given by the sum of overdrive of M_3 and v_{th} .

$$V_{bias} < V_{DD} - \left(\sqrt{\frac{2I_o}{\mu_n C_{ox} \frac{W}{L}}} + v_{th3} \right) + v_{th1} \quad (4)$$