EE539: Analog Integrated Circuit Design; Lecture 20

Nagendra Krishnapura (nagendra@iitm.ac.in)

20 Feb. 2006

Biasing of transistors in Analog ICs

- AC coupling/large caps to short out signal not possible since IC capacitance values are quite small and it will take enormous area to make capacitors to behave as short at relatively low frequencies
- Common-Drain amplifier: gain is independent of g_m and if there is no body effect, change in bias voltages doesn't affect the gain.
- Common-Gate amplifier: the current gain is independent of g_m. So, changes in bias don't affect the gain.
- Common-Source amplifier: gain depends on g_m and it is not possible to get constant gain with changes in bias if we use a single transistor. Either we have to use feedback or we have to go for a differential amplifier.

Current Mirror

A reference current is made to pass through one transistor by diode connecting it.

$$V_{GS} = V_T + \sqrt{\frac{2I_0}{\mu C_{ox}\frac{W}{L}}}$$

Now, if the same V_{GS} is applied to another transistor, then a scaled version of the current flows through it according to the aspect ratio. Equal aspect ratios give the same current.

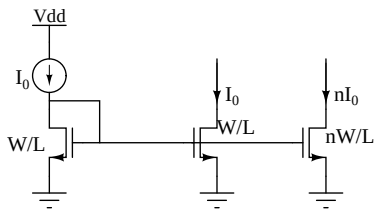

Figure 1: Current Mirror

We have to design W/L according to the required minimum output voltage constraint.

$$\frac{W}{L} \geqslant \frac{2I_0}{(\mu C_{ox})_{min} V_{out}^2}$$

If we use a large value of L, we might get a high resistance at DC, but the large capacitance reduces the resistance at high frequencies. Its the other way around if we use a small value of L. So, we must choose the value of L depending on the expected frequency of operation.
Fig. 2 shows a common drain amplifier biased using a current mirror.

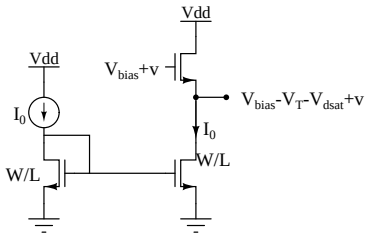

Figure 2: Common Drain biased by current mirror

Cascode current source

We can have a common gate structure above the current source in order to increase the output resistance.

$$r_{out} = \frac{g_{m2}}{g_{ds2} g_{ds1}} + \frac{1}{g_{ds1}} + \frac{1}{g_{ds2}}$$

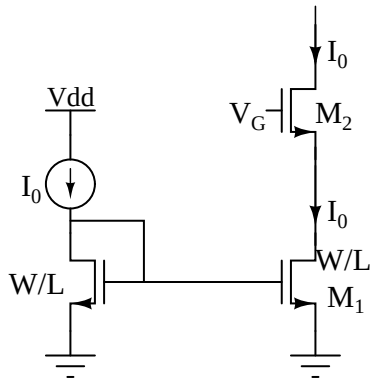

Figure 3: Cascode current source

The downside of this is that the minimum V_{out} is increased by V_{dsat}. Now, M_2 needs to be biased properly for the transistors to work in saturation. We see that

$$V_{G_{min}} = V_T + 2\sqrt{\frac{2I_0}{\mu C_{ox} \frac{W}{L}}} = V_T + \sqrt{\frac{2I_0}{\mu C_{ox} \frac{W}{4L}}}$$

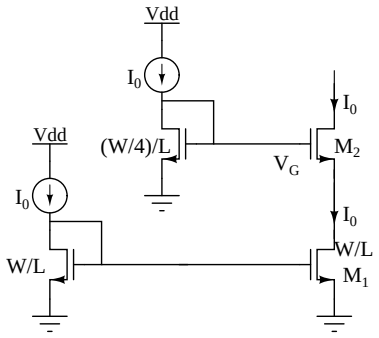

Figure 4: Cascode current source properly biased

We can also have a triple cascode structure where we have one more common gate structure on top of the cascode. This results in an increase in r_{out} by a factor of $\frac{g_m}{g_{ds}}$. The minimum V_{out} increases further by V_{dsat}.

Folded Cascode

In the folded cascode structure, the two transistors are of different type(p and n). An extra current source is needed to provide bias currents for the two transistors.

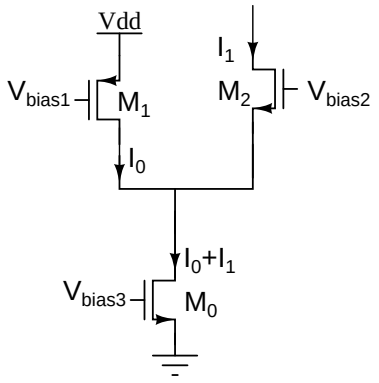

Figure 5: Folded Cascode

$$r_{out} \approx \left(\frac{g_{m2}}{g_{ds2}}\right)\left(\frac{1}{g_{ds0}+g_{ds1}}\right)$$