EE539: Analog Integrated Circuit Design; Lecture 18

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13 Feb. 2006

Common Gate Amplifier

Small Signal Analysis-DC

Consider the Common Gate Amplifier given in Fig. 1 for the following analysis. Assume that it is biased properly. Fig. 2 is the small signal model at DC.

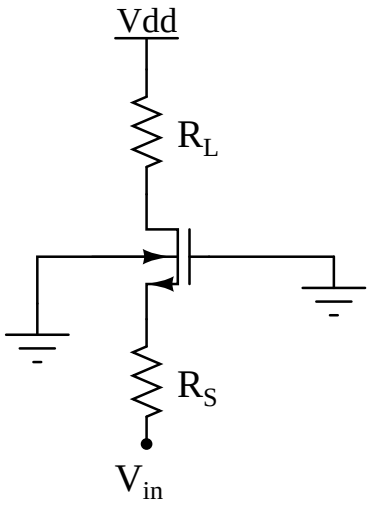

Figure 1: Common Gate Amplifier

Voltage Gain

Applying KCL at source node,

$$\frac{v_o}{R_L} = g_m v_s + g_{mbs} v_s + g_{ds}(v_s - v_o)$$

$$v_s = \frac{v_o\left(\frac{1}{R_L} + g_{ds}\right)}{g_m + g_{mbs} + g_{ds}}$$

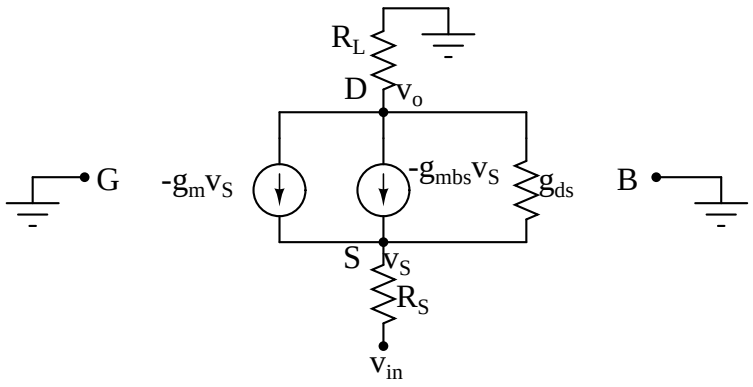

Figure 2: Small signal model at DC

$$\begin{aligned} v_i &= v_s + v_o \frac{R_s}{R_L} \\ &= \frac{v_o\left(\frac{1}{R_L} + g_{ds}\right)}{g_m + g_{mbs} + g_{ds}} + v_o \frac{R_s}{R_L} \end{aligned}$$

$$\frac{v_o}{v_i} = \frac{1}{\frac{R_s}{R_L} + \frac{G_L + g_{ds}}{g_m + g_{mbs} + g_{ds}}}$$

Input Impedance

The input impedance looking into the source,

$$R_i = \frac{v_s}{\left(\frac{v_o}{R_L}\right)} = \frac{1 + g_{ds} R_L}{g_m + g_{mbs} + g_{ds}}$$

If we neglect $g_{ds} R_L$ when compared to unity,

$$R_i \approx \frac{1}{g_m + g_{mbs} + g_{ds}}$$

Output Impedance

Here, we calculate the output impedance looking into the drain,

$$v_o = \frac{\left(g_m + g_{mbs} + \frac{1}{R_s}\right) v_s}{g_{ds}} + v_s$$

$$\begin{aligned} R_{out} &= \frac{\left(g_m + g_{mbs} + \frac{1}{R_s}\right) R_s}{g_{ds}} + R_s \\ &= \frac{1 + (g_m + g_{mbs}) R_s}{g_{ds}} + R_s \end{aligned}$$

- Since output impedance is high, Common Gate amplifier acts as a good current source
- We also see that having a high source resistance in series with source gives a higher resistance.
- To further improve the output resistance of the current source, we can use a cascode configuration. (Fig. 3)

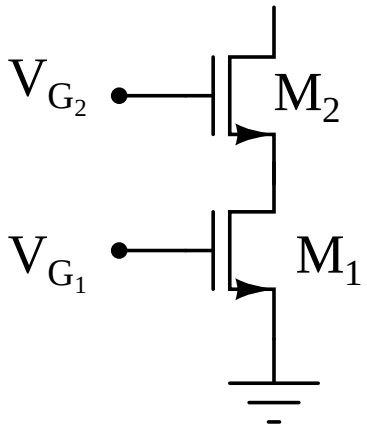

Figure 3: Cascode structure

For the cascode structure,

$$R_{out} = \frac{1 + \frac{(g_m + g_{mbs})}{g_{ds1}}}{g_{ds2}} + \frac{1}{g_{ds1}}$$

Small Signal Analysis-AC

Fig. 4 shows the equivalent circuit. It can be redrawn as in Fig. 5
Here,

$$C_s = C_{gs} + C_{bs}$$

$$C_L = C_{gd} + C_{db}$$

Writing KCL at the source node,

$$(v_{in} - v_s)G_s = v_s s C_s + (g_m + g_{mbs})v_s + g_{ds}(v_s - v_o)$$

Writing KCL at drain node,

$$(g_m + g_{mbs})v_s + g_{ds}(v_s - v_o) = v_o(G_L + sC_L)$$

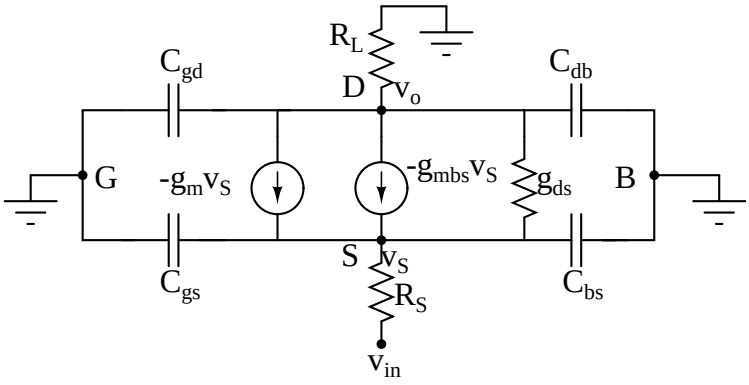

Figure 4: Equivalent Circuit at high frequencies

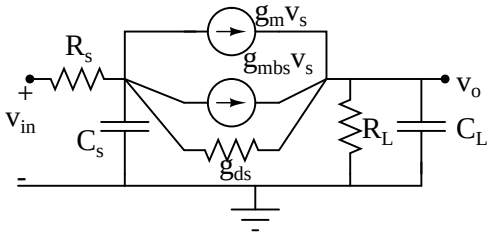

Figure 5: Equivalent Circuit at high frequencies-redrawn

Solving these two equations, we get

$$\frac{v_{in}G_s}{v_o} = (G_L + sC_L) + \frac{(G_L + sC_L + g_{ds})(G_s + sC_s)}{(g_m + g_{mbs} + g_{ds})}$$

If $G_L >> g_{ds}$

$$\frac{v_{in}G_s}{v_o} \approx \frac{(G_L + sC_L)(g_m + g_{mbs} + g_{ds} + G_s + sC_s)}{(g_m + g_{mbs} + g_{ds})}$$

$$\frac{v_o}{v_{in}} \approx \frac{(g_m + g_{mbs} + g_{ds})G_s}{(G_L + sC_L)(g_m + g_{mbs} + g_{ds} + G_s + sC_s)}$$

We see that there are two poles in the transfer function, one low freq pole corresponding to the output side and one high freq pole corresponding to the input side.