EE539: Analog Integrated Circuit Design; Lecture 11

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Single Transistor Amplifiers

- MOSFET - a voltage controlled current source. By passing the current through a resistor, voltage gain can be obtained
- Transconductance (g_m) is higher in saturation region when compared to triode region
  Saturation: $g_m = \frac{\mu C_{ox} W}{L}(V_{GS} - V_T)$
  Triode: $g_m = \frac{\mu C_{ox} W}{L} V_{DS}$ where $V_{DS} < (V_{GS} - V_T)$
- Transconductance is almost independent of V_{DS}in the saturation region(there is a slight variation due to channel length modulation)
  So, amplifiers are always biased in saturation region to get good amplification

Common Source Amplifier

Small signal analysis-DC

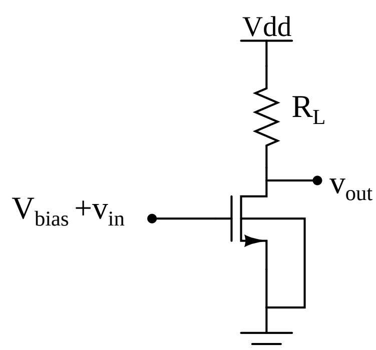

Figure 1: Common source amplifier

Assume that V_{dd} and V_{bias} bias the MOSFET in saturation.

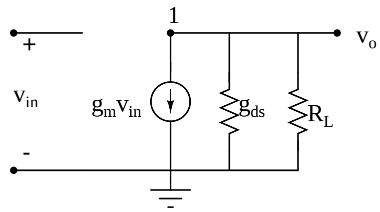

Figure 2: Small signal model at DC

Writing KCL at node 1,
$V_{out}(g_{ds} + G_L) = -g_m V_{in}$
$\frac{V_{out}}{V_{in}} = -\frac{g_m}{g_{ds}+G_L} \approx -\frac{g_m}{G_L}$ if $g_{ds} << G_L$
Max DC gain $=-\frac{g_m}{g_{ds}}$ (at $R_L = \infty$)
Noting that $g_m = \sqrt{2\mu I_d C_{ox} \frac{W}{L}}$ and $g_{ds} = \lambda I_d$
Max DC gain $=\frac{\sqrt{2\mu C_{ox}\frac{W}{L}}}{\lambda}\frac{1}{\sqrt{I_d}}$
We see that, to get the highest possible DC gain,

- Bias current should be as low as possible
- Width of the transistor can be increased while keeping the bias current constant
- Length of the transistor can be increased while keeping the bias current constant. This stems from the fact that λ is inversely proportional to length

We also see from the small signal model that
$R_{in} = \infty$
$R_{out} = \frac{1}{g_{ds}+G_L}$

Small signal analysis-AC (qualitative)

Fig. 3 shows the small signal model at high frequencies. If C_{gd} is neglected, then
Gain$=-\frac{g_m}{g_{ds}+G_L+SC_{db}}$
There will be one pole at $\frac{g_{ds}+G_L}{C_{db}}$
We also note that as R_L increases, gain increases and BW decreases. Also, C_{gs} has no effect since it is just a capacitor in parallel with the input voltage source.(Fig. 4)
Now, if C_{gd} is included, a zero is added at g_m/C_{gd} and we see that the output voltage doesn't go to zero at very high freqs, but settles to a non-zero value depending on the relative values of C_{db} and C_{gd} .(Fig. 5)

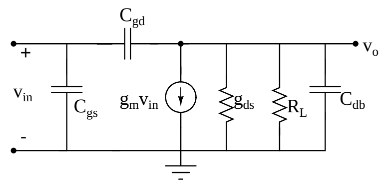

Figure 3: Small signal model at high frequencies

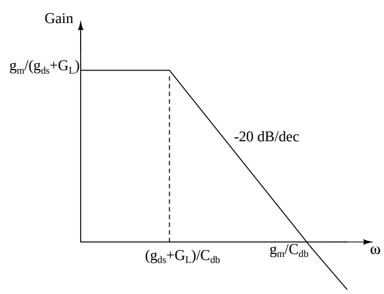

Figure 4: Gain without Cgd

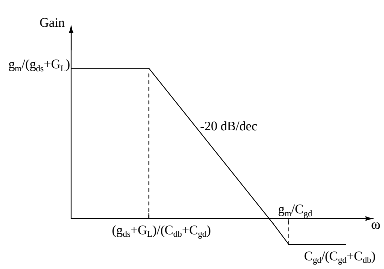

Figure 5: Gain with Cgd