EE539: ANALOG INTEGRATED CIRCUIT DESIGN.

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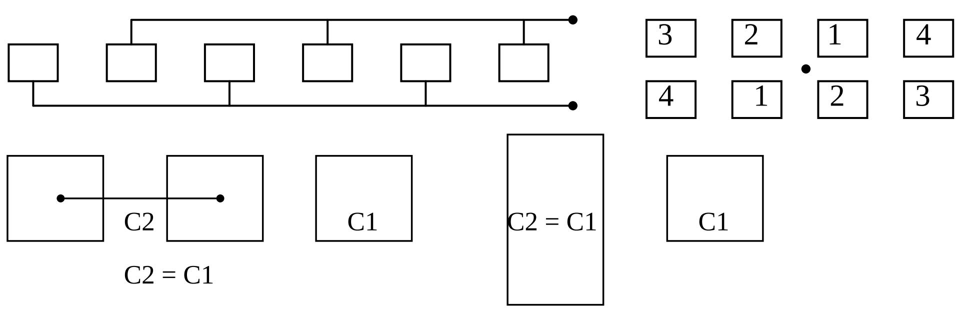
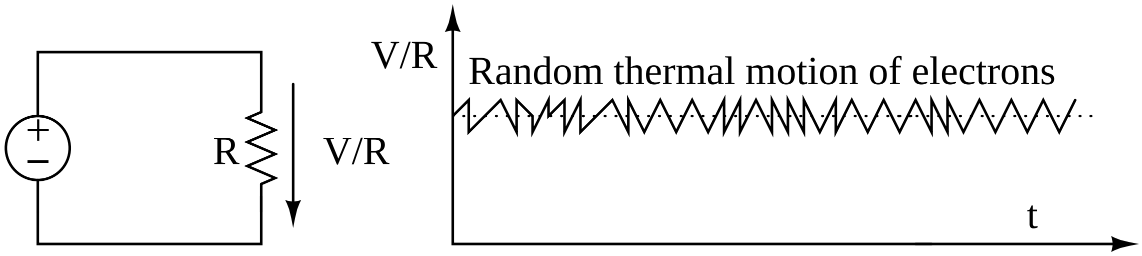
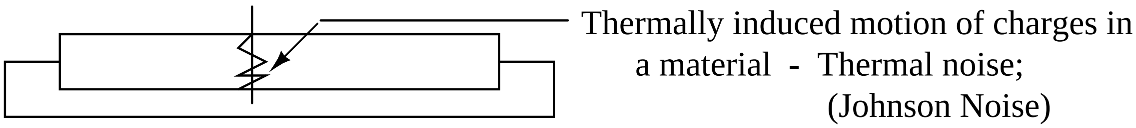
Mismatch in components.

- **Systematic mismatch :**
  - Predicatble variations in component values.
  - Gradients across the chip.
  - Fabrication gradients.
  - Temperature gradients.
  - Usually assumed to be linear.

- **Common centroid arrangement.**
  - The components that need to be matched must have a common centroid
  - But leads to a more complicated layout.



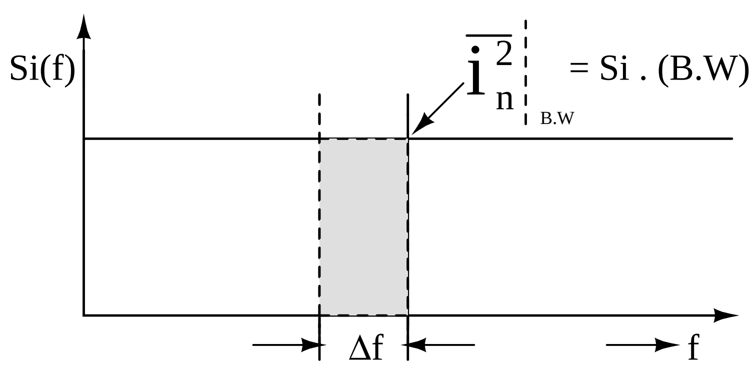


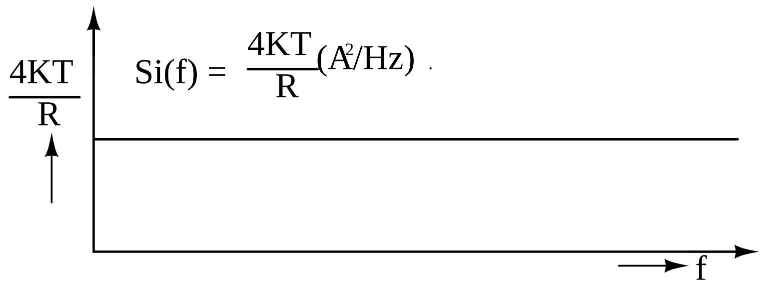


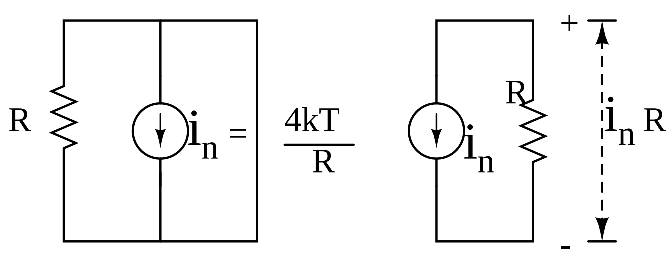
- ✧ $C = C'_A A + C_P.P$;
- ✧ $C_P \Rightarrow$ fringe capacitance per unit length.
- ✧ Dummy devices for identical surroundings.
- ✧ Ratios = no. of identical units.

Noise : Random noise variations in the current(voltage) due to the discreate ness of the current and their random motion.
Thermal noise current i(t); is uncorellated from instant to instant and from component to component.
$i_n(t)$ = Value at each instant is random white noise.
(i.e.... Power spectral density is uniform.)

Resistance : Thermal noise current.

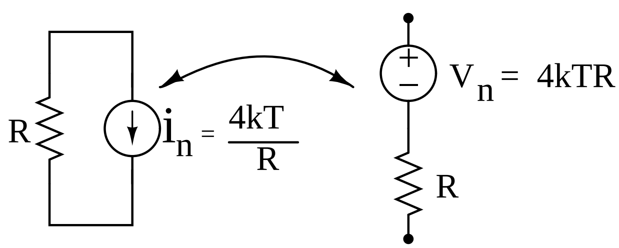


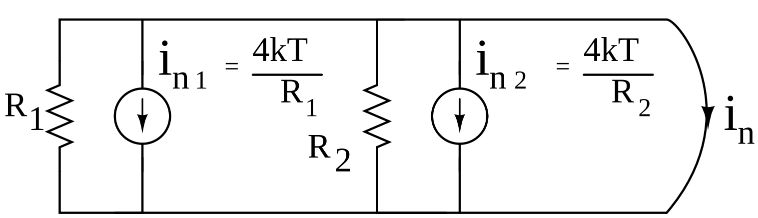




$$V = i_n R$$

$$S_v = \frac{4kT}{R} R^2 = 4kTR$$





$$S_{in} = 4kT \left(\frac{1}{R_1} + \frac{1}{R_2} \right) = \frac{4kT}{R_{eq}}$$

Mean square noise current in the range (f_1, f_2).

$$= \int_{f_1}^{f_2} Si(f)df \frac{4kT}{R}(f_2 - f_1)$$

$$R.M.S = \sqrt{\frac{4kT}{R}(f_2 - f_1).}$$