EE539: Analog Integrated Circuit Design; Lecture 4

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MOSFET-Small Signal Model

- MOSFET: Non-linear element with memory.
- First, analyze non-linearity without memory (dc operating point)
- Around the DC operating point, analyze the effects of small changes in input signal. For small inputs, the cicuit can be considered linear.

Small Signal equivalent Circuit

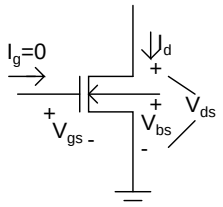

Figure 1: MOSFET Biasing

$$I_D = \frac{\mu C_o x W}{2L}(V_{GS} - V_t(V_{BS}))^2(1 + \lambda V_D S)$$
$$I_D = f(V_{GS}, V_{BS}, V_{DS})$$
$$i_D = \frac{\partial I_D}{\partial V_{GS}}(v_{GS}) + \frac{\partial I_D}{\partial V_{BS}}(v_{BS}) + \frac{\partial I_D}{\partial V_{DS}}(v_{DS})$$

Here, all the differentials are calculated at the DC operating point.

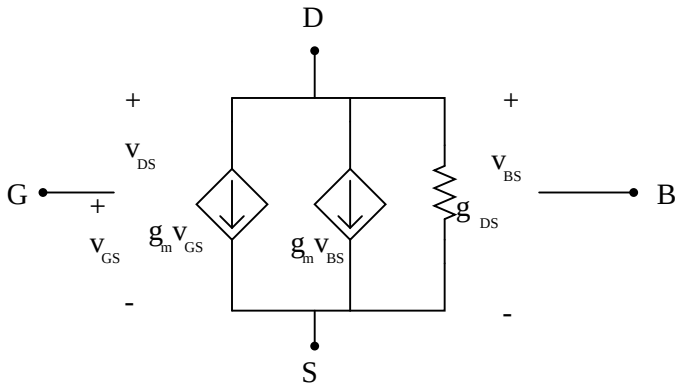

Figure 2: DC Small signal model

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\mu C_{ox} W}{L}(V_{GS} - V_t(V_{BS}))(1 + \lambda V_{DS}) = \frac{2I_D}{[V_{GS} - V_t(V_{BS})]}$$

$$g_{mbs} = \frac{\partial I_D}{\partial V_{BS}} = \frac{-2I_D}{[V_{GS} - V_t(V_{BS})]}\frac{\partial V_t}{\partial V_{BS}}$$

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \frac{\mu C_{ox} W}{2L}(V_{GS} - V_t(V_{BS}))^2\lambda = \frac{\lambda I_D}{1 + \lambda V_{DS}}$$

Capacitances

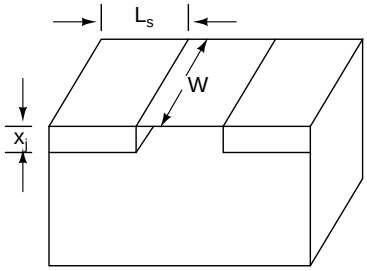

Figure 3: Illustration of Capacitances

- Gate to Channel : distributed, lumped to D/S
  $V_{DS} = 0$, $\frac{C_{ox}WL}{2}$ to D/S
  $V_{DS} > (V_{GS} - V_t)$, $\frac{2}{3}C_{ox}WL$ to S and 0 to D
- Channel to body : distributed, non-linear
- Junction cap : S/D to bulk
  $C_{js} = C_j A_s + C_{jsw} P_s$

$C_{jsw} = C_{jsw'} * x_j$ where $C_{jsw'}$ is the junction cap of side walls per unit area
C_j is the junction cap of bottom plate per unit area
$P_s = 2L_s + W$ and $A_s = L_s * W$
$C_{jd} = C_j A_d + C_{jsw} P_d$
The same calculations apply to drain also

- Overlap cap : Gate to S/D
  $C = C_{ov} W$

- Well to substrate cap: for MOS in well
  $C_{well} = C_{jwell} A_w + C_{jsw} P_w$