EE539: Analog Integrated Circuit Design; HW7

Nagendra Krishnapura (nagendra@iitm.ac.in)

due on 23 Apr. 2006

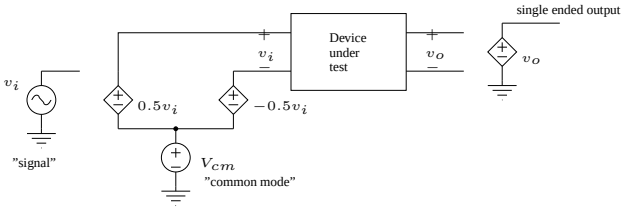

Figure 1: Test bench for differential circuits

0.18 μm technology parameters: $V_{Tn} = 0.5$ V; $V_{Tp} = 0.5$ V; $K_n = 300\ \mu\text{A}/V^2$; $K_p = 75\ \mu\text{A}/V^2$; $A_{VT} = 3.5\,mV\,\mu$m; $A_\beta = 1\%\,\mu$m; $V_{dd} = 1.8$ V; $L_{min} = 0.18\ \mu$m, $W_{min} = 0.24\ \mu$m; Ignore body effect unless mentioned otherwise. Ignore 1/f noise unless mentioned otherwise.

For testing differential circuits, the circuit in Fig. 1 can be used to preserve symmetry and avoid errors (such as not driving the inputs symmetrically). v_i can be the desired signal (ac, dc, or transient). When v_i is the input source for noise analysis, the input referred noise refers to the differential input.

A similar test bench can be created for common mode input/outputs by appropriately changing the controlled sources.

For differential opamps in this assignment, you should not have redesign anything. You only need to turn the opamps already designed to fully differential versions and add common mode feedback circuitry. Use $V_{cm} = 0.9$ V

1. Design a two stage single ended opamp (Fig. 2) that has a dc gain of at least 1000, and a unity gain frequency of 50 MHz with a load of 10 pF and 5 kΩ in parallel. Design the second stage common source amplifier to have a sufficiently high second pole while driving the desired load capacitance. Use a scaled version[1] of the differential amplifier in the P1 of the previous assignment for the input stage and use a suitable compensation capacitor (Fig. 2). Ensure that there is no systematic offset because of the second stage bias. Add a zero canceling resistor. Report the following and show simulation results where appropriate.

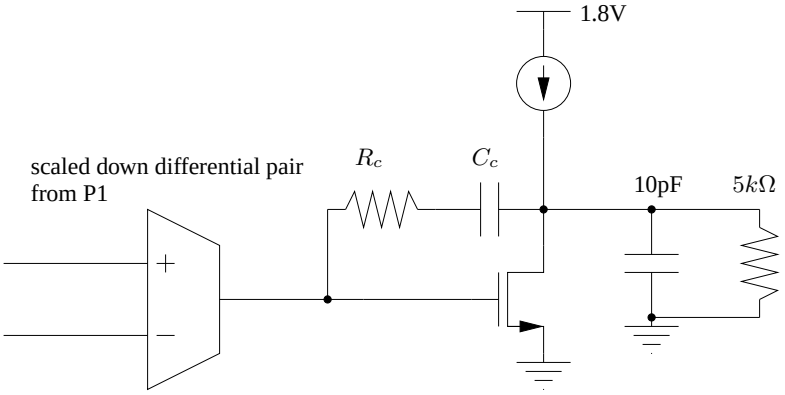

Figure 2: Two stage opamp

   (a) Input common mode range
   (b) Output voltage range
   (c) Open loop and closed loop frequency responses

[1] You should not have to redesign this stage

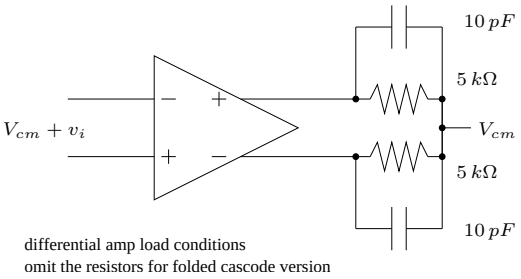

Figure 3: Differential opamp

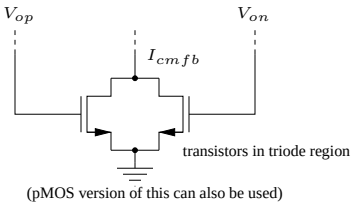

Figure 4: Common mode feedback structure for folded cascode opamp

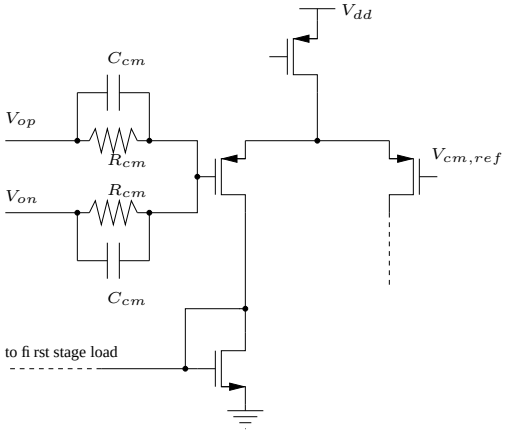

Figure 5: Common mode feedback structure for two stage opamp

(d) An estimate of poles and zeros of the circuit (open and closed loop)

(e) DC sweep of the buffer with input varying from 0 to Vdd

(f) Transient response of the unity gain buffer with a +0.1 V step and a -0.1 V step (use 1 ns rise/fall times). Report the slew rate and compare it with the theoretical value.

(g) Input referred noise spectral density-identify 1/f noise corner if applicable.

(h) Power consumption

(i) Show a schematic with all sizes and operating points (g_m, g_{ds}, V_{GS}-V_T, I_D) of all transistors and the node voltages.

2. Turn the folded cascode opamp designed in assignment 6 to a fully differential version. Use the circuit in Fig. 4 for common mode feedback. Size the CMFB transistors to have 50 mV across them in quiescent condition. Report the following and show simulation results where appropriate.

   (a) Input common mode range

   (b) Output voltage range

   (c) Open loop frequency response

   (d) An estimate of poles and zeros of the circuit

   (e) Input(differential) referred noise spectral density-identify 1/f noise corner if applicable.

   (f) Power consumption

   (g) Show a schematic with all sizes and operating points (g_m, g_{ds}, V_{GS}-V_T, I_D) of all transistors and the node voltages.

3. Turn the two stage opamp in P1 above into a fully differential version. Use the circuit in Fig. 5 for common mode feedback. Report the same quantities as above.

4. Use the opamps in P2 and P3 (fully differential opamps designed earlier) in the sample hold circuit in Fig. 6. Use ideal switches with 1 kΩ on resistance. Use $f_s = 4$ MHz and

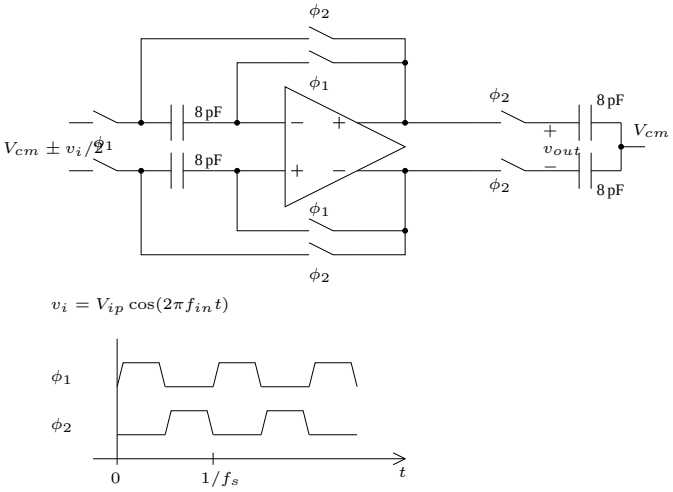

Figure 6: Sample and hold circuit

$f_{in} = \{1/4, 9/4\}$ MHz (sinusoidal input with 1.6 Vppd[2] amplitude) and plot the output waveforms.

5. Simulate the response of the circuit in Fig. 7 to a differential step of 1 V and plot the output. Also plot the output for a 0.5 V common mode step. Use the two stage fully differential opamp designed above.

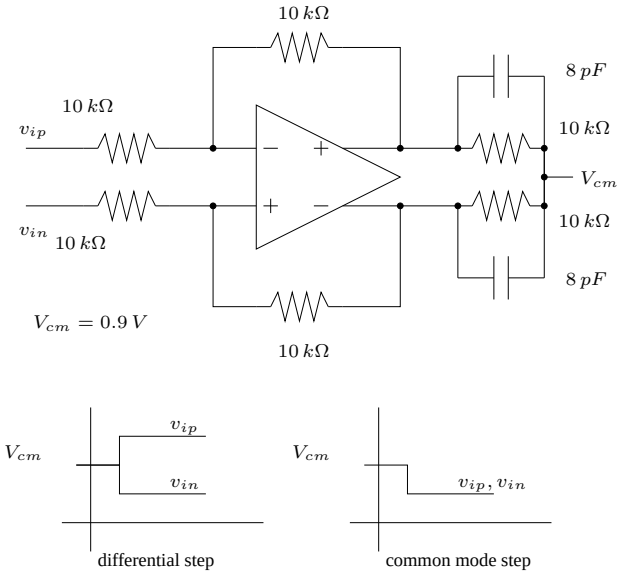

Figure 7: Inverting amplifier

[2]Vppd: volts, peak-peak differential