EE539: Analog Integrated Circuit Design; HW6

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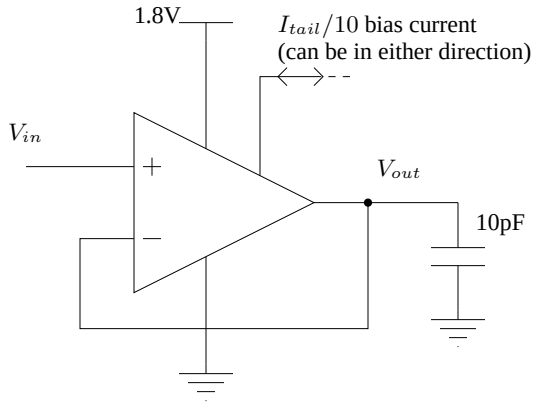

Figure 1: Unity gain buffer with an opamp

0.18 μm technology parameters: $V_{Tn} = 0.5$ V; $V_{Tp} = 0.5$ V; $K_n = 300\ \mu\text{A}/V^2$; $K_p = 75\ \mu\text{A}/V^2$; $A_{VT} = 3.5\,mV\,\mu$m; $A_\beta = 1\%\,\mu$m; $V_{dd} = 1.8$ V; $L_{min} = 0.18\ \mu$m, $W_{min} = 0.24\ \mu$m; Ignore body effect unless mentioned otherwise. Ignore 1/f noise unless mentioned otherwise.

1. Design a single stage single ended opamp with a dc gain of 50 using a pMOS differential pair. The application is a unity gain buffer with 0.5 Vpp (± 0.25 V around the common mode) swing. The unity gain buffer should have a 3 dB bandwidth of 50 MHz, with $C_L = 10$ pF. All parasitic poles and zeros should be at at least twice the unity gain frequency. Report the following and show simulation results where appropriate.

   (a) Input common mode range

   (b) Output voltage range

   (c) Open loop and closed loop frequency responses

   (d) An estimate of poles and zeros of the circuit (open and closed loop)

   (e) DC sweep of the buffer with input varying from 0 to Vdd

   (f) Transient response of the unity gain buffer with a +0.1 V step and a -0.1 V step (use 1 ns rise/fall times). Report the slew rate and compare it with the theoretical value.

   (g) Input referred noise spectral density-identify 1/f noise corner if applicable.

   (h) Power consumption

   (i) Show a schematic with all sizes and operating points (g_m, g_{ds}, V_{GS}-V_T, I_D) of all transistors and the node voltages.

Do not use an ideal current source in the tail. You can use one ideal reference current source of 1/10$^{\text{th}}$ the tail current for bias generation (Fig. 1).

Try to determine as many parameters as possible from the specifications and choose sensible starting points for the others. Try to adjust the channel lengths so that g_{ds} contributions from nMOS and pMOS sides are equal (This is not the only possible choice. Other choices may be preferable to optimize other figures of merit-e.g.

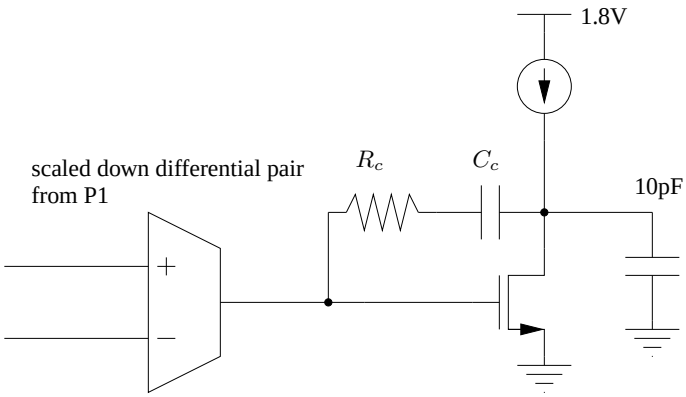

Figure 2: Unity gain buffer with an opamp

noise. This is a suggested starting point for simplicity). Choose an appropriate common mode voltage.

Try to maximize the output voltage swing and reduce the power consumption during the design.

2. Turn the previously designed circuit into a telescopic cascode opamp[1]. Use cascode devices of the same size as the respective devices. Design the biasing circuit for the cascode devices to maximize the swing. Report the same quantities as above.

3. Turn the circuit in P. 1 into a folded cascode opamp[1]. Ensure that the slew rate limitations due to the first and the second stage are identical. Design the biasing circuit for the cascode devices to maximize the swing. Report the same quantities as above.

4. Design a two stage single ended opamp that satisfies the specs above. Design the second stage common source amplifier to have a sufficiently high second pole while driving the desired load capacitance. Use a scaled down version of the differential amplifier in the first problem for the input stage and use a suitable compensation capacitor (Fig. 2). Ensure that there is no systematic offset because of the second stage bias. Add a zero canceling resistor. Report the same quantities as above.

[1]Do not redesign the circuit except for the addition of cascode devices and suitable bias circuitry