# EE539: Analog Integrated Circuit Design; HW5

Nagendra Krishnapura (nagendra@iitm.ac.in)

due on 15 Mar. 2006

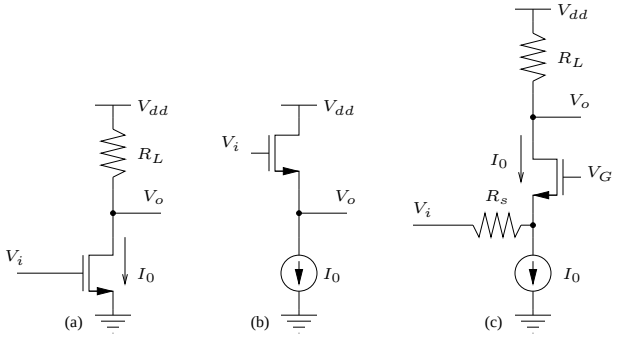


Figure 1: Problem 1

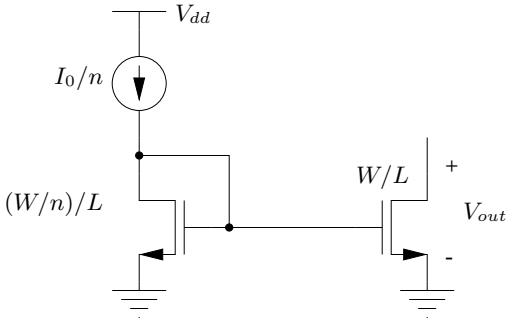


Figure 2: Problem 3

0.18 $\mu$m technology parameters: $V_{Tn} = 0.5$ V; $V_{Tp} = 0.5$ V; $K_n = 300\ \mu\text{A}/V^2$; $K_p = 75\ \mu\text{A}/V^2$; $A_{VT} = 3.5\,mV\,\mu$m; $A_\beta = 1\%\,\mu$m; $V_{dd} = 1.8$ V; $L_{min} = 0.18\ \mu$m, $W_{min} = 0.24\ \mu$m; Ignore body effect unless mentioned otherwise. Ignore 1/f noise unless mentioned otherwise.

1. Determine the output and input referred noise voltages of the stages in Fig. 1.

2. A 1:1 current mirror has devices with sizes $W/L$ and an output current $I_0$ has an rms current mismatch in the output of $\sigma_{I0}$. Redesign the current mirror to have an rms mismatch of $\sigma_{I0}/2$. (It should be usable in place of the origianl source).

3. A current mirror generating $I_0$ is realized as shown in Fig. 2. It is required to support a minimum output voltage of $V_{out}$. It is proposed that the reference branch have a current $I_0/n$ in order to minimize "overhead" currents. How do the power consumption and noise compare with a 1:1 current mirror?

4. Compute the contribution to output current noise from noise current $i_{n1}$ and $i_{n2}$ in the two devices in Fig. 3.

5. Compute the effect of threshold voltage mismatch ($\Delta V_{t1,2}$) and current factor mismatch ($\Delta\beta_{1,2}$) in the top and the bottom transistors in Fig. 4.

6. Compute $v_o/v_i$ in the two circuits in Fig. 5. Calculate the tail node voltage in each case. Explain the results.

7. Compute the differential frequency response. Consider $g_m, C_{gs}, C_{gd}, C_{db}$ in the calculations. What is the purpose of $C_f$? What value would you set it to?

8. Design and simulate a 100 $\mu$A pMOS cascode current mirror using 0.5 $\mu$m length transistors

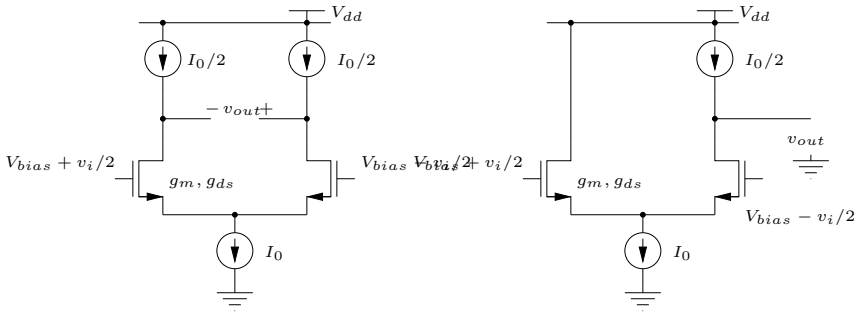


Figure 5: Problem 6

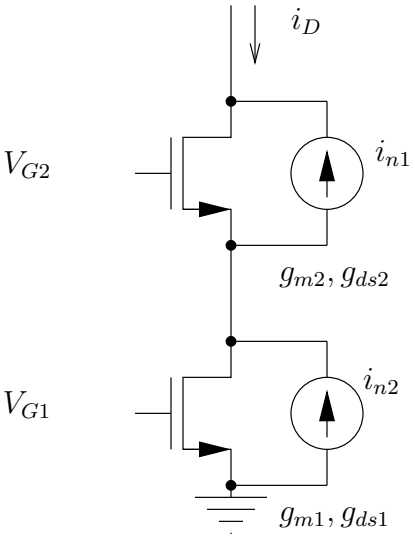


Figure 3: Problem 4

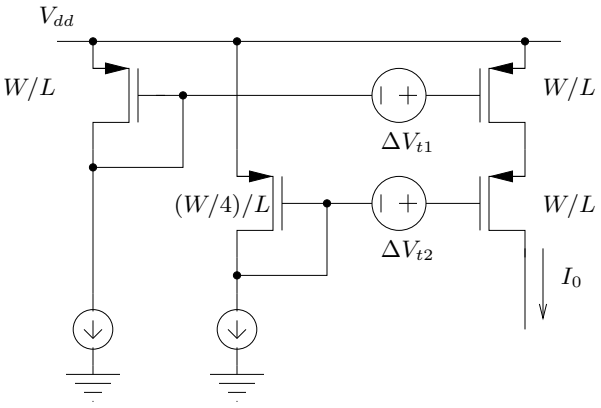


Figure 4: Problem 5

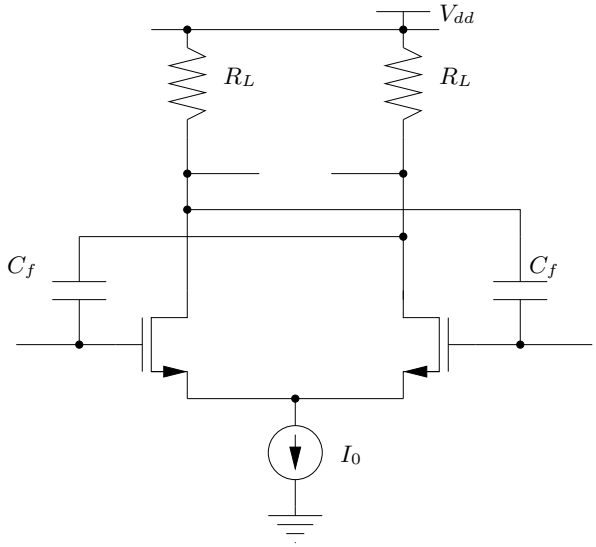


Figure 6: Problem 7

for $V_{out} = 300\,mV$. Report the dc node voltages and the saturation voltages of each transistor. Plot the output impedance vs. frequency. Reduce $W$ and $L$ of the cascoding device by 2x and plot $|Z_{out}|$ vs. frequency on the same plot. What do you infer?