EE539: Analog Integrated Circuit Design; HW4

Nagendra Krishnapura (nagendra@iitm.ac.in)

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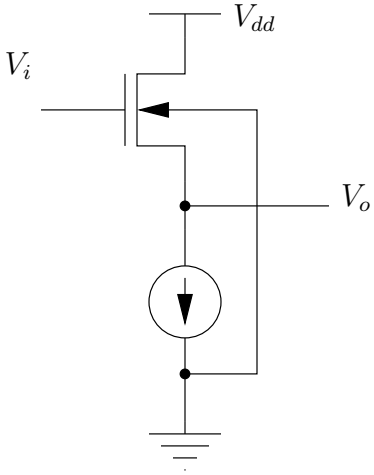

Figure 1:

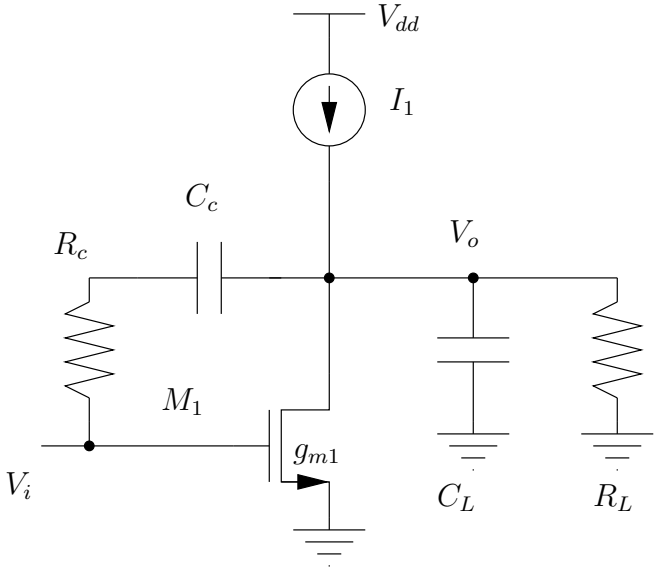

Figure 2:

0.18 μm technology parameters: $V_{Tn} = 0.5$ V; $V_{Tp} = 0.5$ V; $K_n = 300\ \mu\text{A}/V^2$; $K_p = 75\ \mu\text{A}/V^2$; $A_{VT} = 3.5\,mV\,\mu$m; $A_\beta = 1\%\,\mu$m; $V_{dd} = 1.8$ V; $L_{min} = 0.18\ \mu$m, $W_{min} = 0.24\ \mu$m; Ignore body effect unless mentioned otherwise.

1. The threshold voltage of the MOS transistor in Fig. 1 is given by $V_T = V_{T0} + \gamma(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F})$. Find the first three coefficients of the Taylor expansion of the function $V_o = f(V_i)$.

2. Compute the small signal transfer function V_o/V_i in Fig. 2. What is the purpose of R_c? What value would you set it to? Why?

3. Compute the small signal transfer function V_o/V_i in Fig. 3. What is the 3 dB bandwidth of the circuit with $R_G = 0$? Calculate R_G for maximally flat magnitude response (Derivatives of $|V_o(\jmath\omega)/V_i(\jmath\omega)|$ should be zero). What is the 3 dB bandwidth in this case?

4. Calculate analytically the transfer function V_o/V_s for the amplifier in Fig. 4.

   $g_{m1} = 100\,\mu$S, $g_{ds1} = 1\,\mu$S, $g_{m2} = 200\,\mu$S, $g_{ds2} = 4\,\mu$S, $C_L = 1$ pF, $C_1 = 1/16$ pF. With $R_c = 0$, determine C_c such that the phase shift is 120° when the gain magnitude is unity. Determine the poles and zeros of the system.

   Determine the poles and zeros of the system, the unity gain frequency, and the phase shift at unity gain frequency for

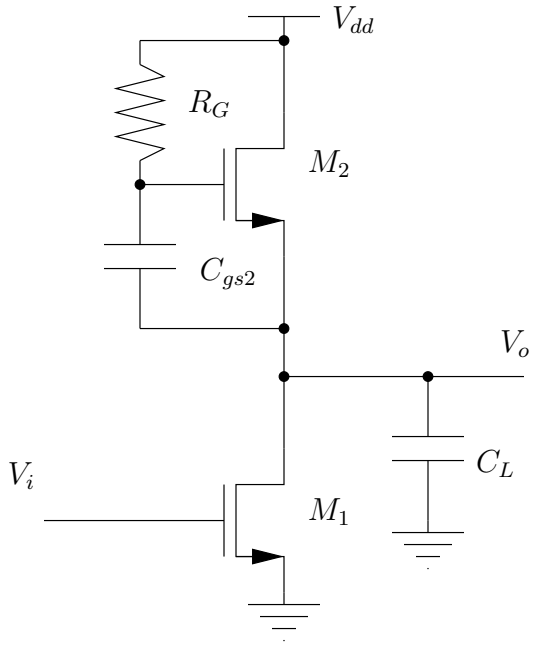

Figure 3:

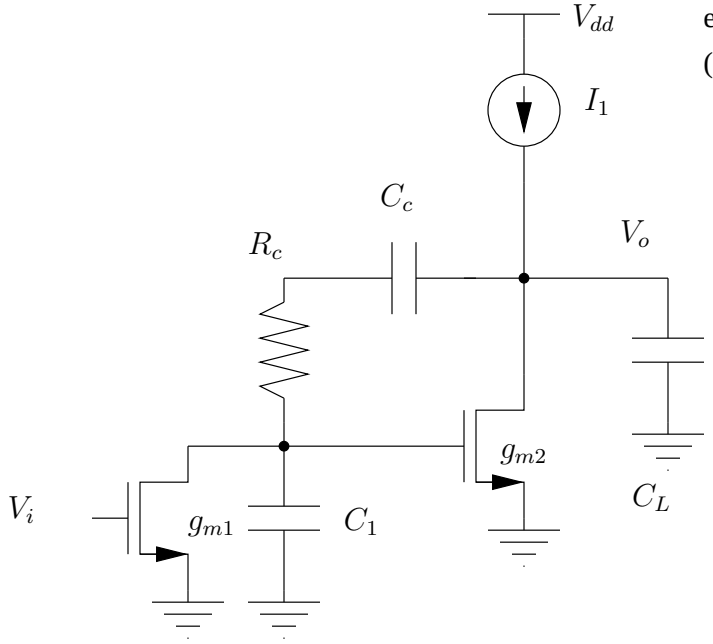

Figure 4:

(a) $R_c = 0$, $C_c = \{0, 1/4, 1/2, 1, 2\}$ pF;

(b) $R_c = 5\,\text{k}\Omega$, $C_c = \{0, 1/4, 1/2, 1, 2\}$ pF

(c) $R_c = 5\,\text{k}\Omega + 1/(2 \times 10^8 C_c)$, $C_c = \{0, 1/4, 1/2, 1, 2\}$ pF.

What do you infer from the results?

5. A two stage amplifier is shown in Fig. 5(a) (biasing arrangement not shown completely). Neglect parasitic capacitors other than the ones shown. Neglect g_{ds2}. C_{db1}, C_{db2}, and C_{gs2} are of the order of 10% of C_c and C_L. Assume that the dc bias through $M_{1,2}$ is $I_{1,2}$. V_L is such that no dc flows through R_L. C_c is an external capacitor. The small signal frequency response is as shown in Fig. 5(b).

   For each of the following, suggest modifications (to $M_{1,2}$, $I_{1,2}$, or C_c) if necessary and state what happens to A_{dc}, ω_u, p_2, z_1, and the power dissipation of the circuit. Consider both first and second order variations. Provide very brief explanations for each answer. For (a), (b), and (d), provide two alternative solutions.

   (a) The dc gain needs to be doubled. ω_u, p_2, or z_1 should not change in the first order.

   (b) The load capacitance is doubled. The unity gain frequency and the second second pole should not change in the first order.

   (c) I_2 is reduced to half its value.

   (d) The load resistance is halved, but the dc gain should be maintained at A_0.

   (e) The size is halved by shrinking all transistors in X and Y direction by $2\times$.

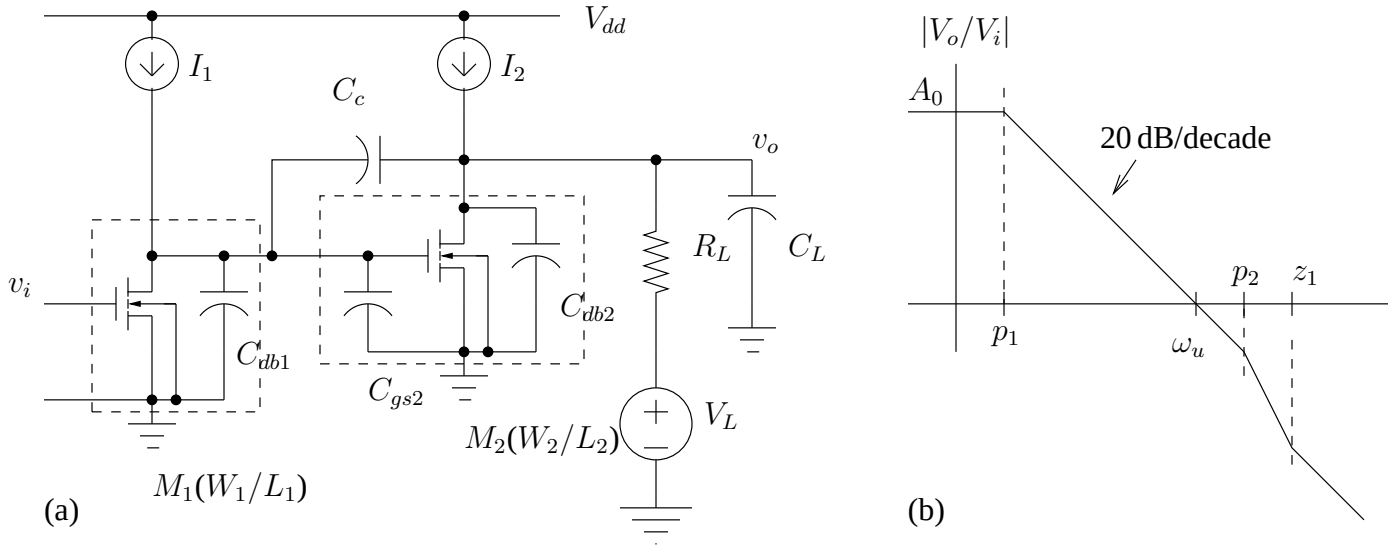

Figure 5: Two stage amplifier