EE539: Analog Integrated Circuit Design; HW3

Nagendra Krishnapura (nagendra@iitm.ac.in)

due on 8 Feb. 2006

0.18 μm technology parameters: $V_{Tn} = 0.5$ V; $V_{Tp} = 0.5$ V; $K_n = 300\ \mu\text{A}/V^2$; $K_p = 75\ \mu\text{A}/V^2$; $A_{VT} = 3.5\,mV\ \mu$m; $A_\beta = 1\%\,\mu$m; $V_{dd} = 1.8$ V; $L_{min} = 0.18\ \mu$m, $W_{min} = 0.24\ \mu$m; Ignore body effect unless mentioned otherwise.

1. Bias a pMOS transistor with $V_{GS} = V_{DS} = 1\,V$ and determine W (with minimum length) to get a current of 100 μA. Simulate S_{I_D} the noise spectral density of drain current from 100 Hz to 100 MHz.

   Double the length and resize W to get 100 μA, and simulate S_{I_D}. Repeat until $L = 5.76\,\mu$m. Overlay the spectral density plots and identify the $1/f$ noise corners. Briefly explain the results.

2. Repeat for nMOS

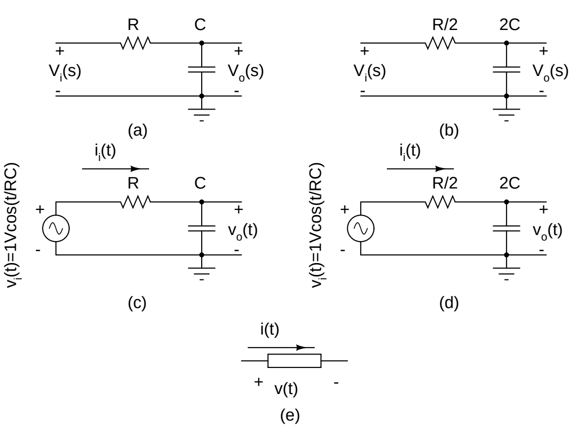

Figure 1:

3. For the circuits in Fig. 1(a) and Fig. 1(b), evaluate the transfer function $H(s) = V_o(s)/V_i(s)$ and the output rms noise voltage.

4. In the circuits in Fig. 1(c) and Fig. 1(d), evaluate the current $i_i(t)$ through the input voltage source. Evaluate the average power dissipated in the voltage source and the resistor, and the output rms signal voltage. Compare the signal to noise ratio (S/N) and the power dissipation of the two circuits.

5. Evaluate analytically the output signal to noise ratio (S/N) for an input peak voltage V_p, the power dissipation P in the resistor, and the bandwidth f_b (in Hz) of the circuit in Fig. 1(c). Express the power dissipation in terms of S/N and f_b.

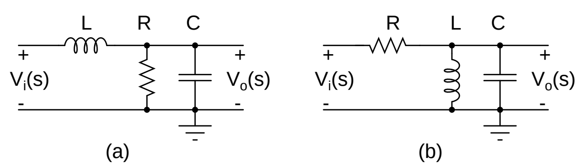

Figure 2:

6. Calculate the transfer functions and the output noise spectral density of the filters in Fig. 2(a,b). Simulate the transfer function and the output noise spectral density(in $V/\sqrt{Hz}$) for $L = 10$ nH, $C = 10$ pF, $R = 100$ from 1 MHz to 10 GHz.