EE539: Analog Integrated Circuit Design; HW2

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due on 30 Jan. 2006

0.18 μm technology parameters: $V_{Tn} = 0.5$ V; $V_{Tp} = 0.5$ V; $K_n = 300\ \mu\text{A}/V^2$; $K_p = 75\ \mu\text{A}/V^2$; $A_{VT} = 3.5\,mV\,\mu$m; $A_\beta = 1\%\,\mu$m; $V_{dd} = 1.8$ V; $L_{min} = 0.18\ \mu$m, $W_{min} = 0.24\ \mu$m; Ignore body effect unless mentioned otherwise.

1. Textbook problem 2.11 (Textbook Fig. 2.48;You don't have to sketch-just show the calculations)

2. Design a 1 pF capacitor using A square nMOS device (drain/source shorted). Plot its capacitance as a function of voltage (0 to 1.8 V). What is the usable voltage range of this capacitor?

   Repeat the above for a square pMOS device.

   Repeat the above for a parallel combination of equal sized nMOS and pMOS.

   A square Metal1-Metal2 structure

   A square sandwiched structure with poly, M2, M4 tied together and M1, M3, M5 tied together.

3. Plot the f_T of an nMOS device with W/L from $3.6\,\mu\text{m}/0.18\,\mu\text{m}$ to $115.2\,\mu\text{m}/5.76\,\mu\text{m}$ with W and L doubled in each step. Comment on the results.

4. Two transistors carrying a current I_D are required to have a current mismatch $\leq \sigma_{I_D}$ and operate in saturation with an output voltage V_{out} (Fig. 1). Compute the transistor dimensions and its f_T in terms of the mismatch constants A_{VT} and A_β, I_D, σ_{I_D} and V_{out}. Comment on tradeoffs between speed, voltage, and precision.

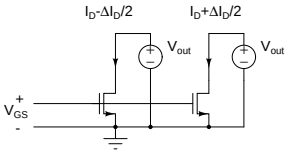

Figure 1:

5. The current in a velocity saturated device is given by $I_D \approx WC_{ox}(V_{GS} - V_T)v_{sat}$ where v_{sat} is the saturation velocity. Compute the g_m and the f_T of such a device and comment on the qualitative differences from a device without velocity saturation. Simulate I_D versus L for a $10\,\mu\text{m}/L$ device with $V_{GS} = V_{DS} = 1$ V and identify the onset of velocity saturation.

6. Plot g_m, g_{ds}, g_{mbs}, g_m/g_{ds}, f_T, V_{GS}, and $V_{DS,SAT}$[1] as a function of I_D (from $1\,\mu$A to $100\,\mu$A) for a diode connected nMOS transistor for two cases: $W/L = 5\,\mu\text{m}/0.5\,\mu$m and $W/L = 25\,\mu\text{m}/2.5\,\mu$m. In each case, overlay the plots for 0°C and 100°C.

7. Repeat the previous problem for pMOS.

[1] g_m, g_{ds}, g_{mbs}, V_{GS}, and $V_{DS,SAT}$ will be reported by the simulator at the dc operating point. Calculate f_T