EE539: Analog Integrated Circuit Design; HW1

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Submit all solutions by email as a single pdf file; Present the solutions in the same order as the problems below.

0.18 μm technology parameters: $V_{Tn} = 0.5$ V; $V_{Tp} = 0.5$ V; $K_n = 300$ μA$/V^2$; $K_p = 75$ μA$/V^2$; $A_{VT} = 3.5\,mV$ μm; $A_\beta = 1\%$ μm; $V_{dd} = 1.8$ V; $L_{min} = 0.18$ μm, $W_{min} = 0.24$ μm; Ignore body effect unless mentioned otherwise.

1. Textbook problem 2.6 (Textbook Figure 2.43). I_x and g_m of M_1.

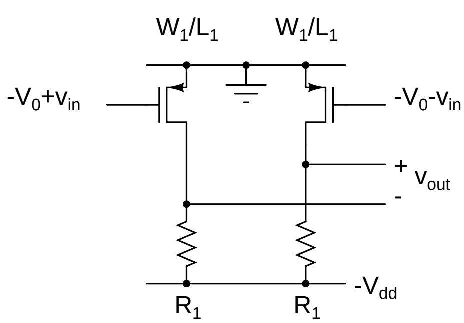

Figure 1: Problem 2

2. Calculate V_{out} in Fig. 1. Comment.

3. Calculate V_{out} in Fig. 2. Comment.

4. Calculate $V_{1,2}$ in Fig. 3(a, b). What is a possible application of this circuit? What is the minimum V_{dd} required? How do $V_{1,2}$ change if the substrates of the transistors are not connected to their individual sources (Fig. 3(c, d)).

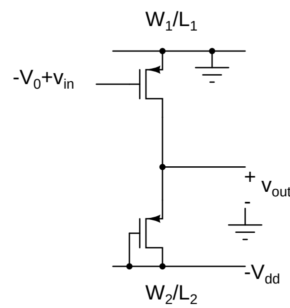

Figure 2: Problem 3

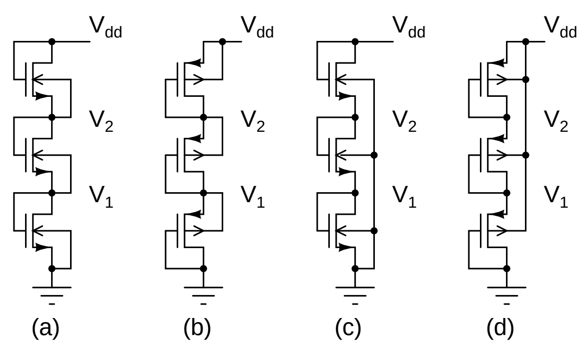

Figure 3: Problem 4

5. (For this problem, The minimum usable dimension is $0.5\,\mu$m.) A MOSFET is used as a $100\,\mathrm{k}\Omega$ resistor (Fig. 4) $V_0 = 0.5\,V$ and v_x is restricted to 0.2 V. The nonlinearity of the resistance should be at most 5%. Calculate the gate bias V_{bias} and the dimensions of the transistor. If a linear resistive material with a sheet resistance of 8 Ω/sq. is available, what would be its dimensions? What is the motivation for using a transistor instead of a resistive material?

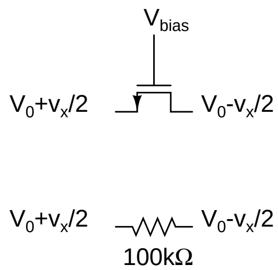

Figure 4: Problem 5

The following are to be simulated. Repeat for pMOS and nMOS.

1. Plot I_D vs. V_{DS} (0 to 1.8 V) for V_{GS} from 0 to 1.5 V in steps of 0.25 V and $V_{BS} = 0$ V. Overlay the plots for $W/L = 5\,\mu$m$/0.5\,\mu$m and $W/L = 25\,\mu$m$/2.5\,\mu$m. Comment on the results.

2. Plot I_D vs. V_{DS} (0 to 1.8 V) for V_{BS} from -1 V to 0 V in steps of 0.25 V and $V_{GS} = 1.5$ V. Overlay the plots for $W/L = 5\,\mu$m$/0.5\,\mu$m and $W/L = 25\,\mu$m$/2.5\,\mu$m. Comment on the results.

3. Plot (log-log) I_D vs. V_{GS} (18 mV to 1.8 V) for $V_{DS} = 1$ V and $V_{BS} = 0$ V. Overlay the plots for $W/L = 5\,\mu$m$/0.5\,\mu$m and $W/L = 25\,\mu$m$/2.5\,\mu$m and temperatures of $\{0, 27, 100\}$°C. Comment on the results. Calculate the subthreshold slope η.

4. Plot (log-log) I_D vs. V_{BS} (-1.5 V to -15 mV) for $V_{DS} = 1$ V and $V_{GS} = 1$ V. Overlay the plots for $W/L = 5\,\mu$m$/0.5\,\mu$m and $W/L = 25\,\mu$m$/2.5\,\mu$m and temperatures of $\{0, 27, 100\}$°C. Comment on the results.