Clock Recovery From Random Binary Signals

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A circuit for detecting timing errors between a binary signal and a local clock pulse generator is described. Three binary samples are compared and logical control signals for the clock are derived.

Clock recovery is often essential for the regeneration of distorted binary signals. The paucity of published work in this field has been noted in a recent paper.[1] Some techniques are outlined in Bennett and Davey.[2] A simple scheme is described in this letter in which zero or datum crossings of a distorted binary signal are measured as early or late events when compared with the transitions of a local clock wave. The circuit is simple to build in t.t.l. and may be used as the detector for an analogue or digital phase-locked loop to achieve clock synchronisation.

An idealised eye diagram is shown in Fig. 1. Two samples are taken in each nominal bit interval. Samples are taken close to midbit and changeover times. Midbit samples taken at times A, C, and E, may be called a, c and e, the changeover samples then being b and d. These samples are transformed into binary variables and processed digitally.

A suitable circuit is shown in Fig. 2. Signal S is the output of a limiter. This signal is a binary function given by the zero, or datum, crossing of the distorted analogue waveform. Samples of S are taken by clocked D-type monostables D_1 and D_3. Clock pulse trains CKM and CKC are at the nominal data rate, and CKM is arranged to be near to the midbit instant whilst CKC occurs at the changeover time. Complementary squarewave clock waveforms and edge triggered monostables ensure exactly interleaved sampling.

Sample a is transferred to D_2 at time C when D_1 stores sample c. At this time, sample b is transferred to D_4. This enables the variables a, b and c to be examined simultaneously at the outputs of D_1, D_2, and D_4. If the midbit clock is early, $a = b$, and $b = c$ randomly. Similarly, if the midbit clock is late, $b = c$ and $a = b$ randomly.

The binary variables a, b and c are related to the early–late situations by the following four rules:

(a) If $a = b$ and $b \neq c$, the clock is late.

(b) If $a \neq b$ and $b = c$, the clock is early.

(c) If $a = b = c$, no decision is possible.

(d) If $a = c \neq b$, no decision is possible.

Let E represent early, L represent late and X represent indecision. The eight possible combinations of abc and the conclusion drawn from the four rules are shown in Table 1.

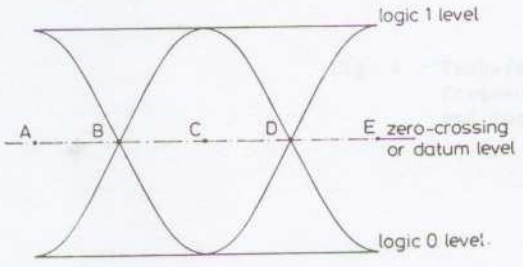

Fig. 1 *Eye diagram showing synchronous timing instants*

Table 1

a	b	c	Conclusions
0	0	0	X
0	0	1	L
0	1	0	X
0	1	1	E
1	0	0	E
1	0	1	X
1	1	0	L
1	1	1	X

A set of control functions may be deduced by noting the conclusion entry is reflected. If the pure binary sequence is expressed as a Grey sequence rst, the XLE function independent of r, as shown in Table 2. This shows that

Table 2

r	s	t	Conclusions
0	0	0	X
0	0	1	L
0	1	1	X
0	1	0	E
1	1	0	E
1	1	1	X
1	0	1	L
1	0	0	X

the modulo-2 sum of s and t, and L is given by t:

$$\bar{X} = s \oplus t$$

But, since

$$s \oplus t = a \oplus b \oplus b \oplus c$$

$$\bar{X} = a \oplus c$$

and

$$X = \overline{a \oplus c}$$

also

$$L = b \oplus c$$

An oscillator may be designed to operate at either of three frequencies: f_0, $f_0 + f_x$ and $f_0 - f_x$. An example of this type of oscillator is the logical phase-controlled oscillator. Frequency control requires a 2 bit word, and the relation

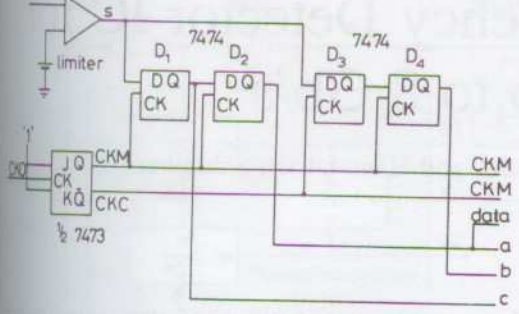

Fig. 2 *Sampling circuit and clock pulse generator*

are shown in Table 3. Any appropriate 3-frequency oscillator

Table 3

$P = \overline{a \oplus c}$

$Q = b \oplus c$

Control word P Q	Frequency
0 0	f_0
0 1	f_0
1 0	$f_0 + f_x$
1 1	$f_0 - f_x$

may be used in conjunction with the early–late detector to realise a phase-locked clock recovery system.

An alternative technique involves the generation of a 3-level signal for frequency control of a v.c.o. A 3-valued variable A may be generated:

$$A = (a \oplus b) \text{ minus } (b \oplus c)$$

The relationships between the binary word *abc* and the 3-valued variable A are shown in Table 4. Circuits for the generation of the logical control signals, P, Q and the 3-valued variable A for analogue loops are shown in Fig. 3.

loop, the sample a may be taken as a true midbit sample of the distorted binary signal. An alternative use for the synchronised changeover clock CKC is control of an integrate-and-dump detector operating directly on the unsliced binary signal.

Table 4

a	b	c	$a \oplus b$	$b \oplus c$	A	early–late
0	0	0	0	0	0	X
0	0	1	0	1	−1	L
0	1	0	1	1	0	X
0	1	1	1	0	+1	E
1	0	0	1	0	+1	E
1	0	1	1	1	0	X
1	1	0	0	1	−1	L
1	1	1	0	0	0	X

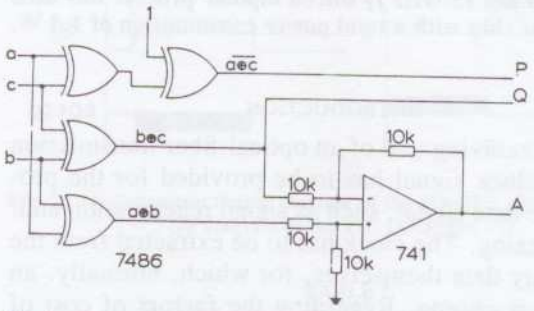

Fig. 3 *2 bit binary and 3-level analogue early–late detectors*

References

1 BETTS, J. A., BROOM, R. S., COOK, S. J., and CLARK, J. G.: 'Use of pilot tones for real-time channel estimation of h.f. data circuits', *Proc. IEE*, 1975, **122**, (9), pp. 887–896

2 BENNETT, W. R., and DAVEY, J. R.: 'Data transmission' (McGraw-Hill, 1965), chap. 14