EE2019

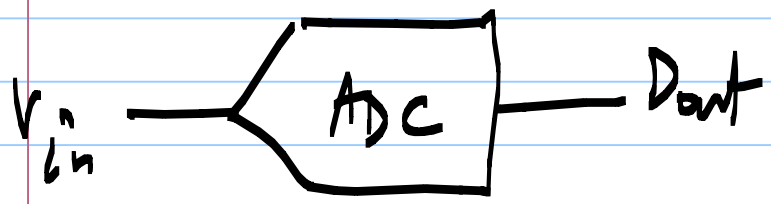
20/4/2018

N: # bits,

V_{ref}: reference voltage

f_s: Sampling rate

Analog-to-Digital conversion (ADCs)

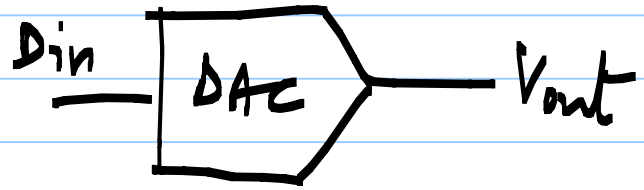


$D_{out} = k$ if

$$\frac{V_{ref}}{2^N} \cdot k < V_{in} \leq \frac{V_{ref}}{2^N} \cdot k+1$$

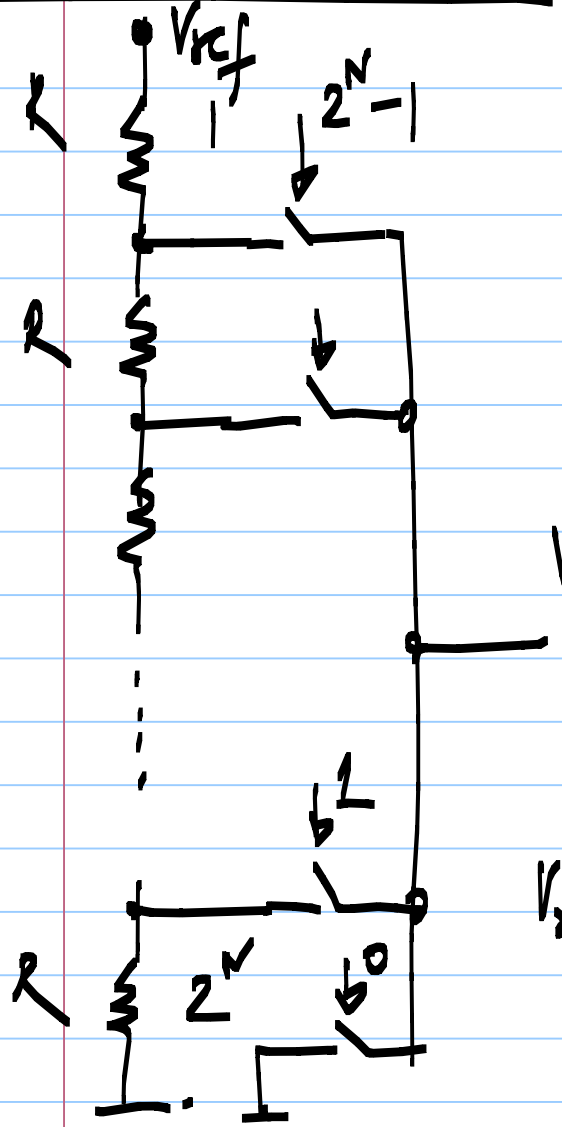
N: # bits

Digital-to-Analog (DACs)

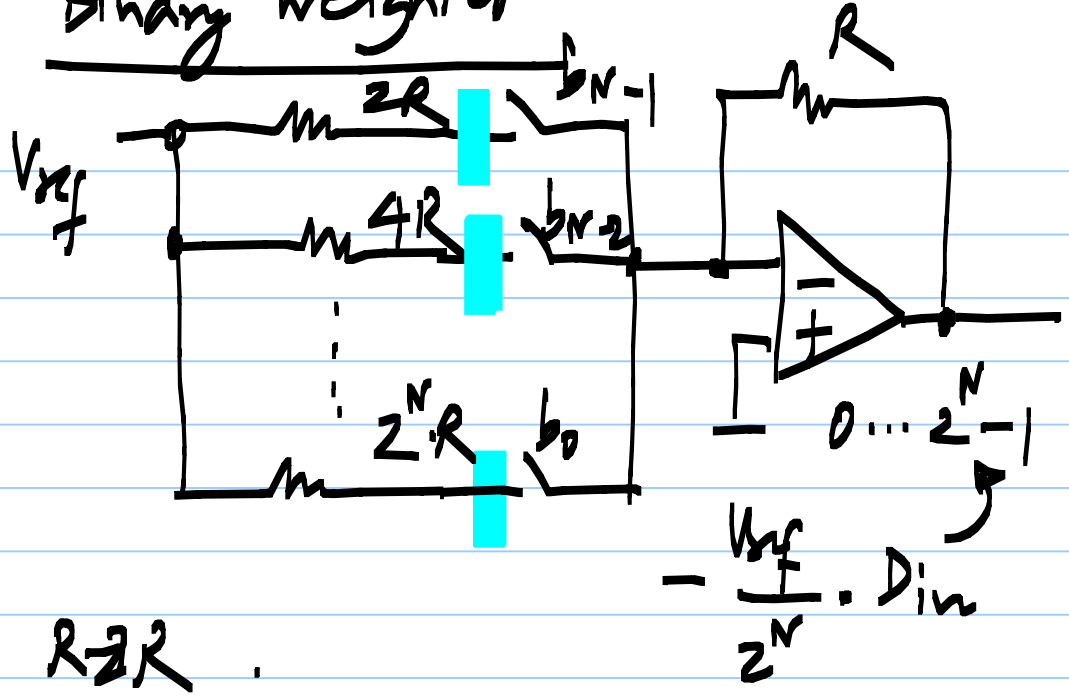


$$V_{out} = D_{in} \cdot \frac{V_{ref}}{2^N}$$

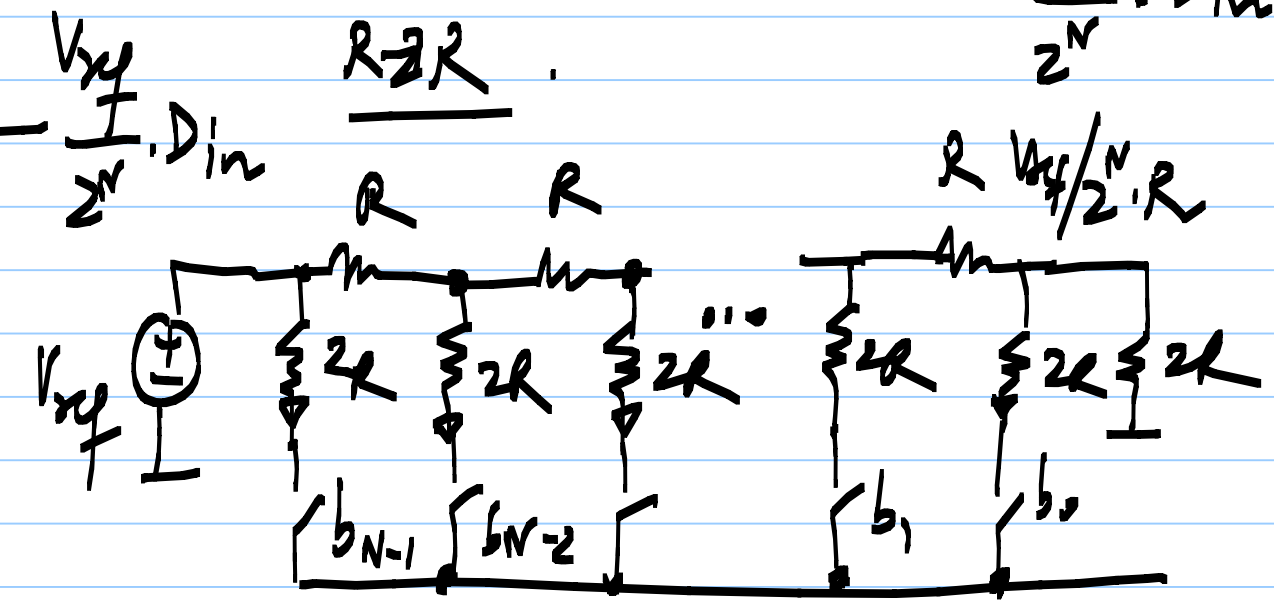
Resistor-string



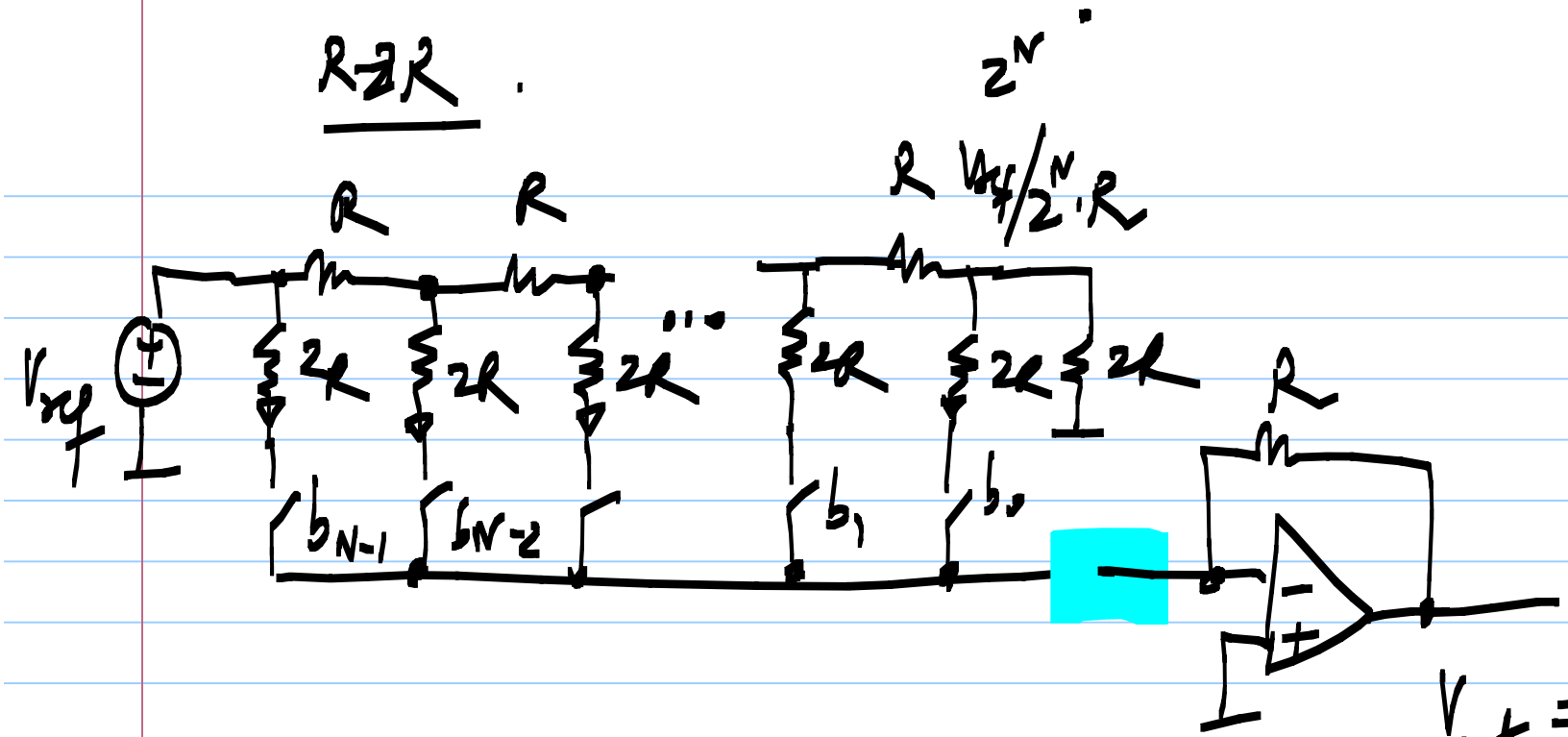
Binary weighted



R-2R



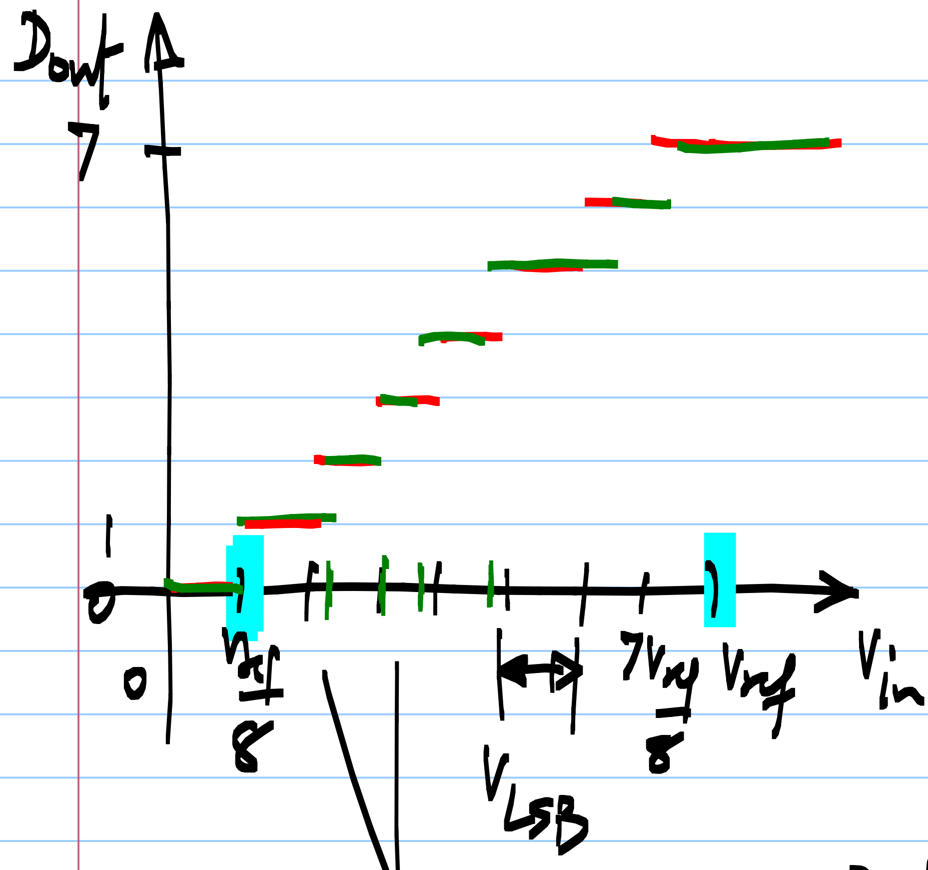
R-2R



$$V_{out} = \frac{V_{ref}}{2^N} \cdot D_{in}$$

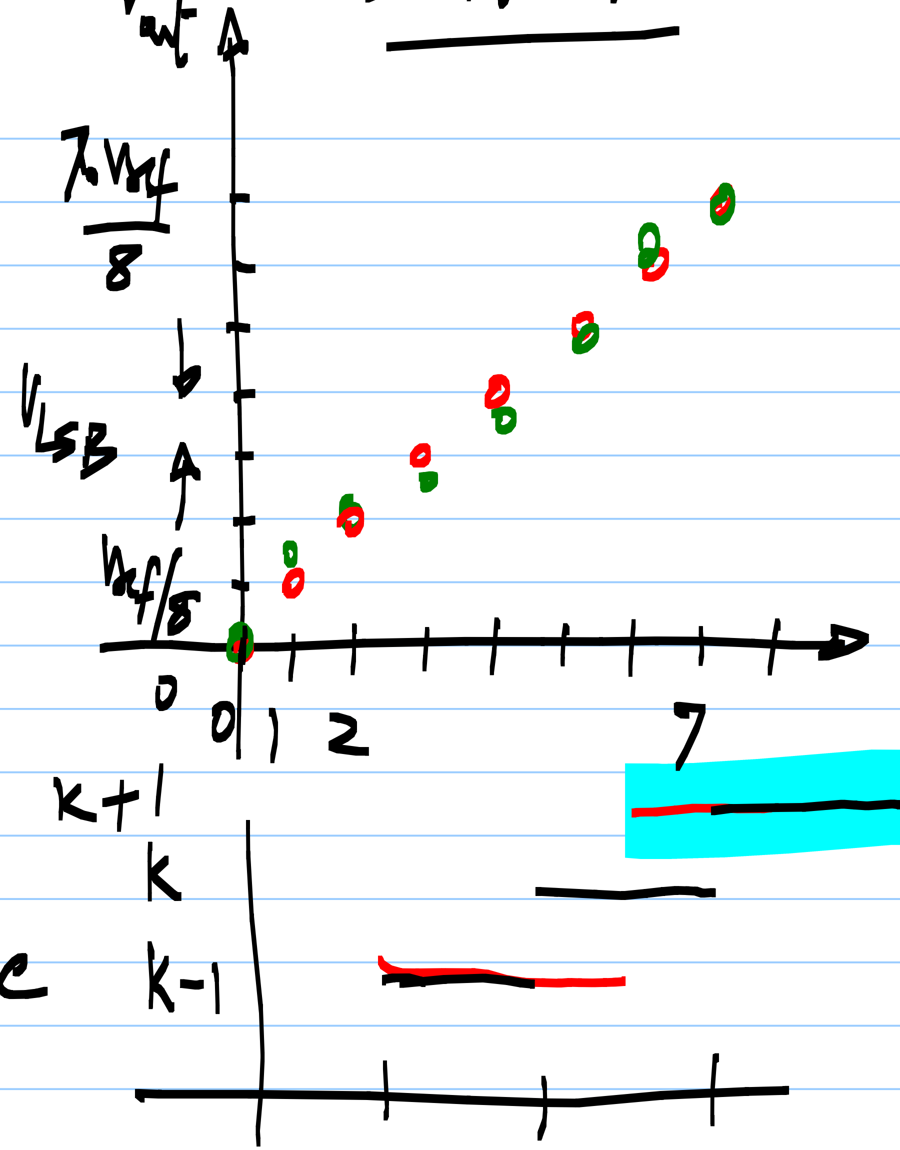
D_{in} : $b_{N-1}\ b_{N-2} \cdots b_1\ b_0$

3-bit ADC



Transition points define the ADC

3-bit DAC



All ADC transition levels move by V_{off}
All DAC output levels move by V_{off} } offset error

Equally sized steps, but different from $\frac{V_{ref}}{2^N} \neq V_{LSB}$
(V_{ref} : intended ref. voltage)

Different ref. value $V_{ref}' = V_{LSB} \cdot 2^N$ **Gain error**

Nonlinearities of ADCs & DACs

(Assume first & last values = their ideal values)

ADC transition levels: $V_{ADC}[k] \neq \frac{V_{ref}}{2^N} \cdot k$

output changes from k-1 to k if V_{in} crosses $V_{ADC}[k]$

Integral nonlinearity (INL) error: $\frac{V_{ADC}[k] - \frac{V_{ref}}{2^N} \cdot k}{V_{ref}/2^N}$

If INL < ½ LSB, no missing steps

Differential nonlinearity error (DNL)

$$DNL[k] = \frac{V_{ADC}[k] - V_{ADC}[k-1] - V_{ref}/2^N}{V_{ref}/2^N}$$

If $DNL[k] < 0.5$ LSB for all k, no missing steps

$$INL[k] = \frac{V_{ADC}[k] - \frac{V_{ref}}{2^N} k}{V_{ref}/2^N}$$

$$DNL[k] = INL[k] - INL[k-1]$$

Static errors

ADC
DAC
3
+
-