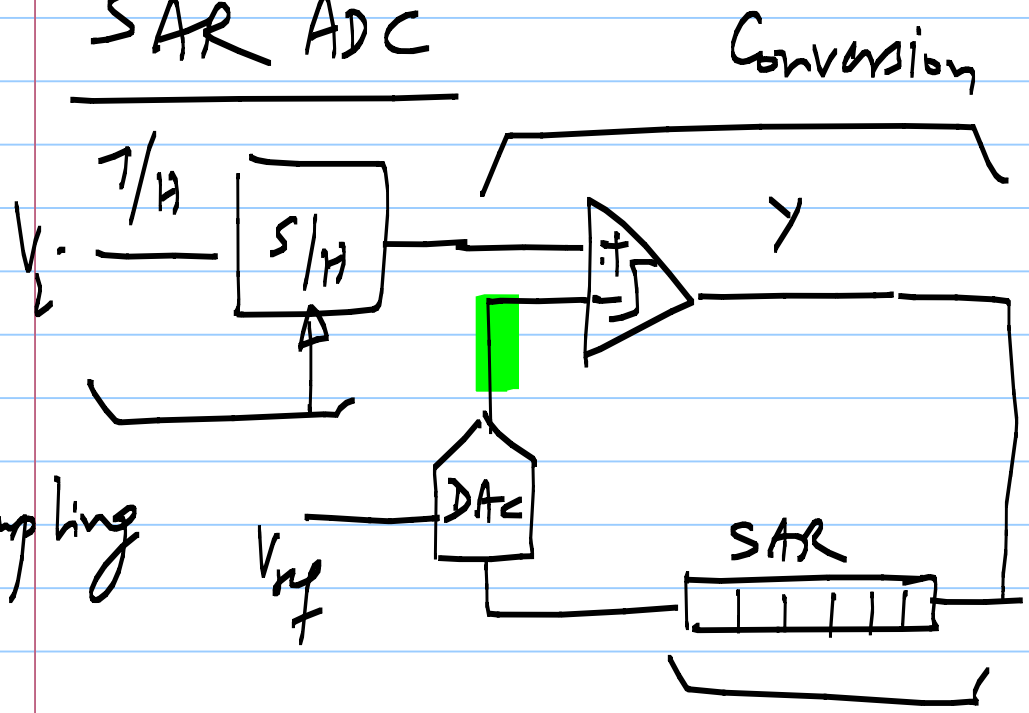
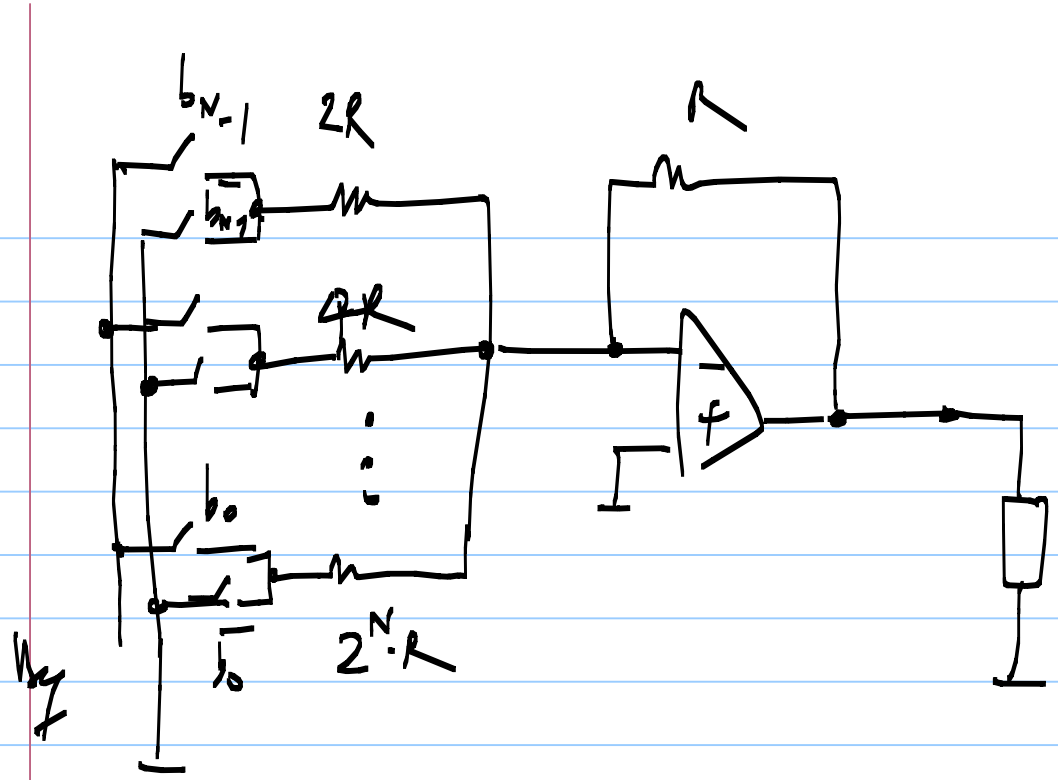
EE 2019 ADC, DAC 18/4/2017

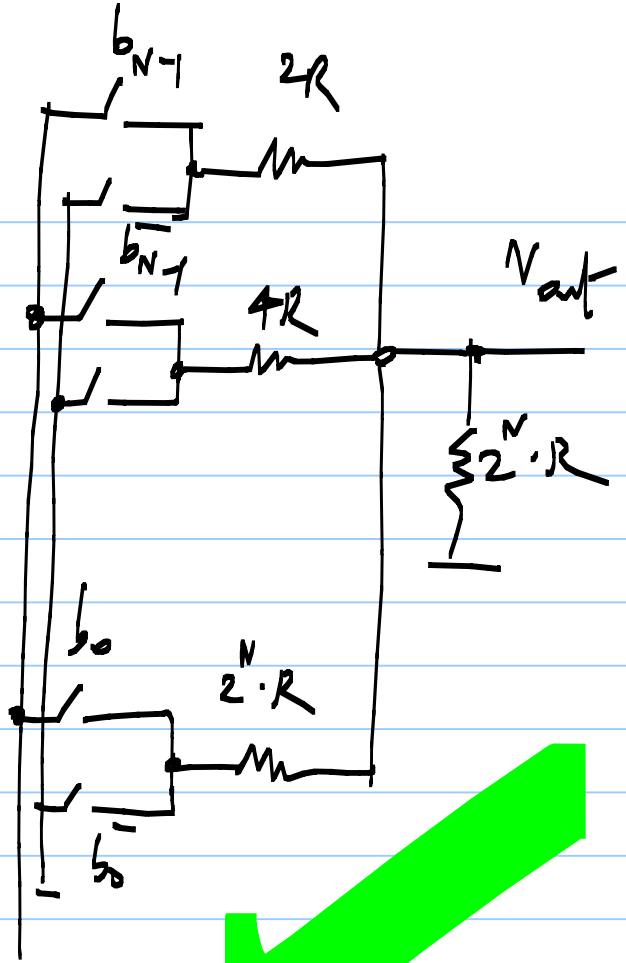
SAR ADC



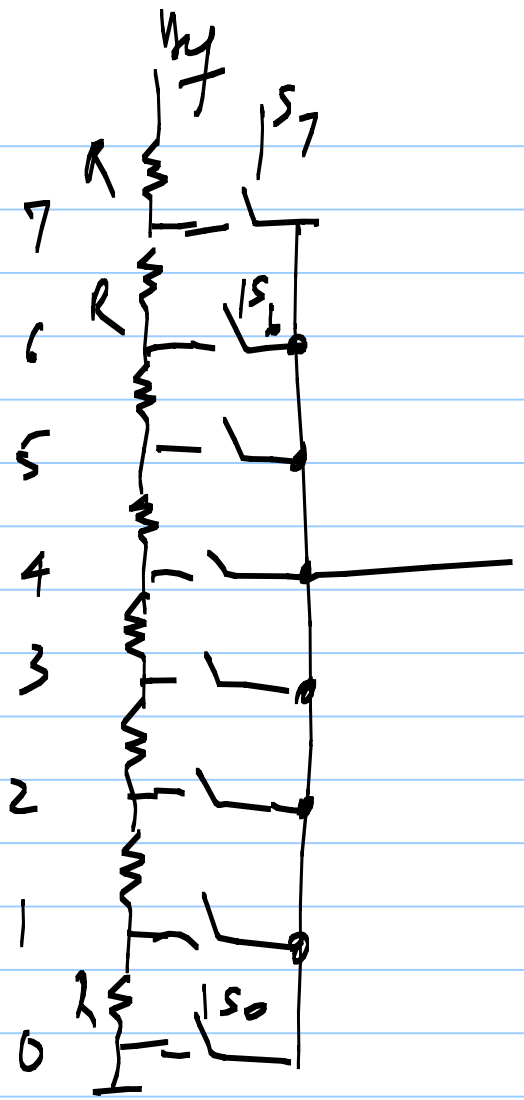
Sampling

N-steps for N-bit ADC





Binary weighted resistor-based DACs

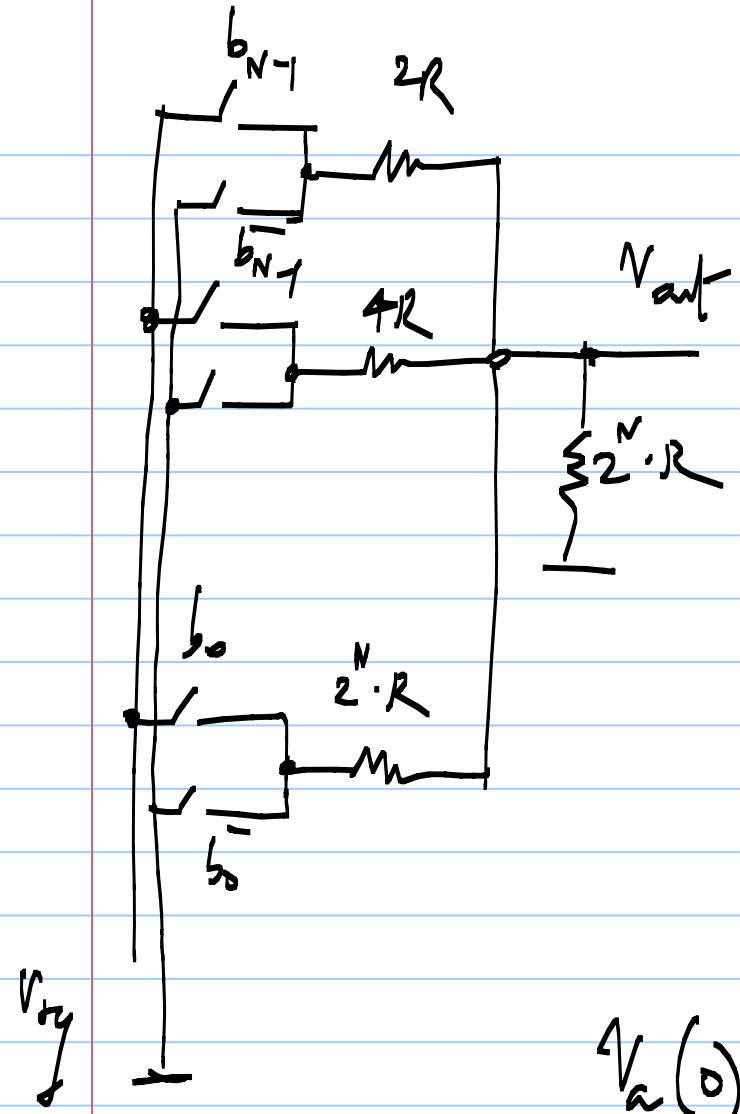


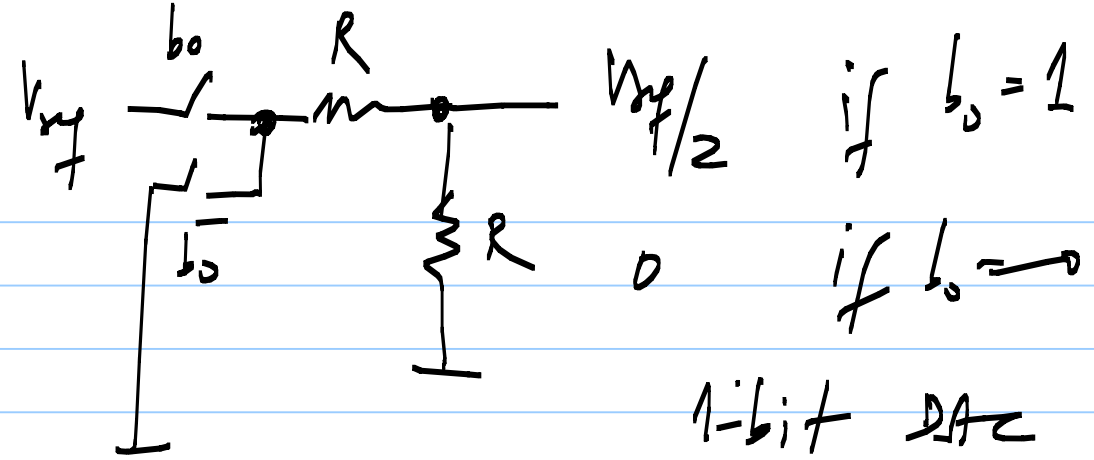
Binary inputs: $b_2 b_1 b_0$

$S_7 = b_2 \cdot b_1 \cdot b_0$

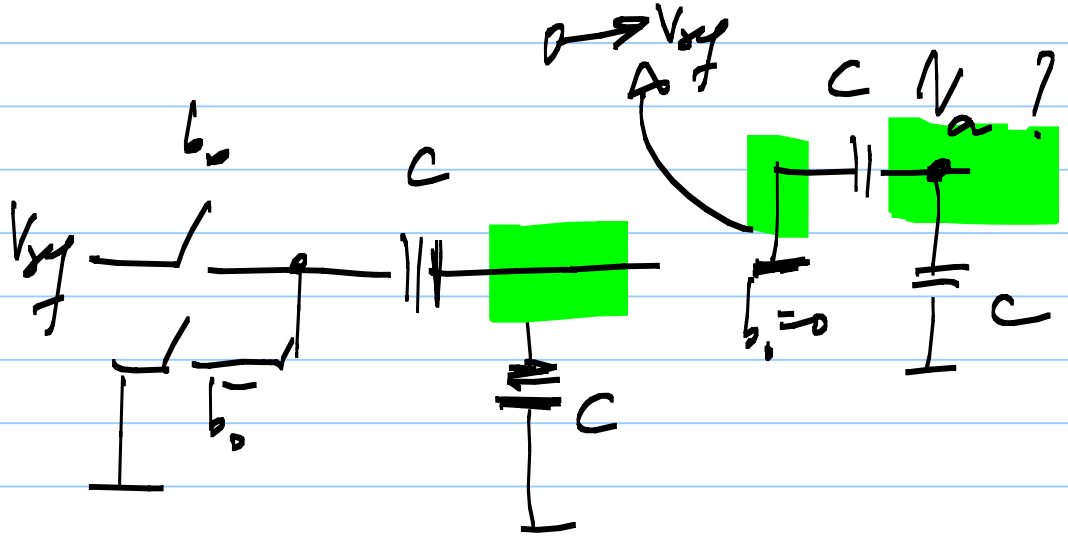
$S_6 = b_2 \, b_1 \cdot \overline{b_0}$

$S_0 = \overline{b_2} \, \overline{b_1} \, \overline{b_0}$

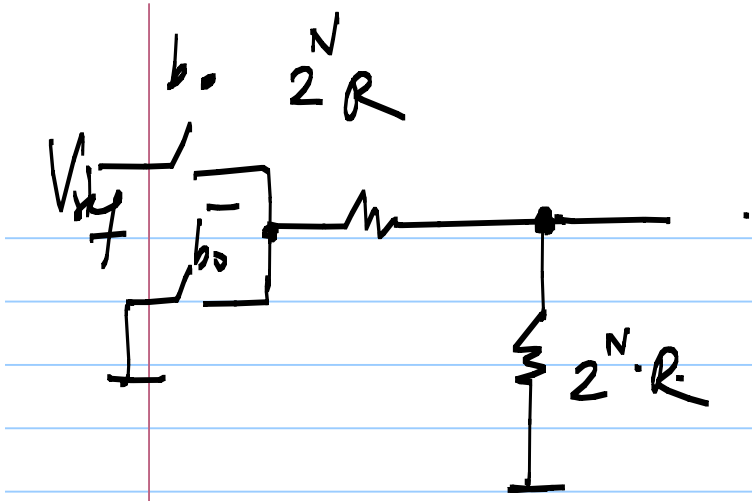


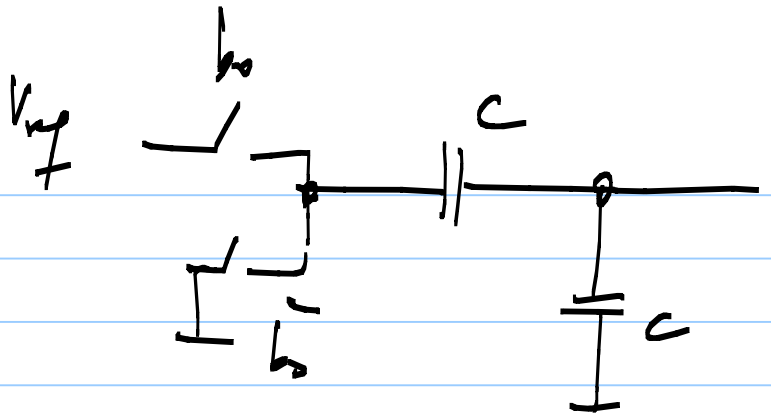


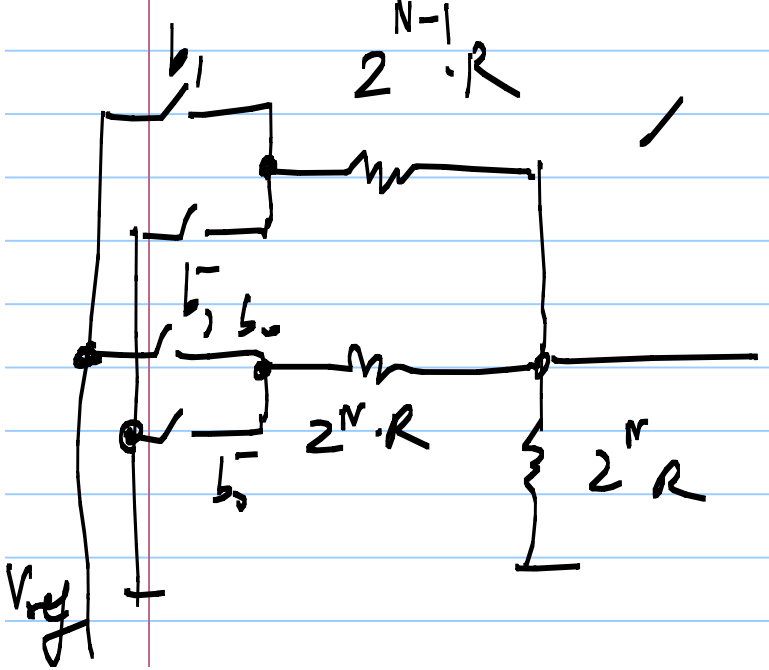
1-bit DAC

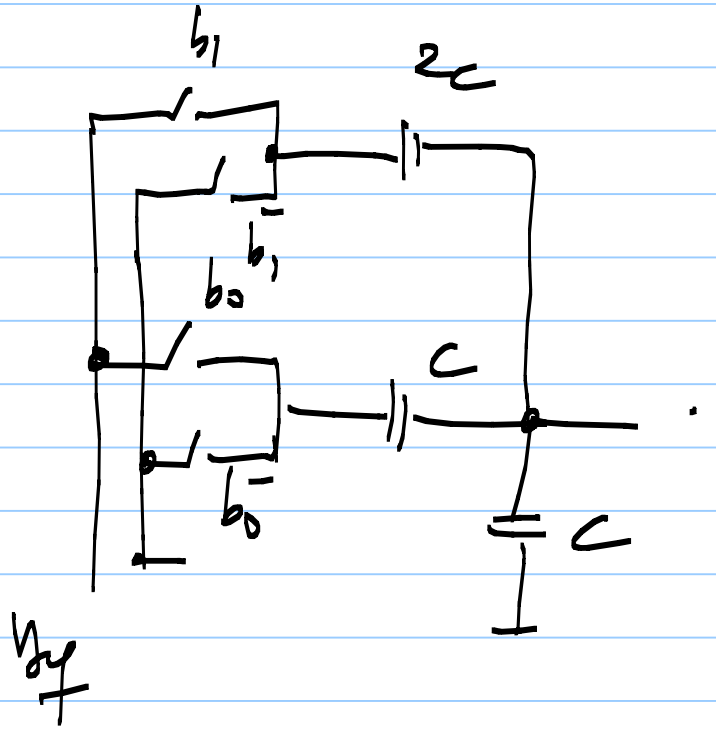


$V_a(0) = V_0$; $b_0 = 1 \Rightarrow V_a \to \frac{V_{ref}}{2}$


b_0
$2^N R$
V_{ref}
b_0
$2^N \cdot R$


b_0
V_{ref}
C
$\bar{b}_0$
C


b_1
$2^{N-1} \cdot R$
$\bar{b}_1$ b_0
$2^N \cdot R$
$\bar{b}_0$
$2^N R$
V_{ref}


b_1
2C
$\bar{b}_1$
b_0
C
$\bar{b}_0$
C
V_{ref}

V_{in}
V_{REF}
0
a_5
a_4
a_1
a_0
$2^{N-1}C$
$2C$
C
C
$2^N C$
SOC
$V_{out} = V_{in} + \sum_{k=0}^{N-1} b_k \cdot \frac{V_{REF}}{2^{N-k}}$