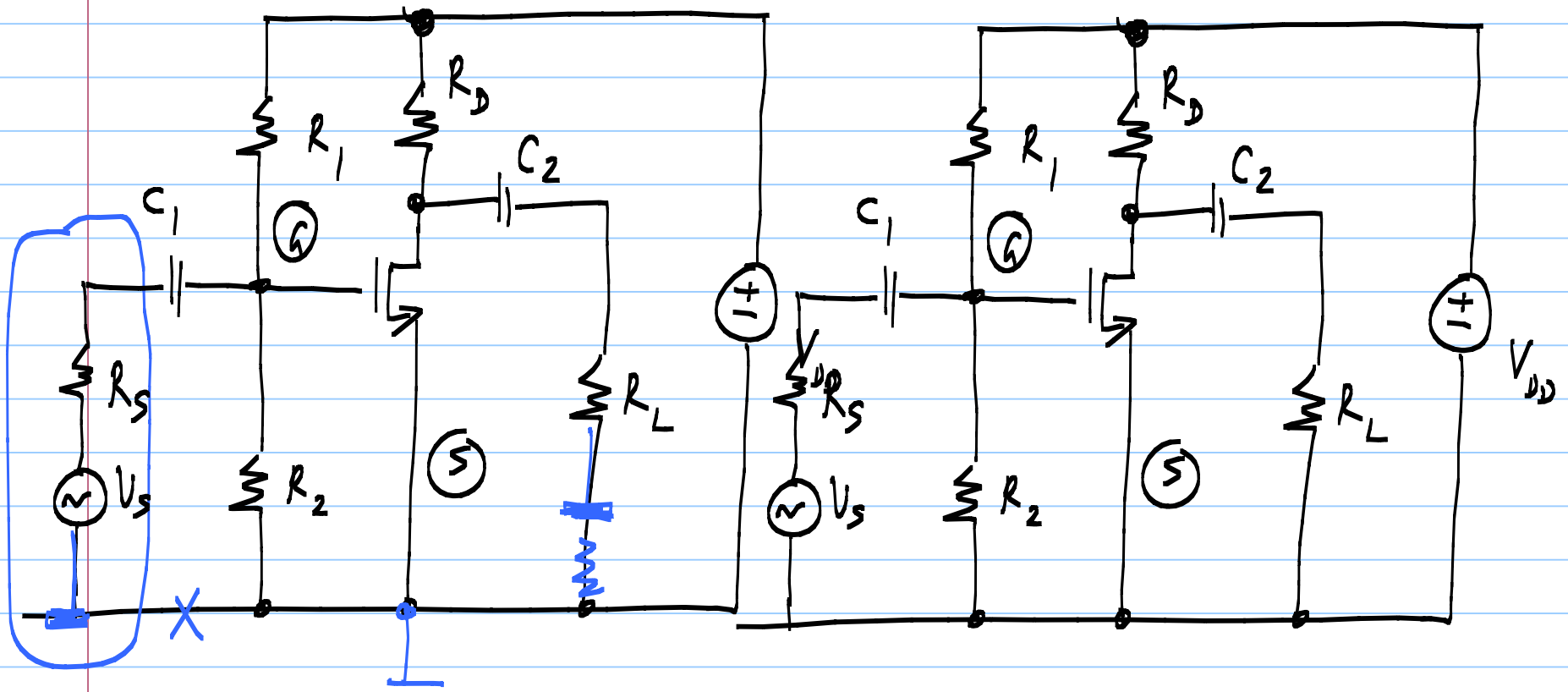
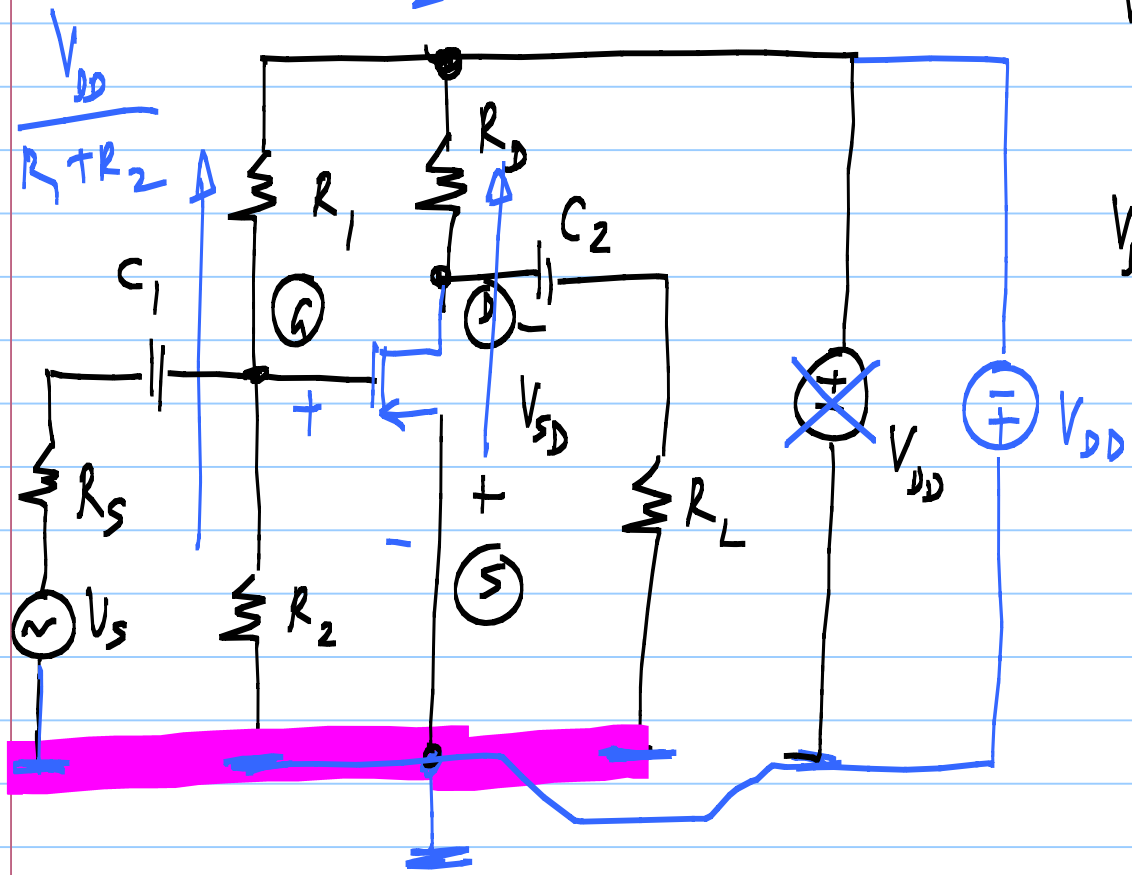
Lecture 27: pMOS transistor circuits

$$K_p = K_n \qquad \mu_p C_{ox}\left(\frac{W}{L}\right)_p = \mu_n C_{ox}\left(\frac{W}{L}\right)_n \qquad V_{Tp} = V_{Tn}$$



$\frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_T)^2$



nMOS

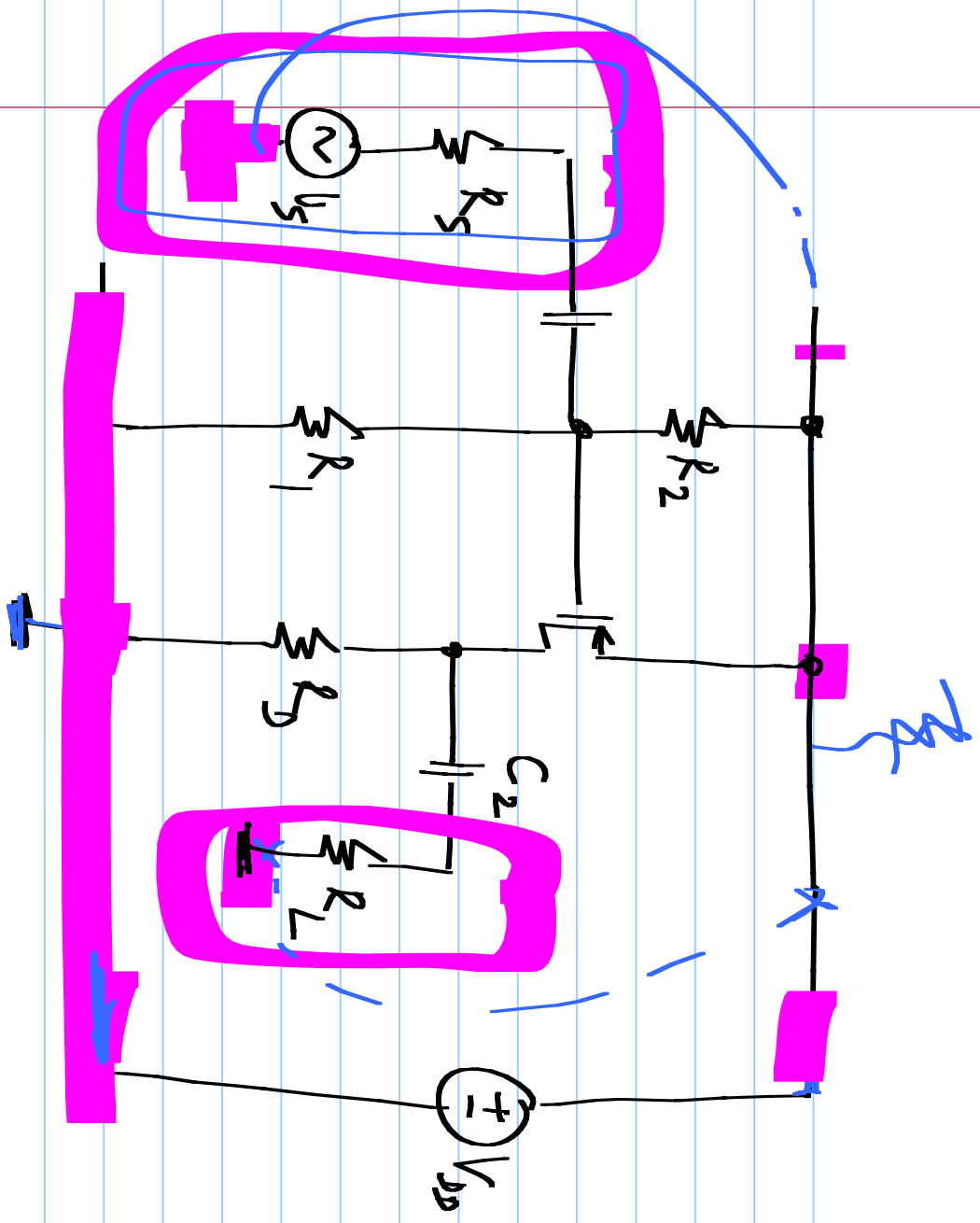
$V_{GS} = V_{DD} \cdot \frac{R_2}{R_1+R_2}$

$V_{DS} = V_{DD} - I_{D_Q} \cdot R_D$

pMOS

$V_{SG} = V_{DD} \cdot \frac{R_2}{R_1+R_2}$

$V_{SD} = V_{DD} - I_{D_Q} \cdot R_D$


R_S
R_1
R_2
R_3
C_2
R_L
V_DD

swing limits reversed

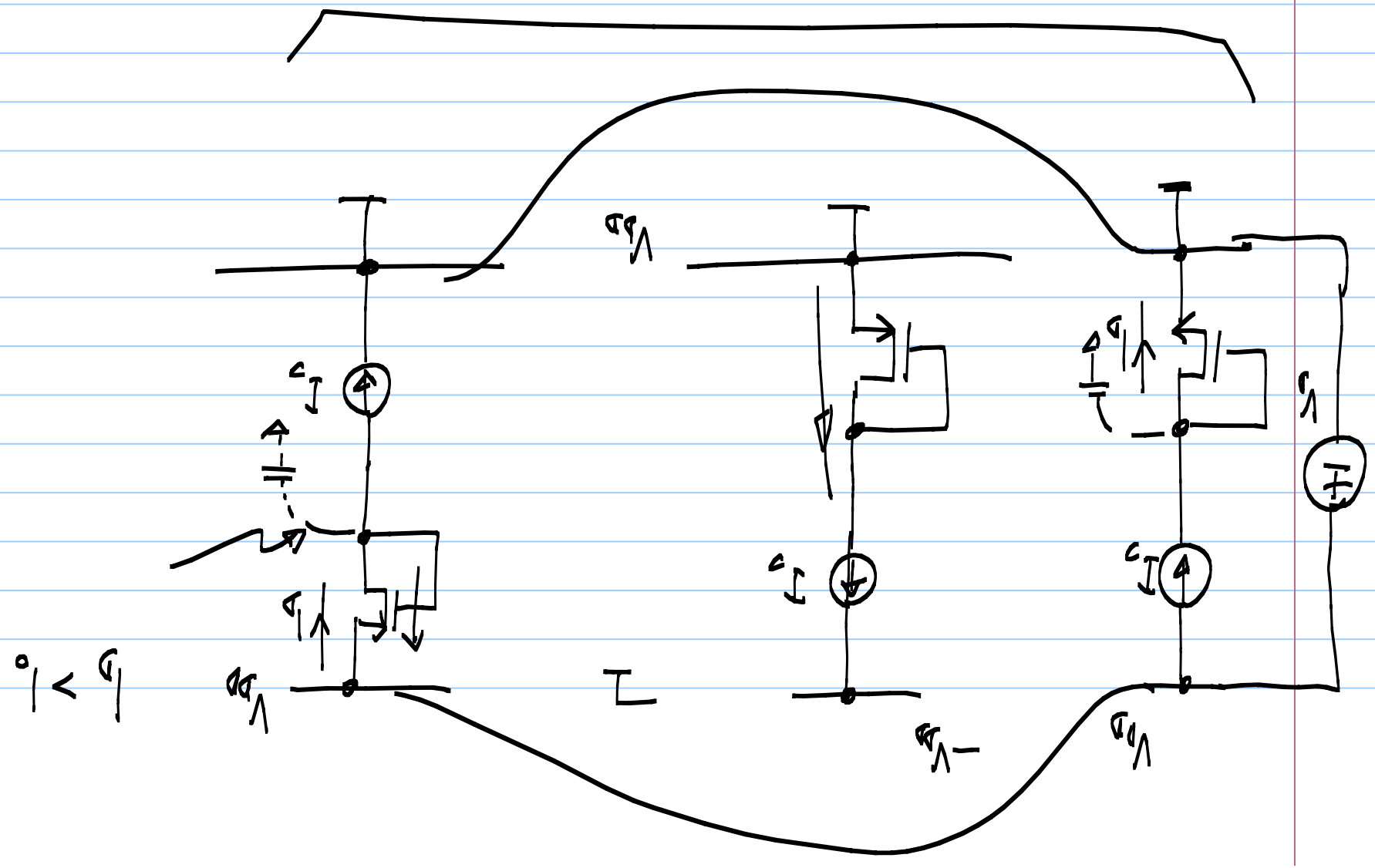
Converting nMOS circuits to pMOS

* substitute nMOS with pMOS
* Invert the polarity of all biasing sources (V_{DD}, I_b etc.)

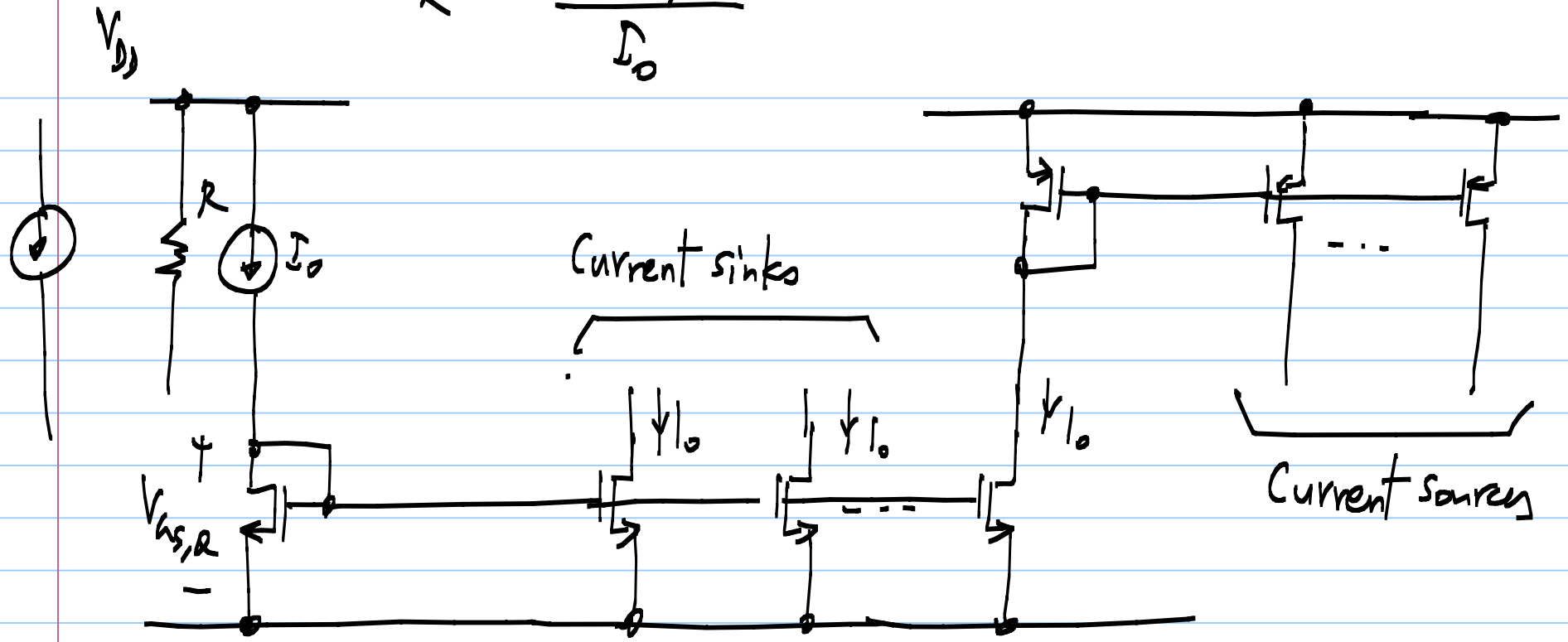
Running pMOS & nMOS circuits from common supply rails

* ~~Consider~~ Consider the lowest voltage (-ve terminal of V_{DD} -ve supply rail as ground
* Refer signal source & load to this ground

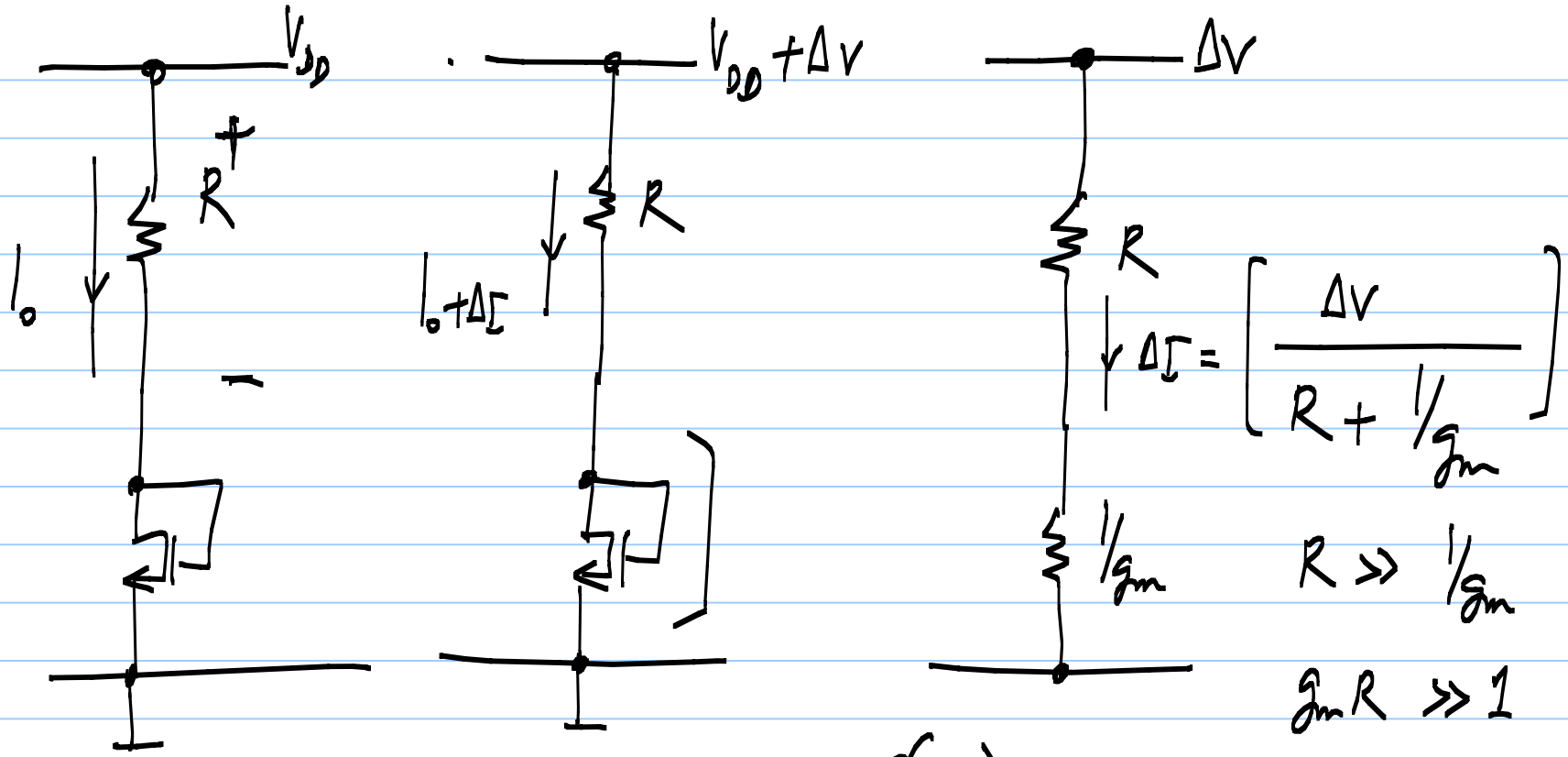
Biasing arrangements



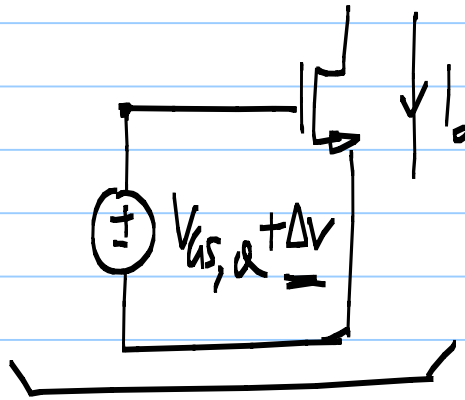
$$R = \frac{V_{DD} - V_{GS/2}}{I_0}$$



$V_T : 0$

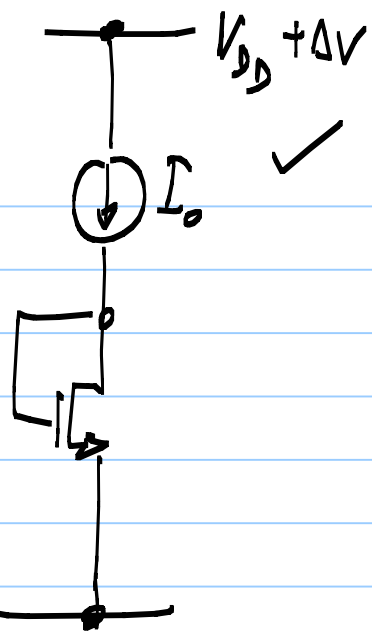


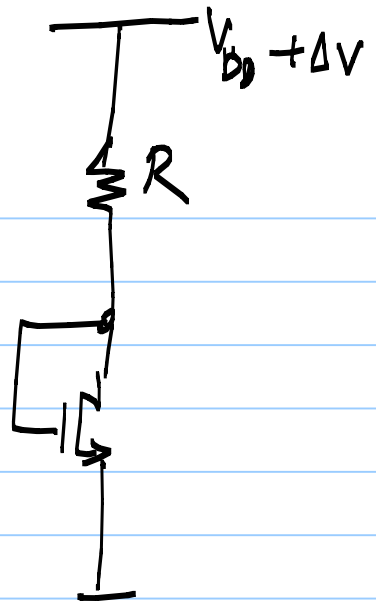
$$g_m = \frac{2I_D}{V_{GS}-V_T} \qquad \frac{2(I_D R)}{(V_{GS}-V_T)} \gg 1$$



$\Delta V \approx g_m$

$-\Delta V_f \cdot g_m$





$\Delta V \cdot \dfrac{g_m}{1+g_m R}$

$-\Delta V_f \cdot \dfrac{g_m}{1+g_m R}$