

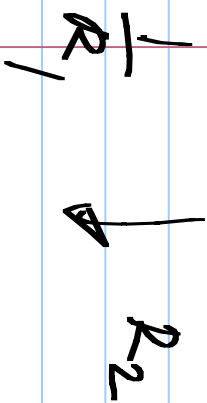
Controlled sources using opamps & transistors

$V_{CCS} + CCVS$

$VCCVS$



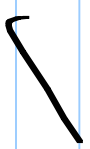
✓ (But 1x)



$VCCS$



$CCVS$

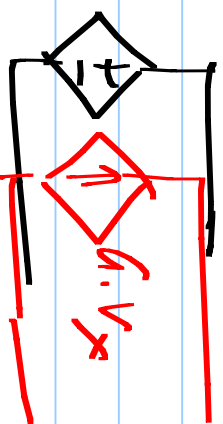
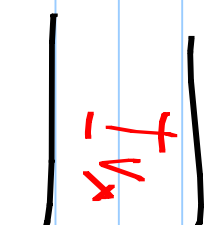
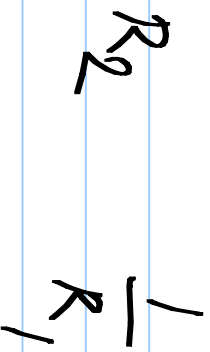


$CCVS + V_{CCS}$

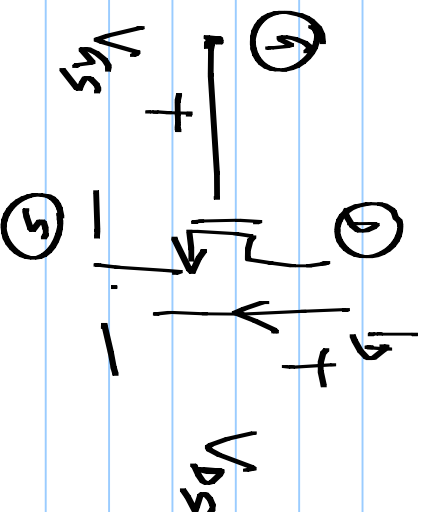
$CCCS$

$A \cdot V_x$

✓ (But 1x)

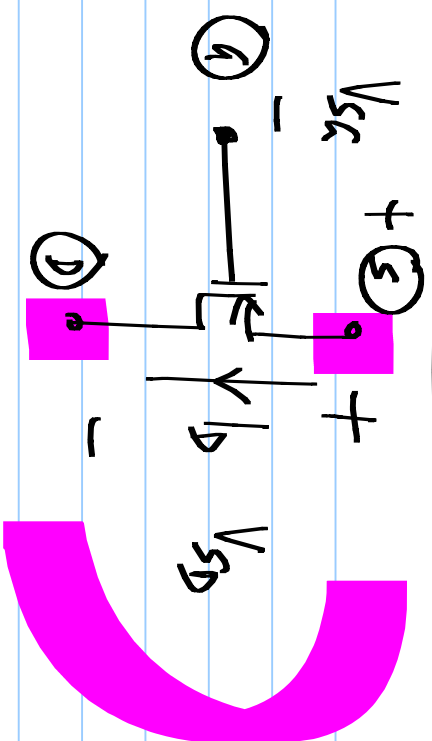


nMOS transistor



Drain Voltage can be below-threshold-like gate voltage but not by more than V_T

pMOS transistor



$$I_D = 0 \quad (\text{OFF})$$

$$V_{GS} < V_T$$

$$\frac{I_D}{\mu_n} \sim \frac{1}{3}$$

$$\mu_p C_{ox} \cdot \frac{W}{L} \left((V_{GS} - V_{TP}) V_{SD} - \frac{V_{SD}^2}{2} \right) \quad (\text{TRIODE})$$

$$V_{GS} > V_T$$

$$V_{SD} < V_{GS} - V_T$$

$$\mu_p C_{ox} \cdot \frac{W}{L} (V_{GS} - V_{TP})^2 (1 + \lambda_p V_{SD}) \quad (\text{SAT})$$

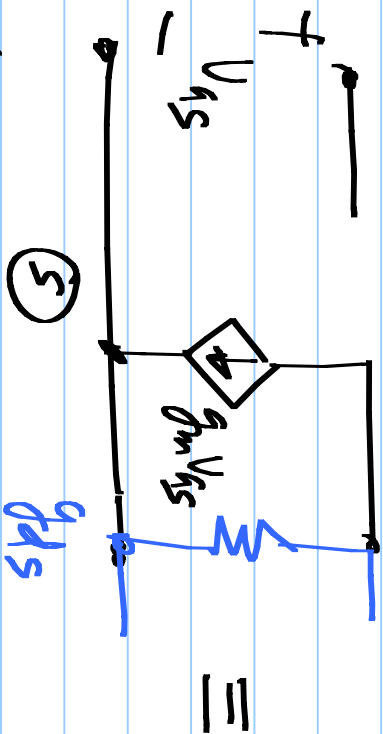
$$V_{GS} > V_T$$

$$V_{SD} > V_{GS} - V_T$$

nMOS:

④

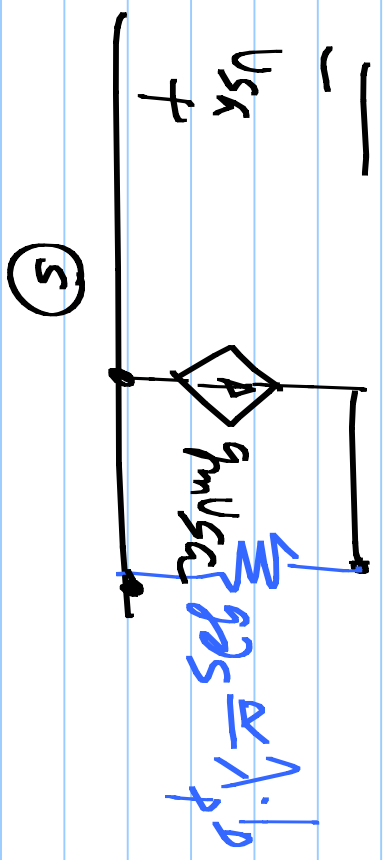
①



pMOS

④

①



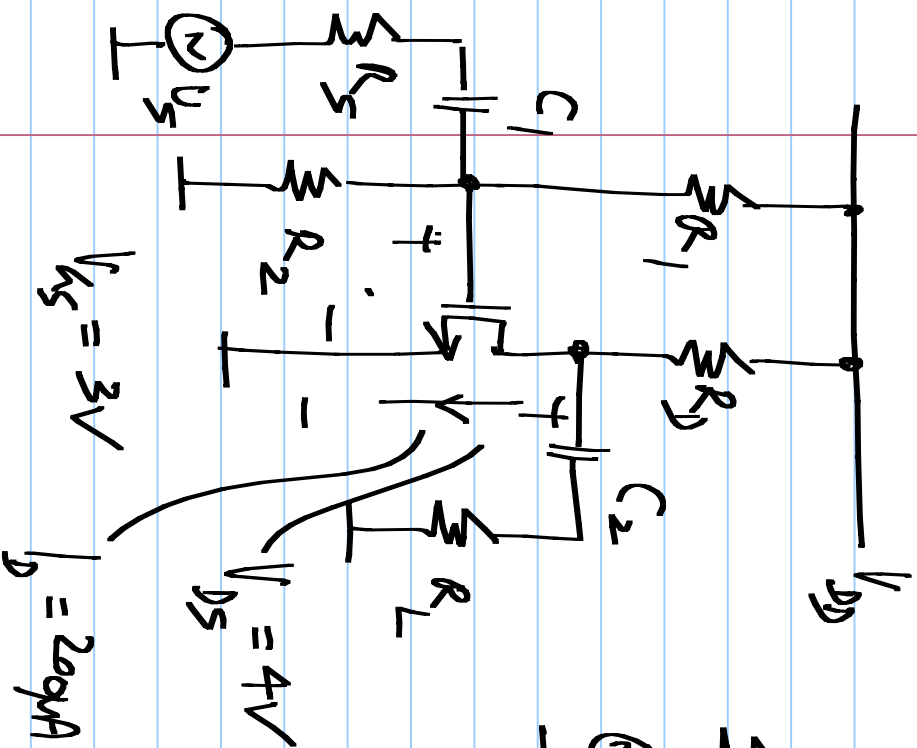
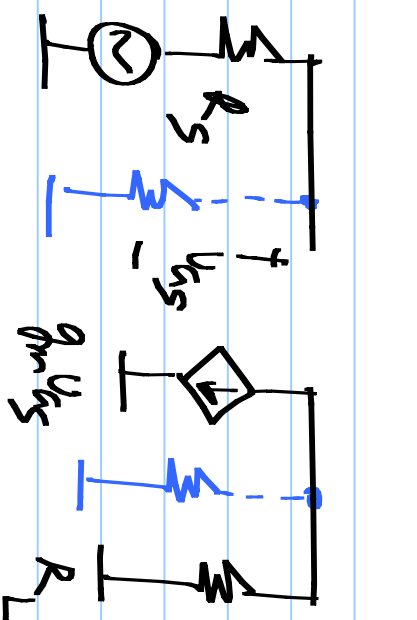
* V_{gs} increases $\Rightarrow$ negative V_{gs}

* Current flowing out of the drain increases $\Rightarrow$ negative increment into the

drain

Common source amplifier:

$$V_{S1} = 3V, V_{S2} = 4V$$



$$\frac{W_p}{L_p} = 100 \mu A / V^2$$

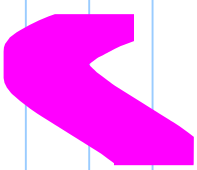
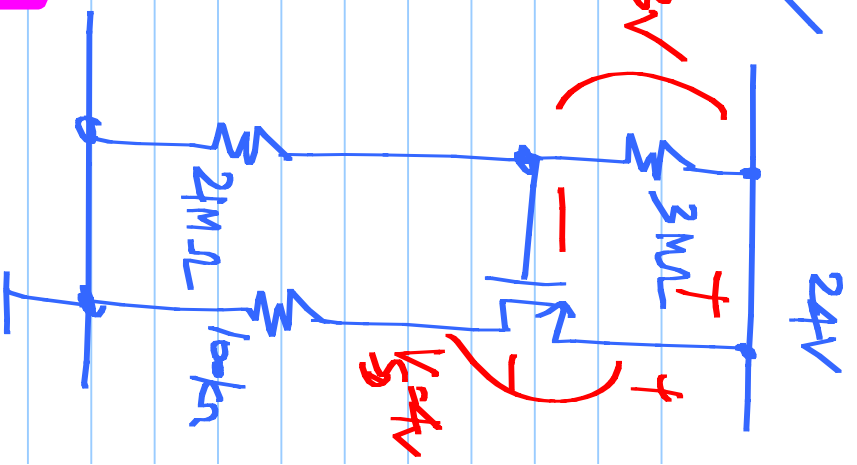
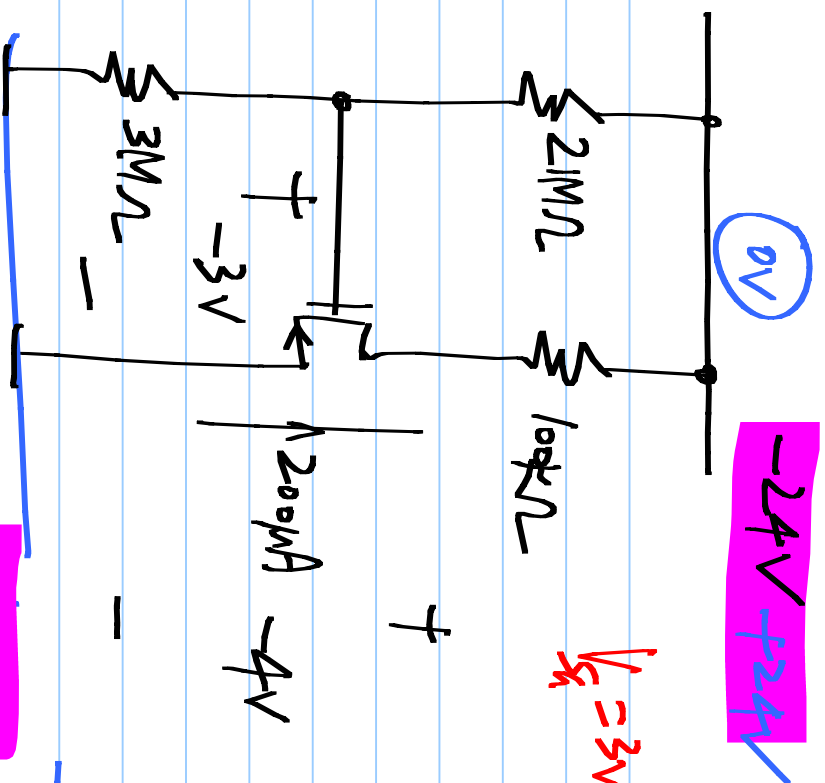
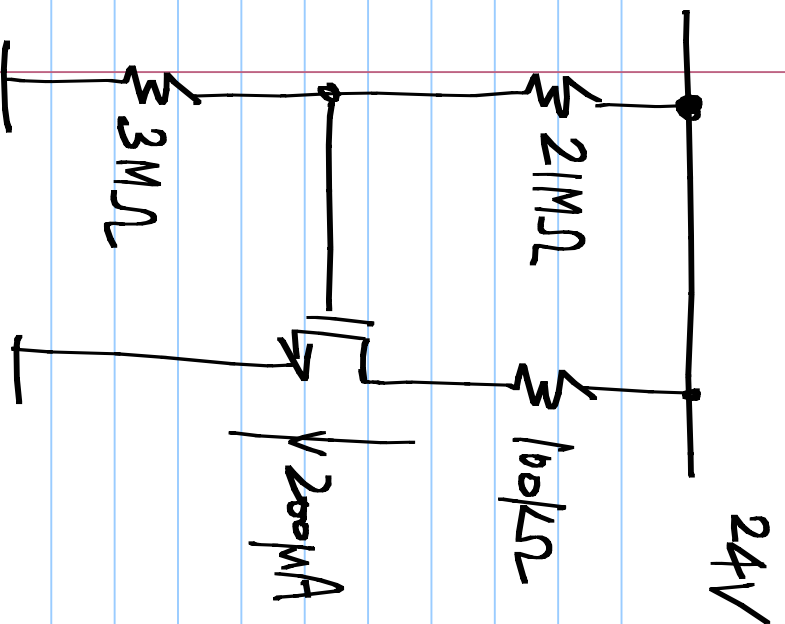
$$\frac{W_n}{L_n} = 100 \mu A / V^2$$

$$V_{Tn} = V_{Tp} = 1V$$

$$I_D = 200 \mu A$$

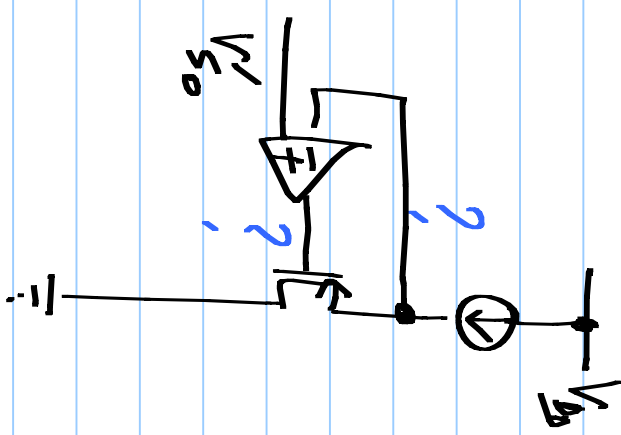
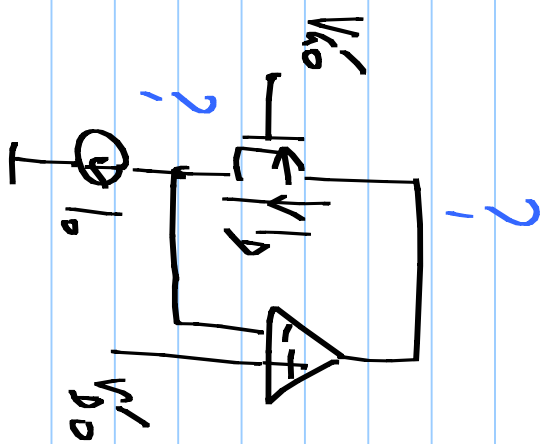
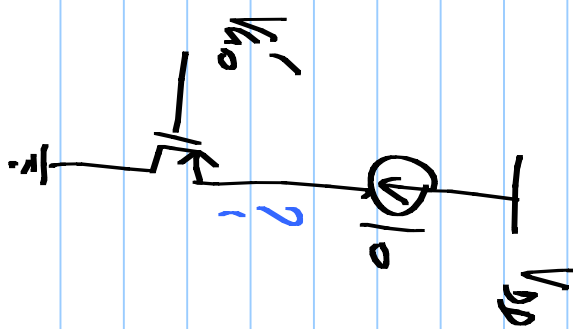
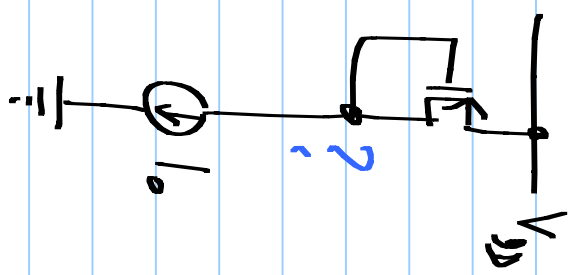
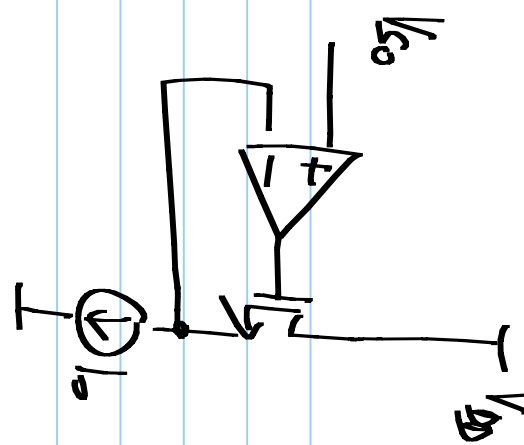
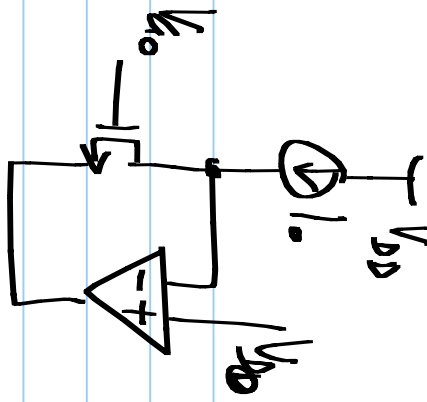
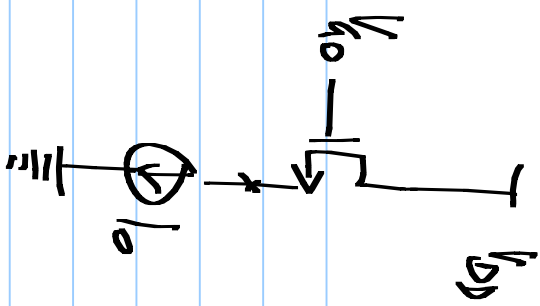
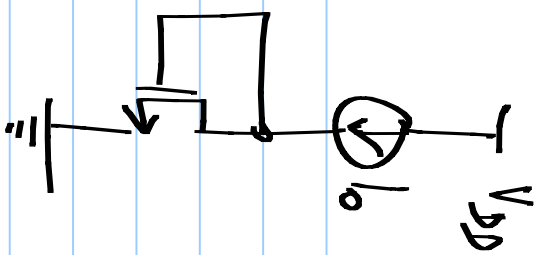
$$V_{DS} = 4V$$

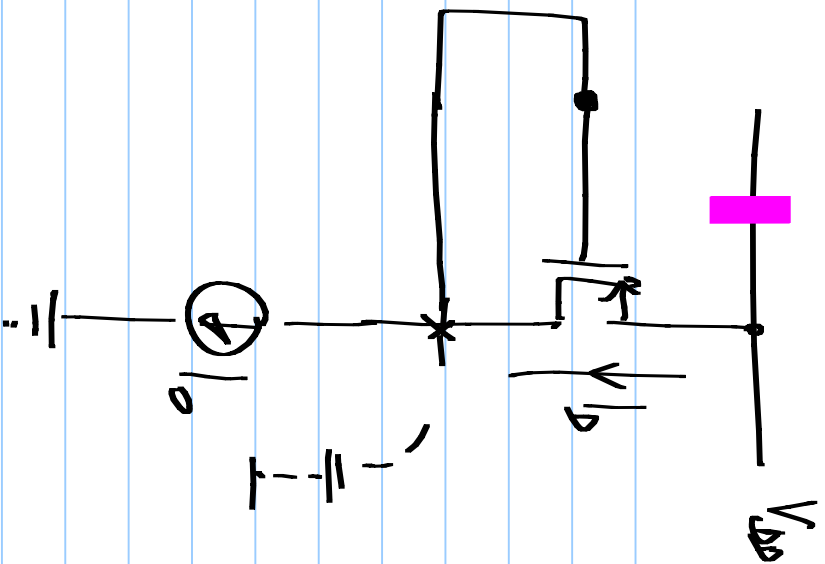
$$V_{S1} = 3V$$



$$V_{gs} = +3V$$

$$V_{gs} = +4V$$





$I_D > I_0$ V_g must be increased

V_g increases

$$V_{SD} > V_{SK} - V_T$$

$$V_{SD} = V_{SK}$$

