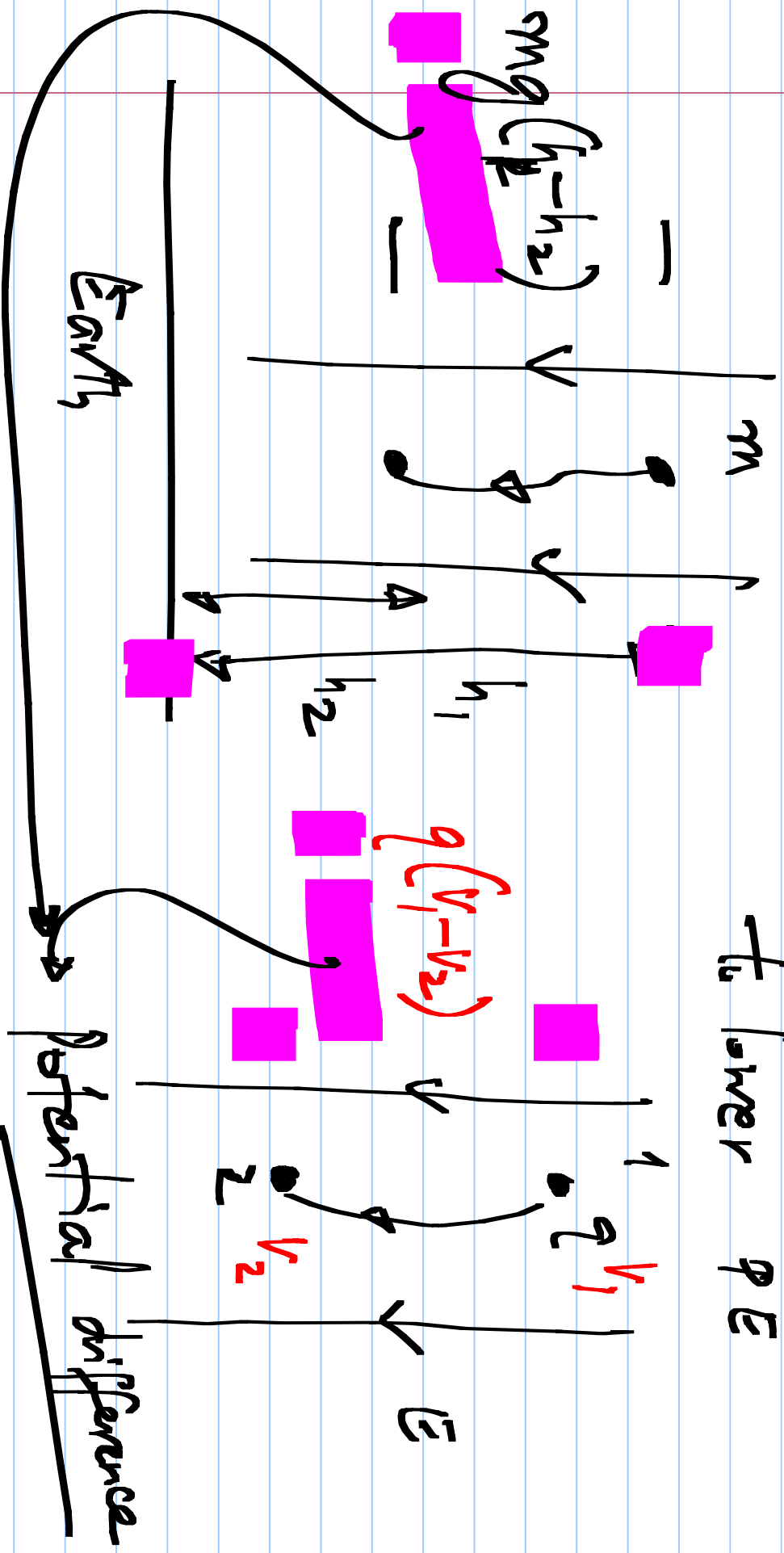


EC1010: Lecture 2

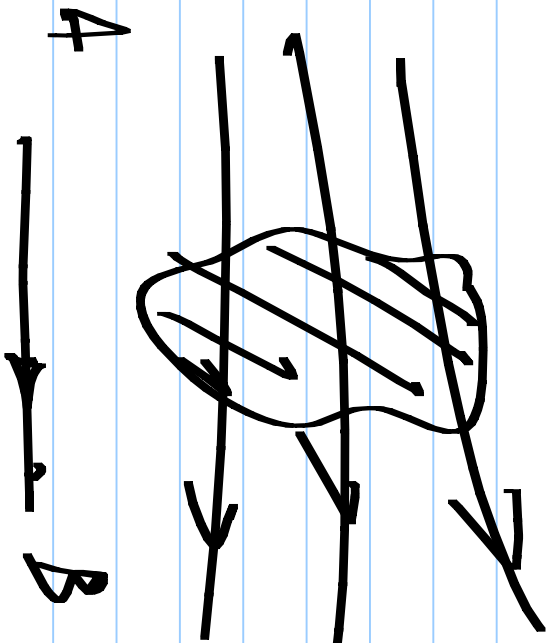
Note Title

moves from higher

to lower PE



1/16/2014



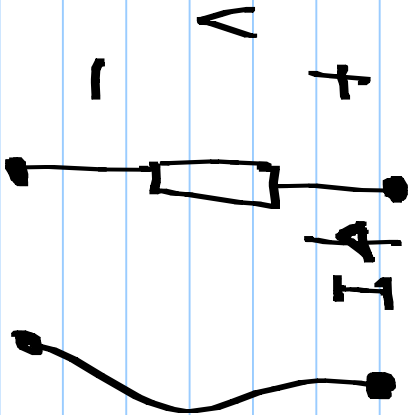
$$i = \frac{dq}{dt}$$

"Aggregated" quantities
spatially explicit
 ignored.

q — Electric current i

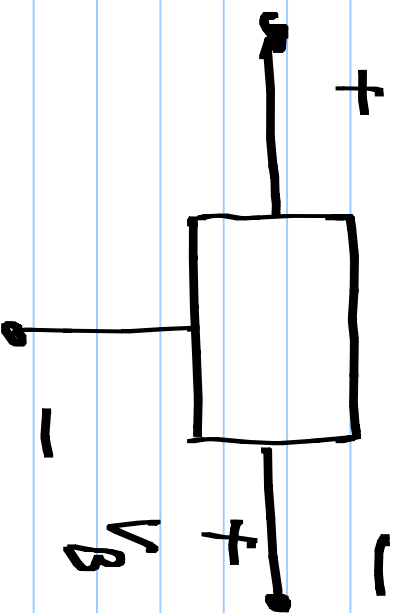
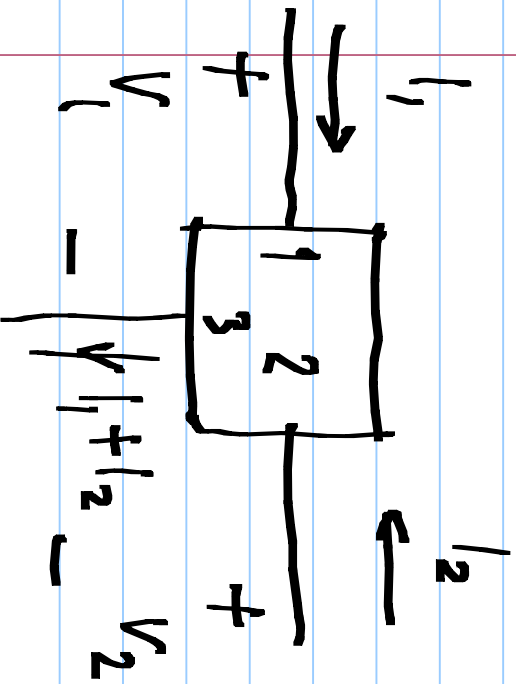
E — Potential difference (Voltage) V

Electrical elements:



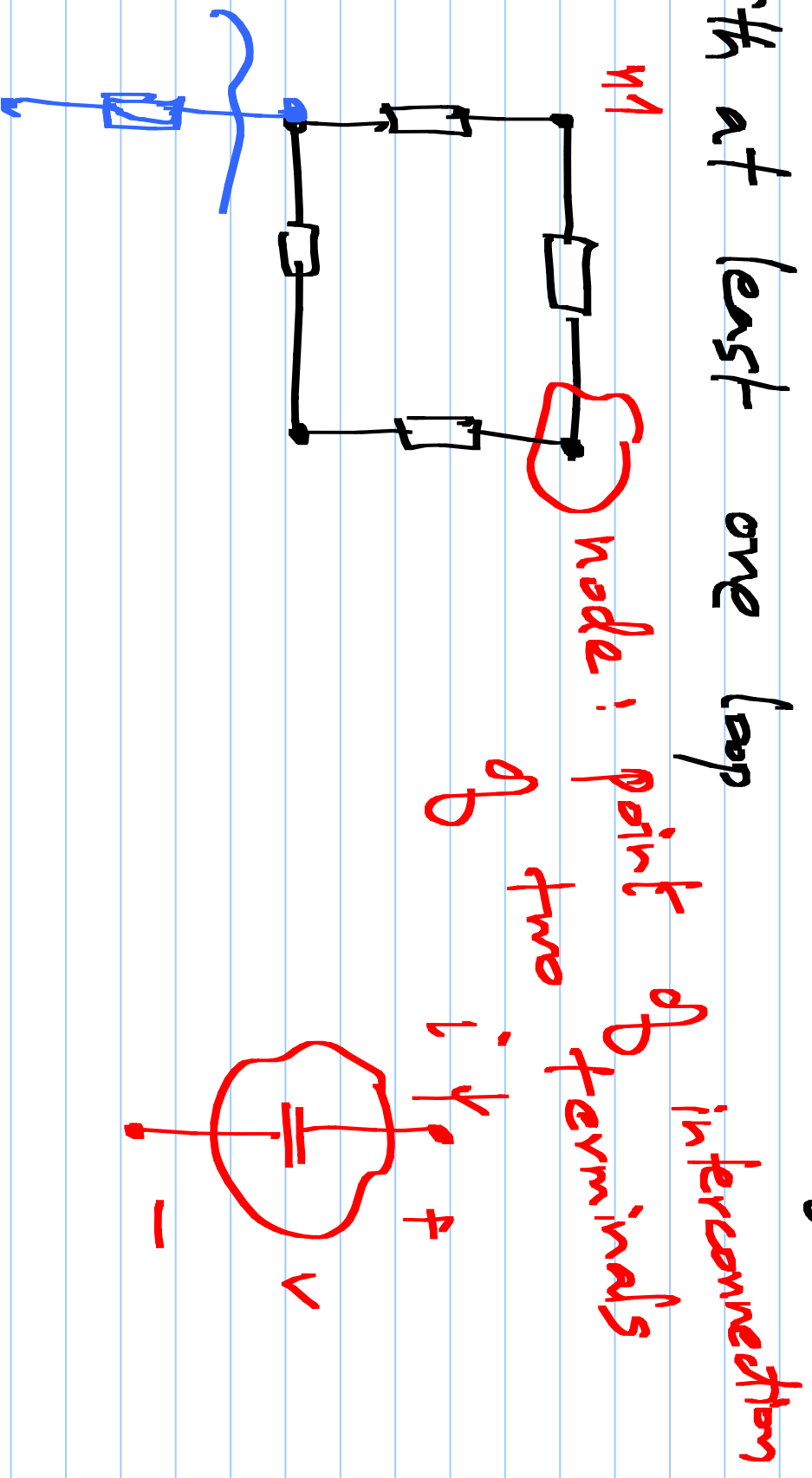
Terminals (≥ 2)

N terminals ($N-1$ currents
 $N-1$ voltages)

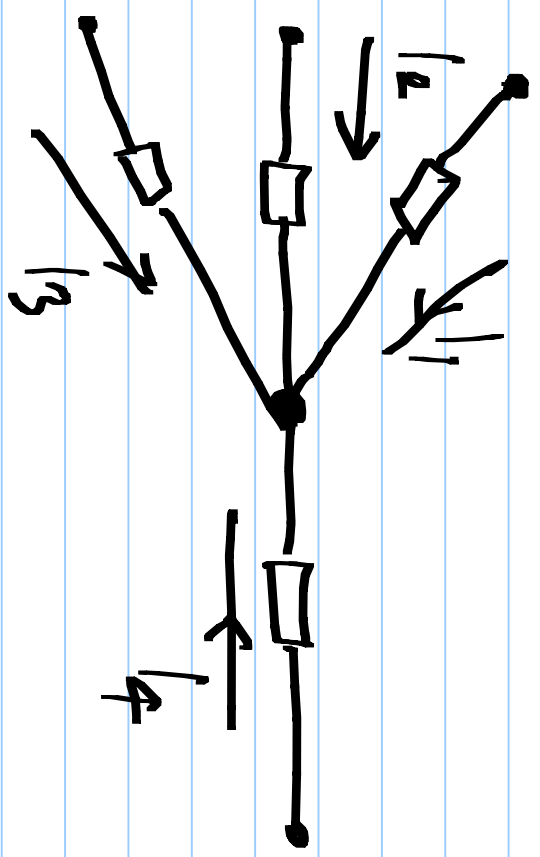


Electrical circuit : Interconnection of elements

with at least one loop



Node: point of connection of 2 or more terminals KCL

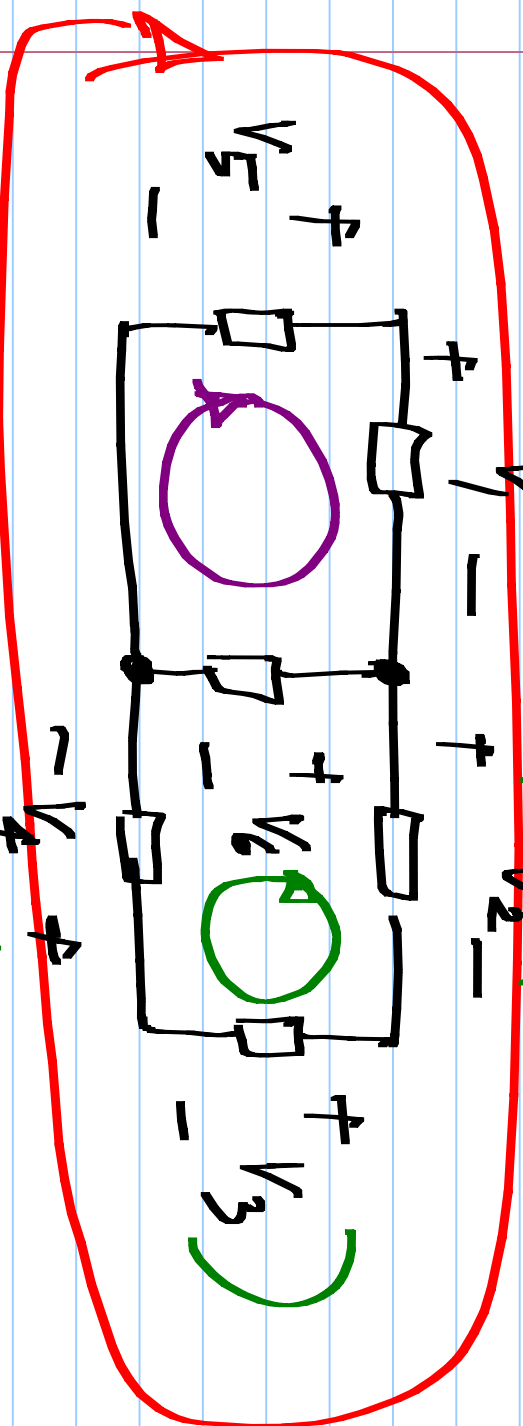


Kirchhoff's
current law

$$\sum \text{entering} = 0$$

the node

Loop: closed path formed by elements



KVL

Kirchhoff's
Voltage
Law

$$V_1 + V_6 - V_5 = 0$$

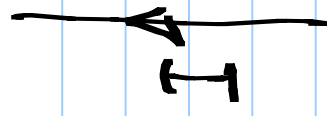
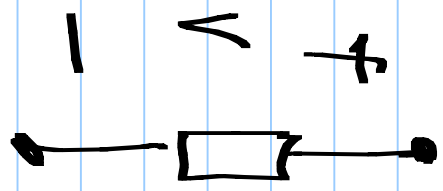
$$V_2 + V_3 + V_4 - V_6 = 0$$

$$V_1 + V_2 + V_3 + V_4 - V_5 = 0$$

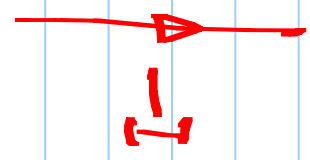
$\frac{dV}{dt}$ (negligible)

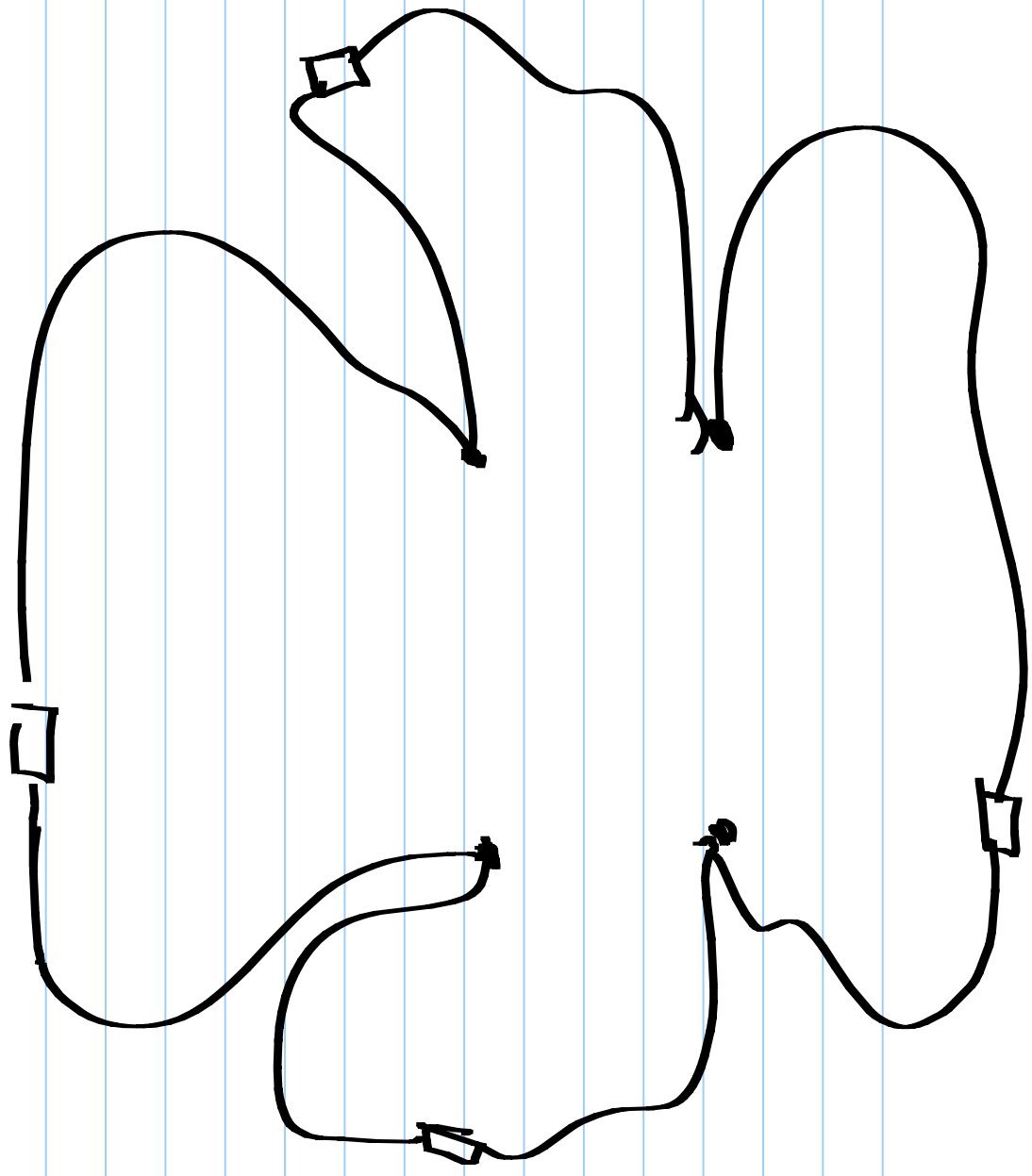
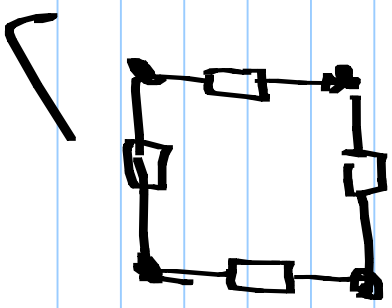
$\frac{1}{r}$

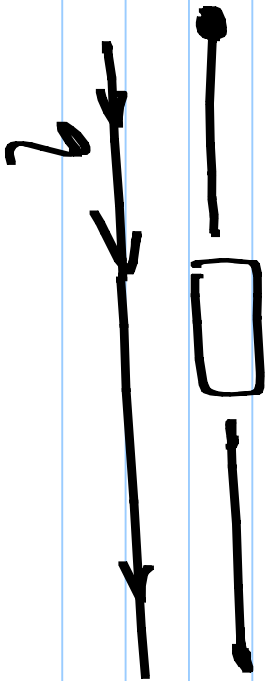
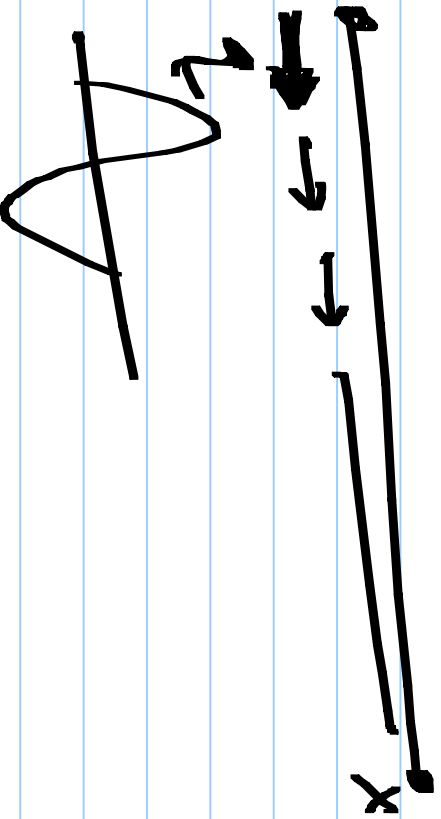
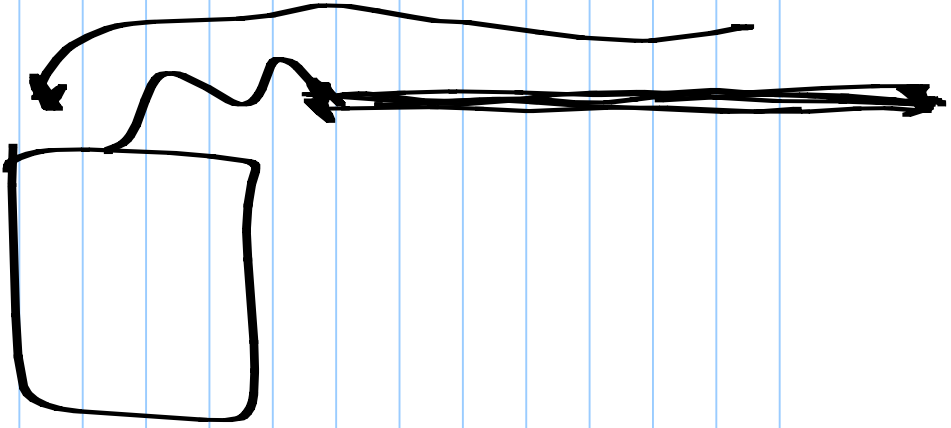
$\frac{1}{r}$



$\frac{1}{r}$



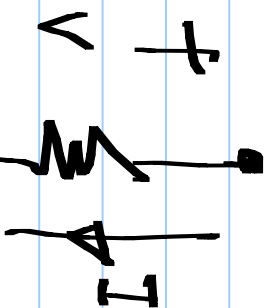
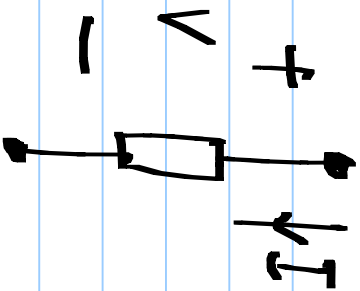




KCL, KVL: can be violated at high frequencies & for large structures

KCL, KVL: valid for all circuits

Resistor:

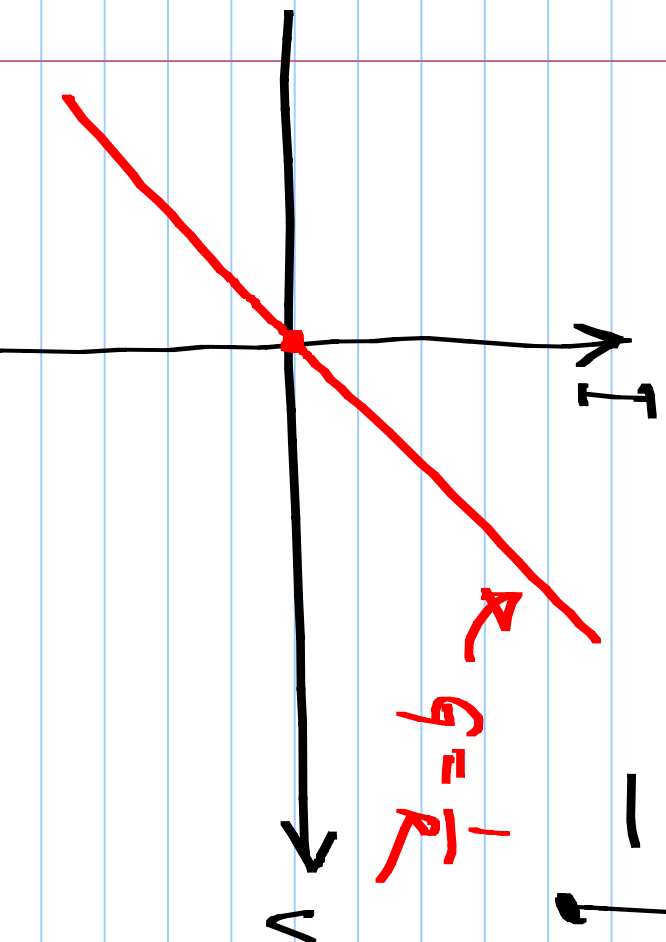


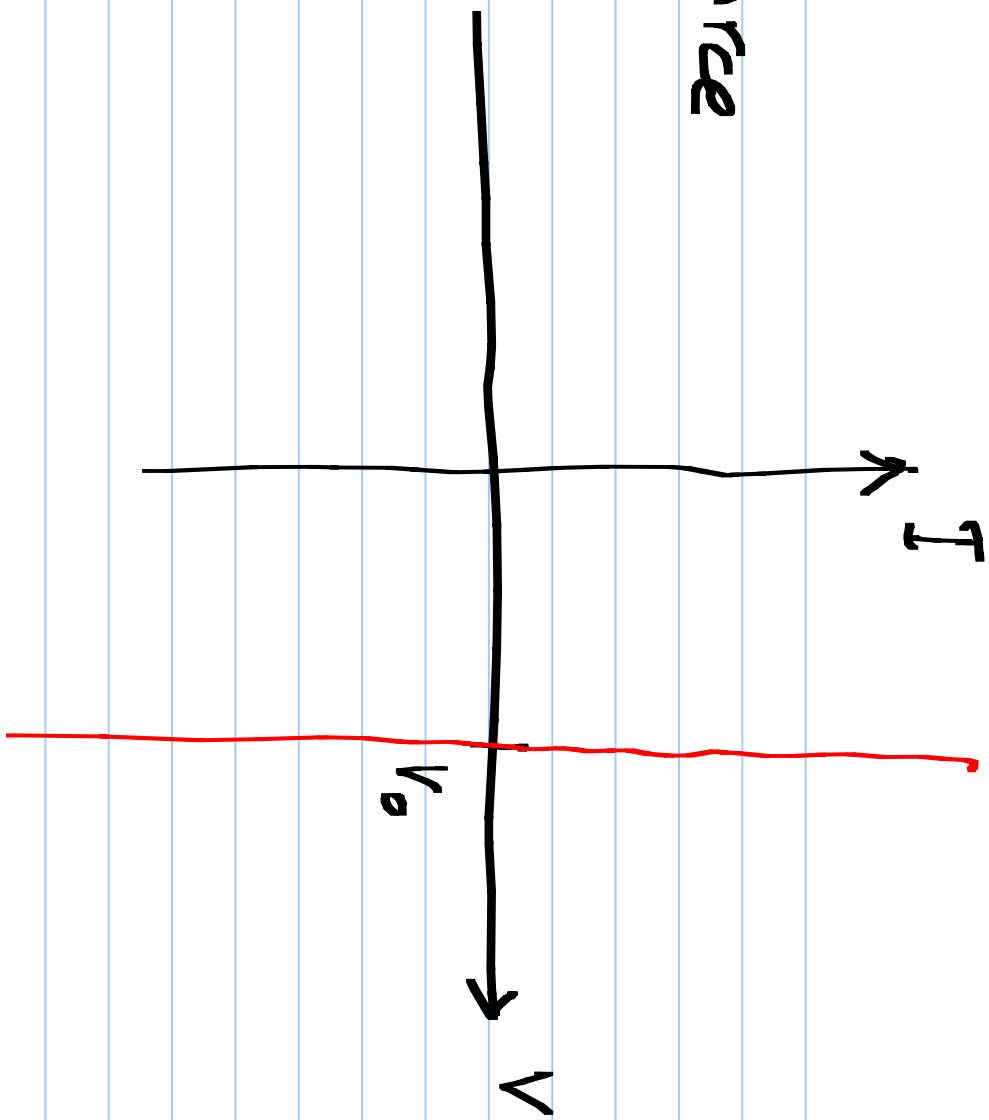
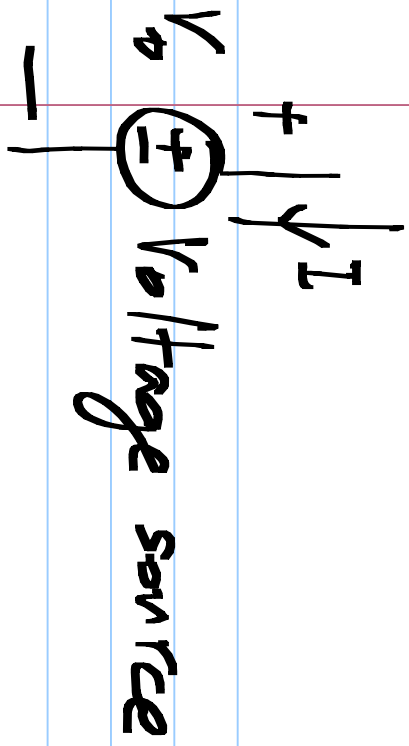
$$V = I \cdot R$$

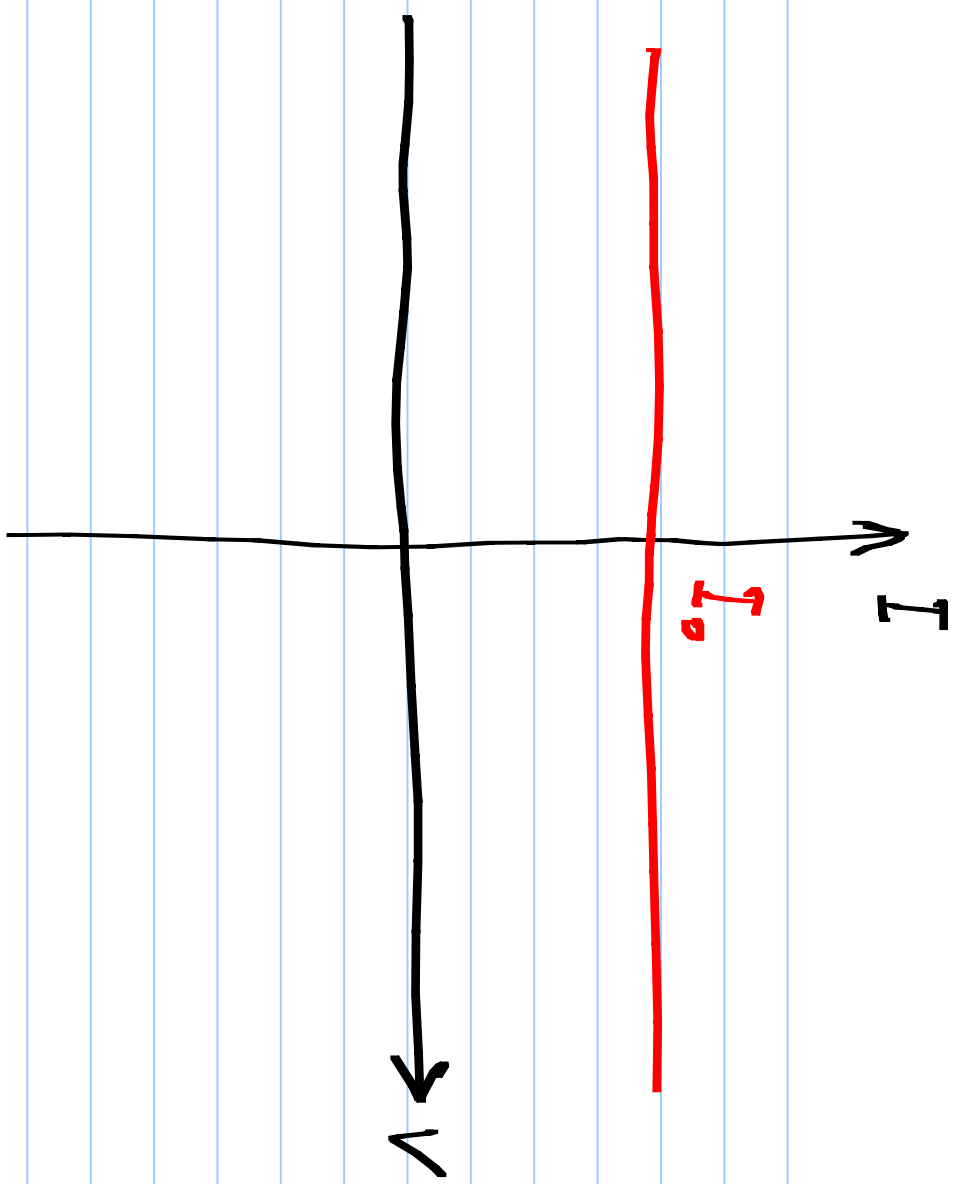
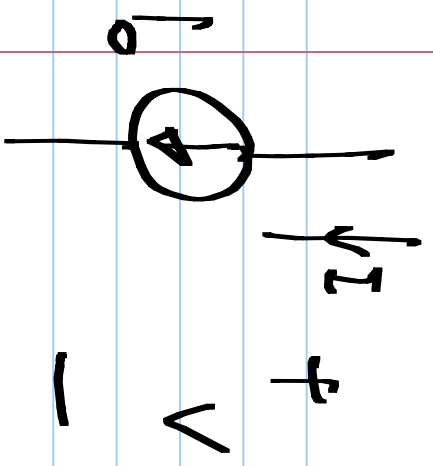
Resistance (Ω)

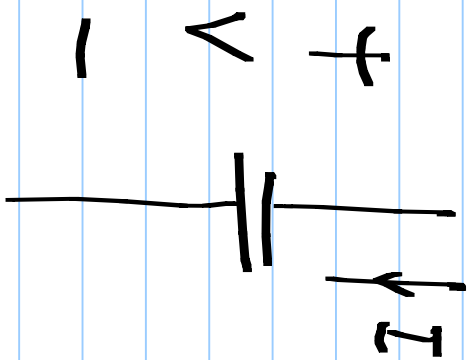
$$I = G \cdot V$$

Conductance (S)









$$I = C \cdot \frac{dV}{dt}$$



$$V = L \cdot \frac{dI}{dt}$$

