Problem 2:
The logic here looks for ’01’ pattern across the output of two consecutive comparators. So if the sa mpled input is different by 1 V_LSB, it will cause a bubble error. Error in Vin = Max. Slope X Sk ew in clock.

This gives maximum tolerable skew = 5 ps.

In the midterm problem, the logic is more "complicated". It looks for ’011’ pattern and hence the s kew tolerance is relaxed. But then the comparators have to drive more gates.

Problem 3:
Rds.C = 10% of 1ns = 100ps. C = 2pf => Rds = 50 ohm.
In order to find the Rds (or gds) of the nFET you can either do small signal simulation (as depicte d in Fig. 2b) or just do operating point simulation.

W/L = 38um/0.35um

a) 1)Clock feed-through: The falling edge of the clock (VT("/clk")) causes drop in the sampled val ue. This is evident when signal (VT("/in")) is rising. When the signal is decreasing, rising edge of the clock appears in the clock feed-through - the tiny rising portions in VT("/out").

If the rise/fall time is changed, the clock feed-through changes.

2) The difference between sampled value and the held value is large when the clock switches off, then when the clock switches on (see markers A,B in the plots attached). This is due to charge inj ection. Under no-charge injection case, the difference between sampled value and held value woul d remain same, whether the clock is switching on or off.

3) There is finite difference between the input and the sampled signal - Due to finite V_DS drop and finite time constant.

b) Pedestal error: input signal is 0.5V DC. Check the output signal. Ideally it should be at 0.5V.

Due to charge injection and clock feed-through, when the switch turns off, the output is not 0.5V. Pedestal error is about 40mV.

c) For fin = 1GHz/64 = 15.625 MHz, Vp = 0.1 V
DC -> -5.893 dB (which corresponds to 507 mV ... close to 500 mV)
Fundamental @ 15.625 MHz -> -20.1 dB (close to 0.1 V input signal)
2nd Harmonic @ 31.25 MHz -> -80 dB
3rd Harmonic @ 46.875 MHz -> -100.7 dB

Vp = 0.4 V
DC -> -5.89 dB (which corresponds to 507.6 mV ... close to 500 mV)
Fundamental @ 15.625 MHz -> -8.039 dB (corresponds to 396.3 mV - close to 400 mV input sig nal)
2nd Harmonic @ 31.25 MHz -> -56.34 dB

3rd Harmonic @ 46.875 MHz -> -86.39 dB

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fin = 65/64 GHz = 1.015625 GHz, Vp = 0.1 V
DC -> -6.004 dB (500.96 mV)
Fundamental @ 15.625 MHz -> -21.43 dB (84.8 mV as compared to 100 mV input)
2nd Harmonic @ 31.25 MHz -> -74.44 dB
3rd Harmonic @ 46.875 MHz -> -87.875 dB

Vp = 0.4 V
DC -> -6.107 dB (495 mV)
Fundamental @ 15.625 MHz -> -9.318 dB (342 mV as compared to 400 mV input)
2nd Harmonic @ 31.25 MHz -> -54.98 dB
3rd Harmonic @ 46.875 MHz -> -63.16 dB

More distortion in the second case (fin = 65/64 GHz).

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Problem 4:
Differential circuit - hence "cleaner" output - common mode errors are reduced.
Pedestal error reduced to 100s of fV.

fin = 1/64 GHz, Vp = 100 mV => Differentially 200 mV input amplitude.
DC -> -142.27 dB
Fundamental @ 15.625 MHz -> -13.88 dB (202.3 mV)
2nd Harmonic @ 31.25 MHz -> -128.92 dB
3rd Harmonic @ 46.875 MHz -> -103.16 dB

Vp = 400 mV => Differentially 800 mV amplitude
DC -> -131.63 dB
Fundamental @ 15.625 MHz -> -1.842 dB (808.95 mV)
2nd Harmonic @ 31.25 MHz -> -106.86 dB
3rd Harmonic @ 46.875 MHz -> -78.34 dB

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fin = 65/64 GHz, Vp = 100 mV => Differentially 200 mV input amplitude.
DC -> -133.57 dB
Fundamental @ 15.625 MHz -> -15.743 dB (163.25 mV)
2nd Harmonic @ 31.25 MHz -> -126.33 dB
3rd Harmonic @ 46.875 MHz -> -80.49 dB

Vp = 400 mV => Differentially 800 mV input amplitude.
DC -> -91.25 dB
Fundamental @ 15.625 MHz -> -3.783 dB (646.92 mV)
2nd Harmonic @ 31.25 MHz -> -85.63 dB
3rd Harmonic @ 46.875 MHz -> -55.89 dB

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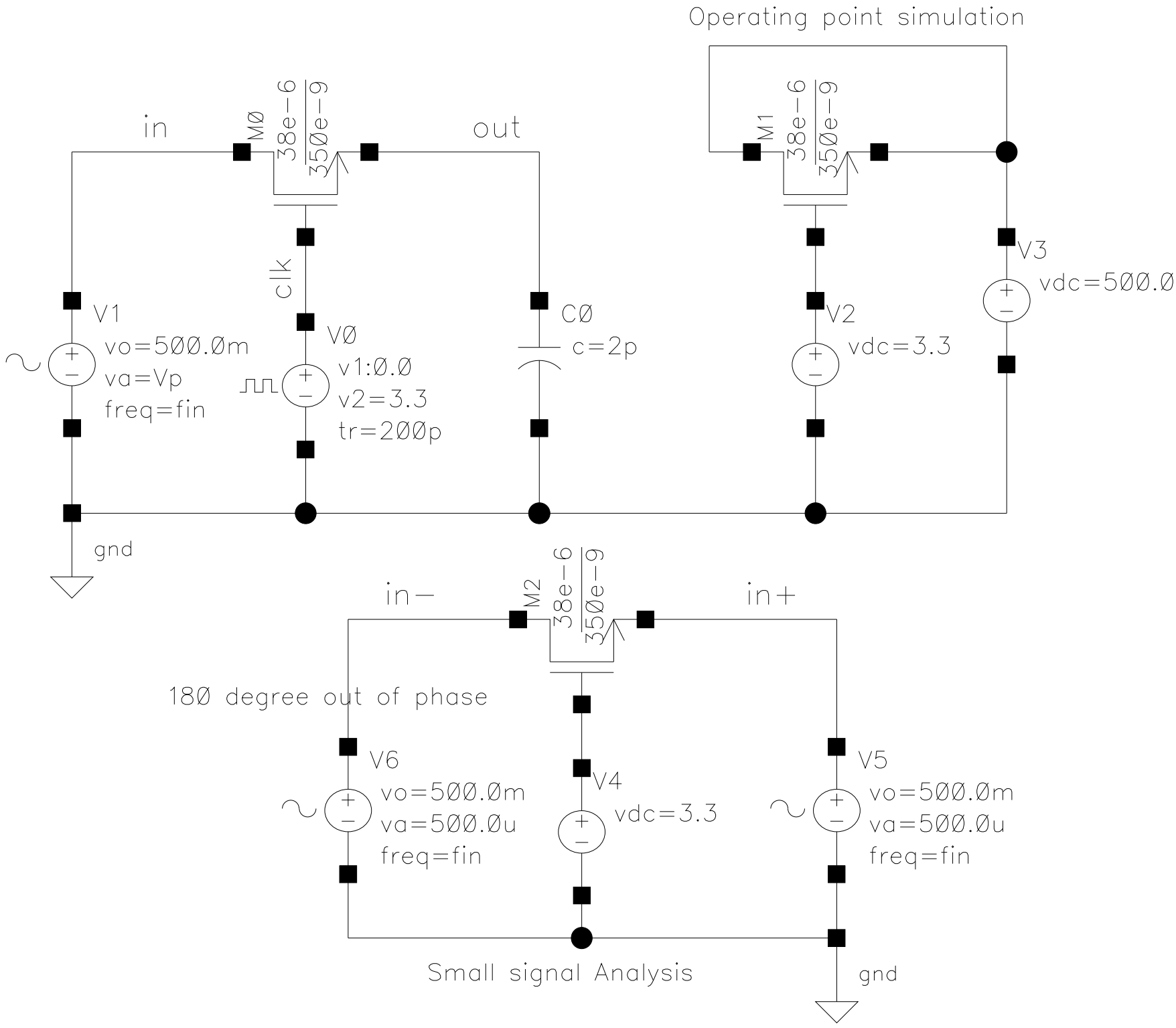
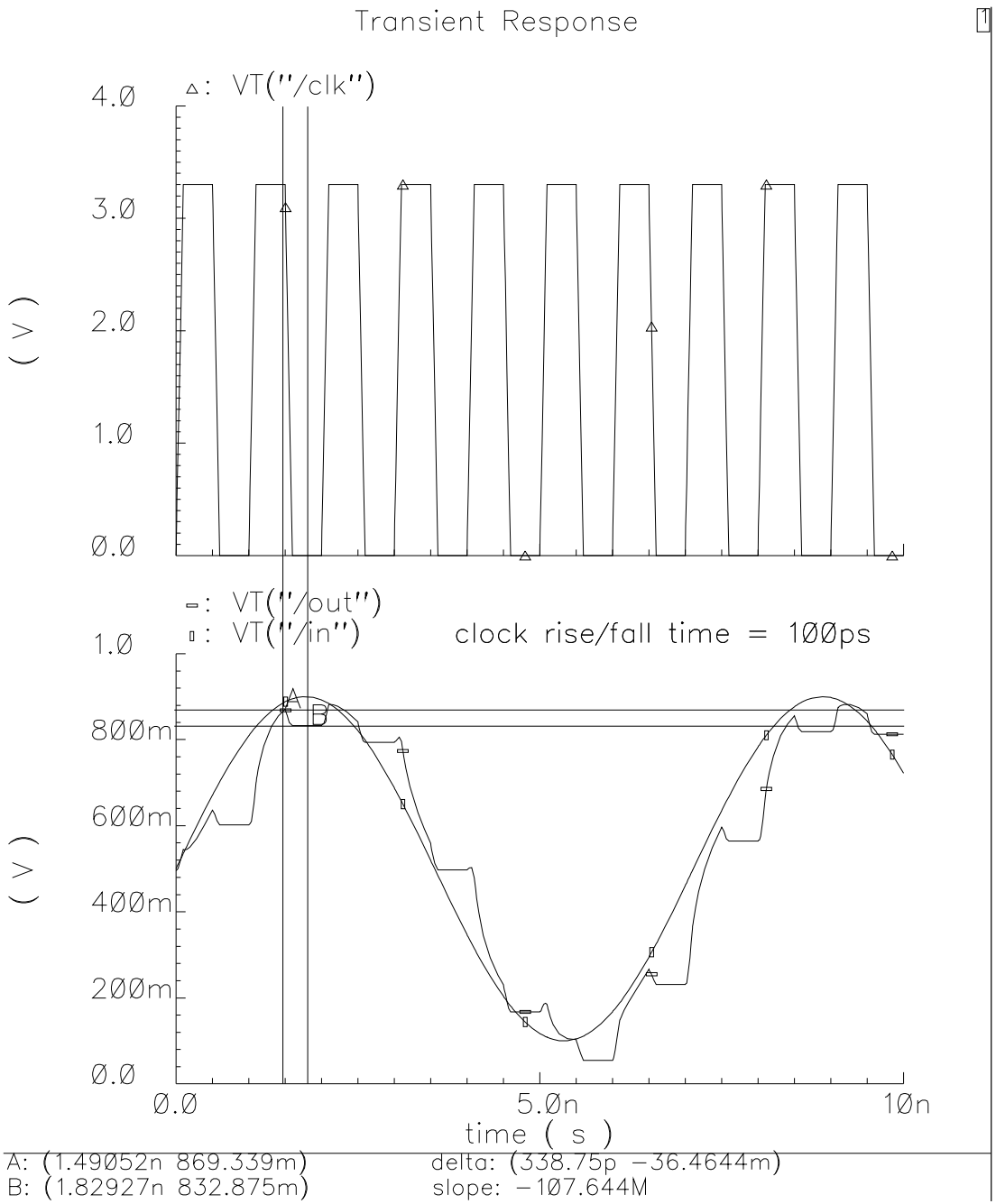
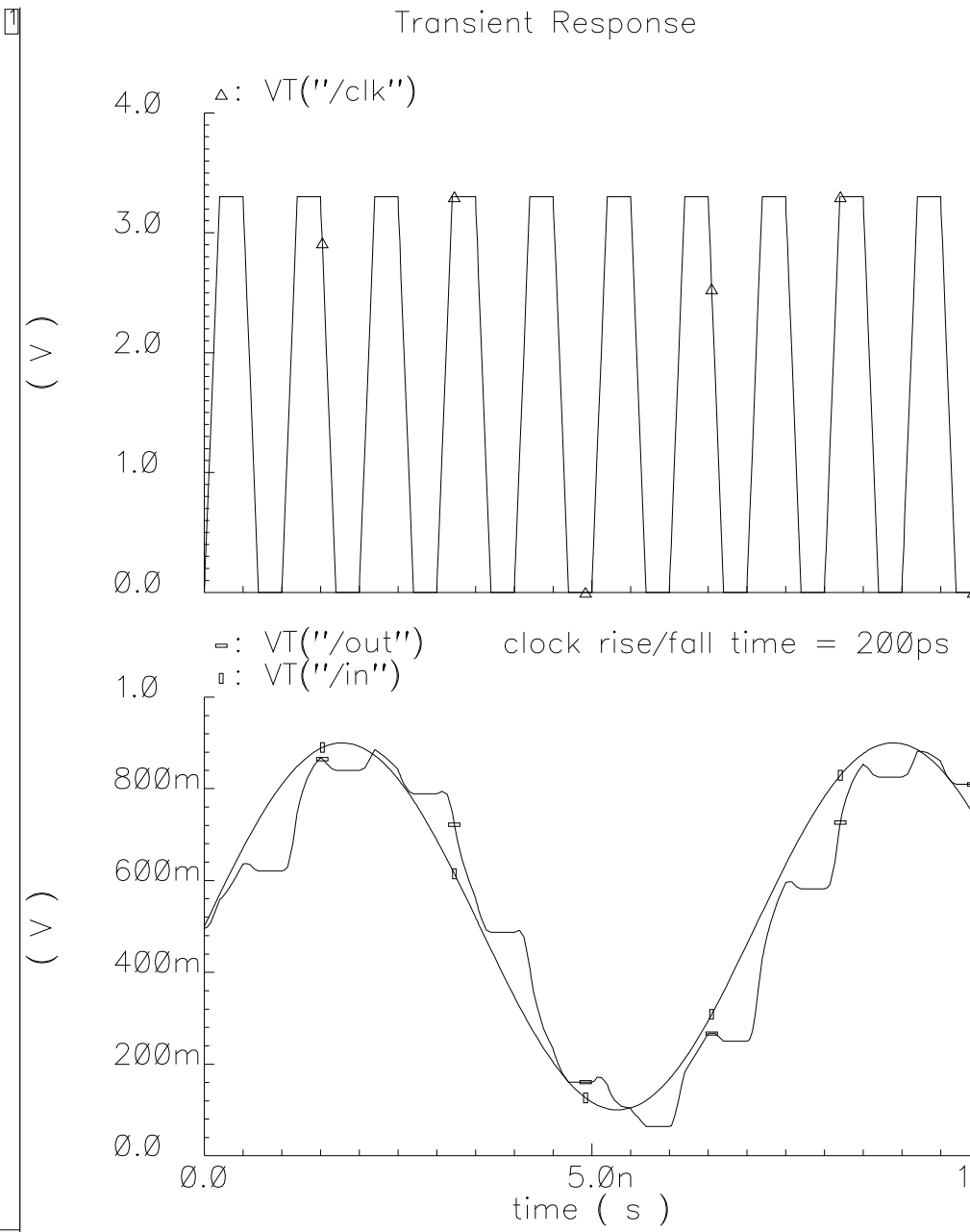
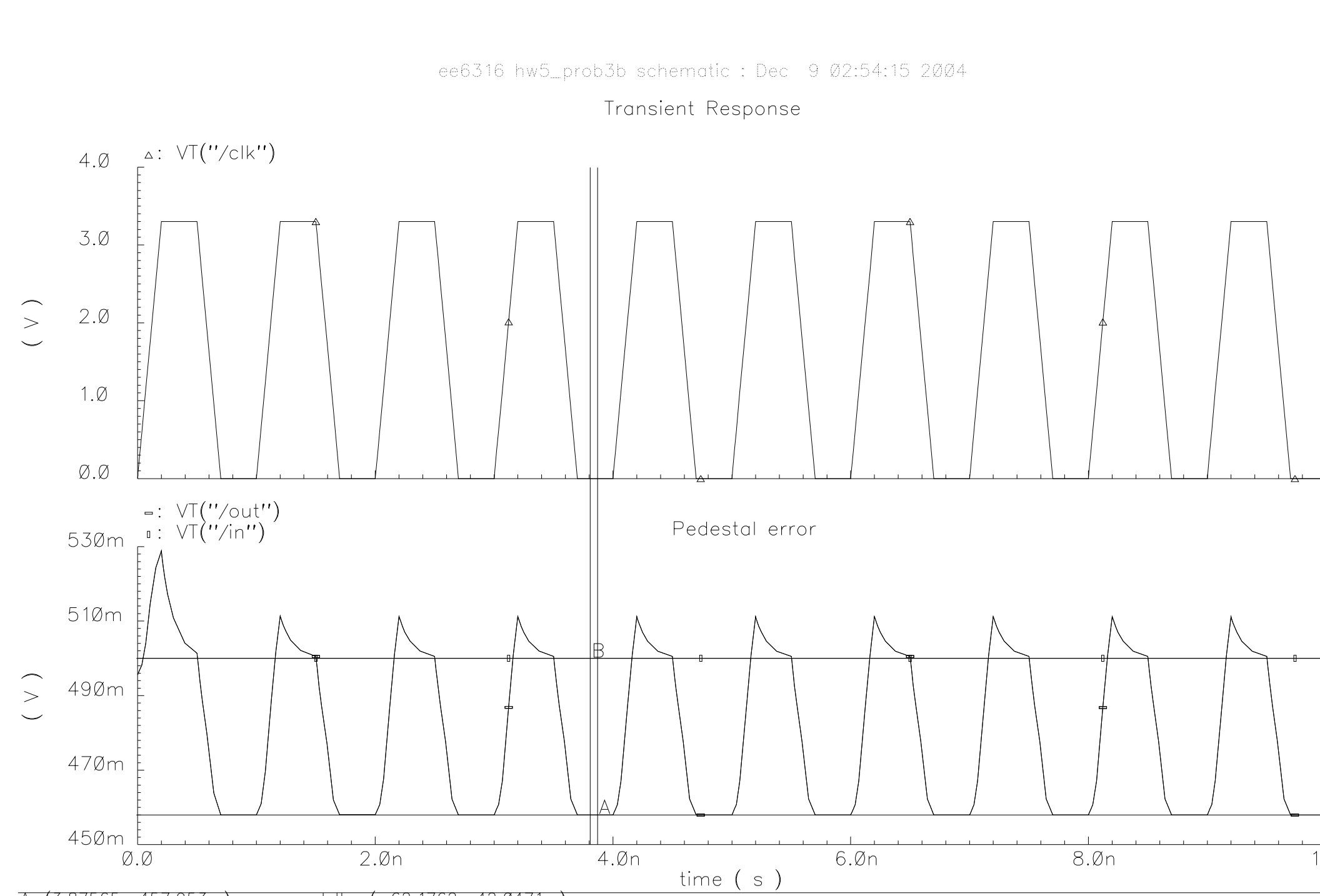
-Anuranjan Jha


Operating point simulation
in
M0
38e-6
350e-9
out
M1
38e-6
350e-9
clk
V1
vo=500.0m
va=Vp
freq=fin
V0
v1:0.0
v2=3.3
tr=200p
C0
c=2p
V2
vdc=3.3
V3
vdc=500.0
gnd
in-
M2
38e-6
350e-9
in+
180 degree out of phase
V6
vo=500.0m
va=500.0u
freq=fin
V4
vdc=3.3
V5
vo=500.0m
va=500.0u
freq=fin
Small signal Analysis
gnd


Transient Response
△: VT("/clk")
4.0
3.0
2.0
1.0
0.0
(V)
▫: VT("/out")
▯: VT("/in")
clock rise/fall time = 100ps
1.0
800m
600m
400m
200m
0.0
0.0
5.0n
10n
time (s)
A: (1.49052n 869.339m)
B: (1.82927n 832.875m)
delta: (338.75p −36.4644m)
slope: −107.644M


Transient Response
△: VT("/clk")
4.0
3.0
2.0
1.0
0.0
(V)
▫: VT("/out")
▯: VT("/in")
clock rise/fall time = 200ps
1.0
800m
600m
400m
200m
0.0
0.0
5.0n
time (s)


ee6316 hw5_prob3b schematic : Dec 9 02:54:15 2004
Transient Response
△: VT("/clk")
4.Ø
3.Ø
2.Ø
1.Ø
Ø.Ø
(V)
▫: VT("/out")
▯: VT("/in")
Pedestal error
530m
510m
490m
470m
450m
B
A
Ø.Ø
2.Ø n
4.Ø n
6.Ø n
8.Ø n
time (s)
A: (3.87565n 457.953m)
B: (3.81347n 500m)
delta: (−62.1762p 42.0471m)
slope: −676.257M