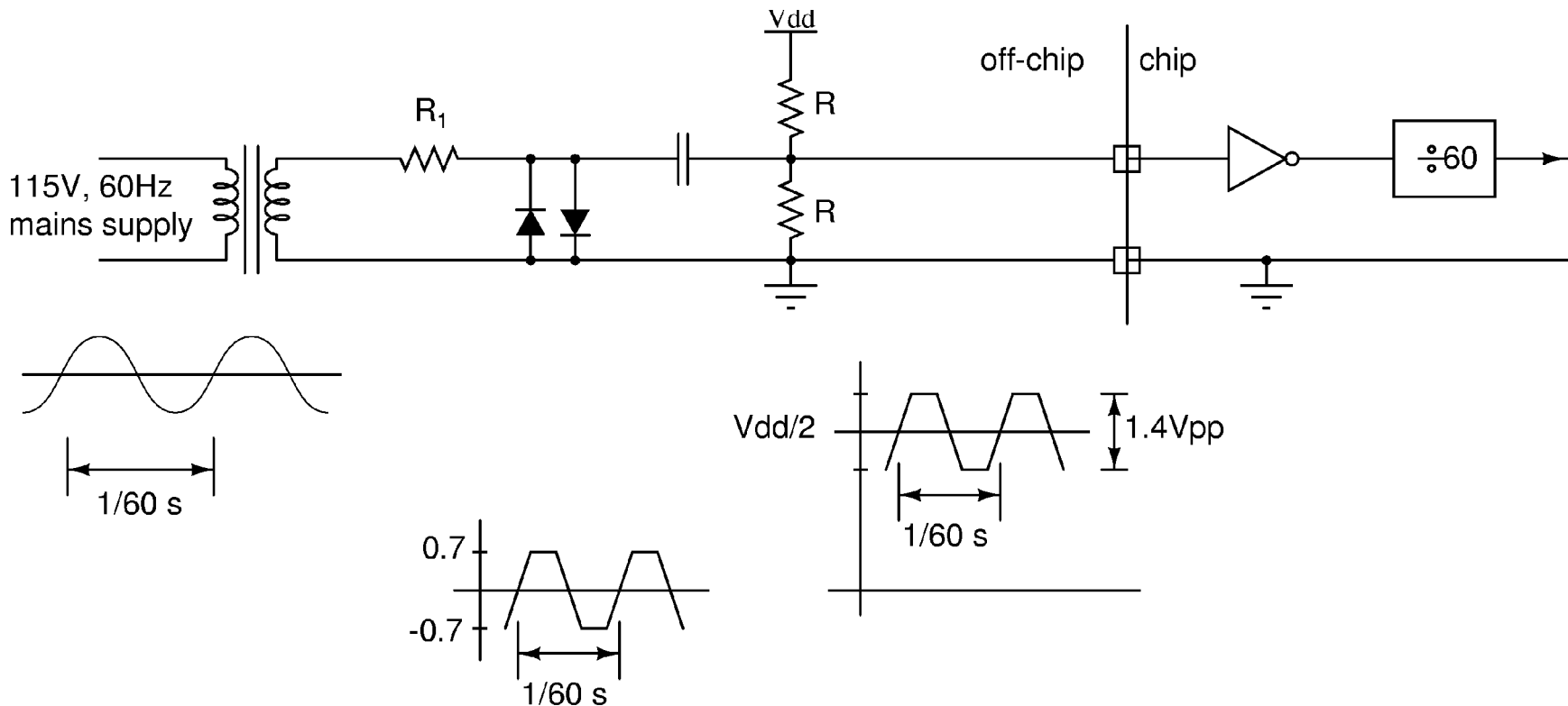


E4332: VLSI Design Laboratory

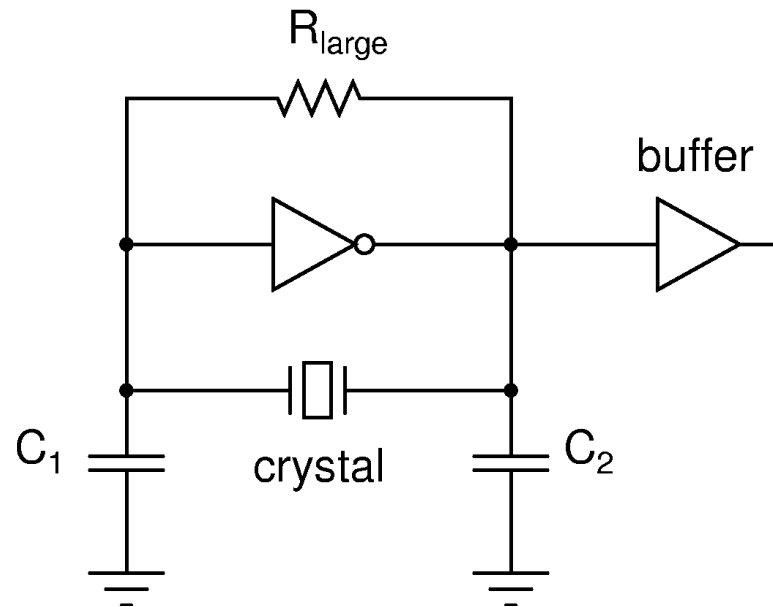
Nagendra Krishnapura
Columbia University
Spring 2005: Lectures
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Digital Clock: Timebase #1



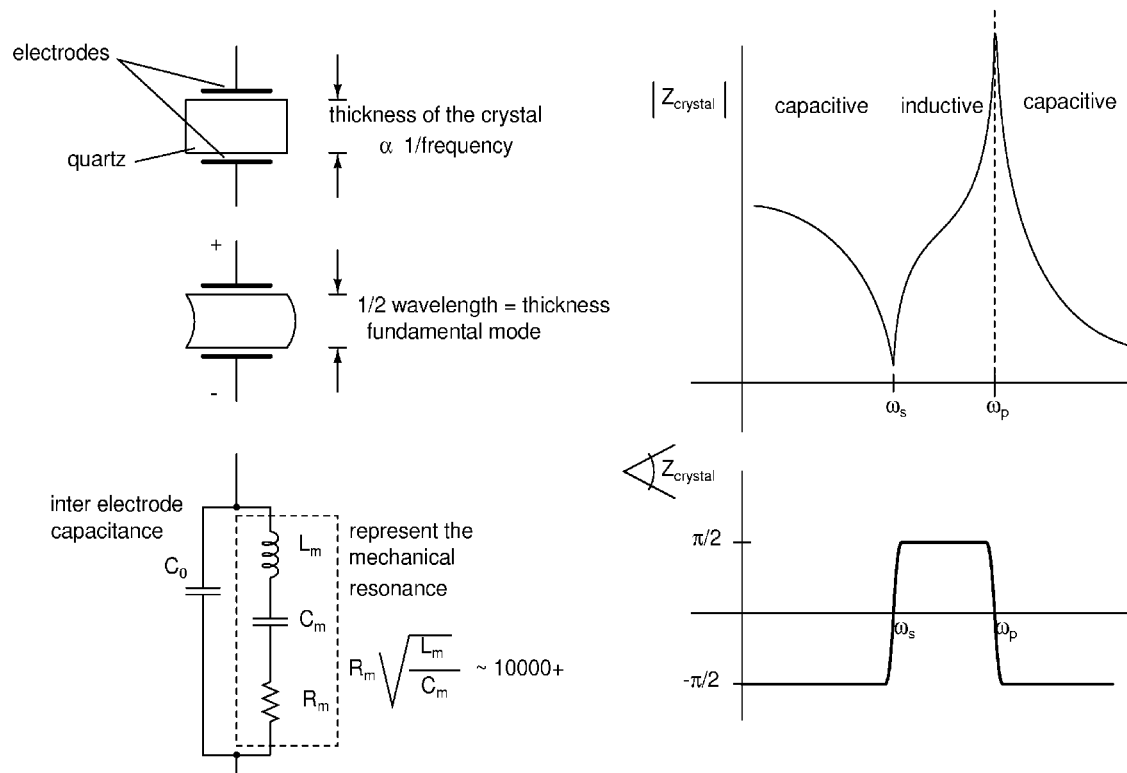
- 60Hz from mains source
- Clip, buffer, and divide by 60 to get 1Hz clock

Digital Clock: Timebase #2



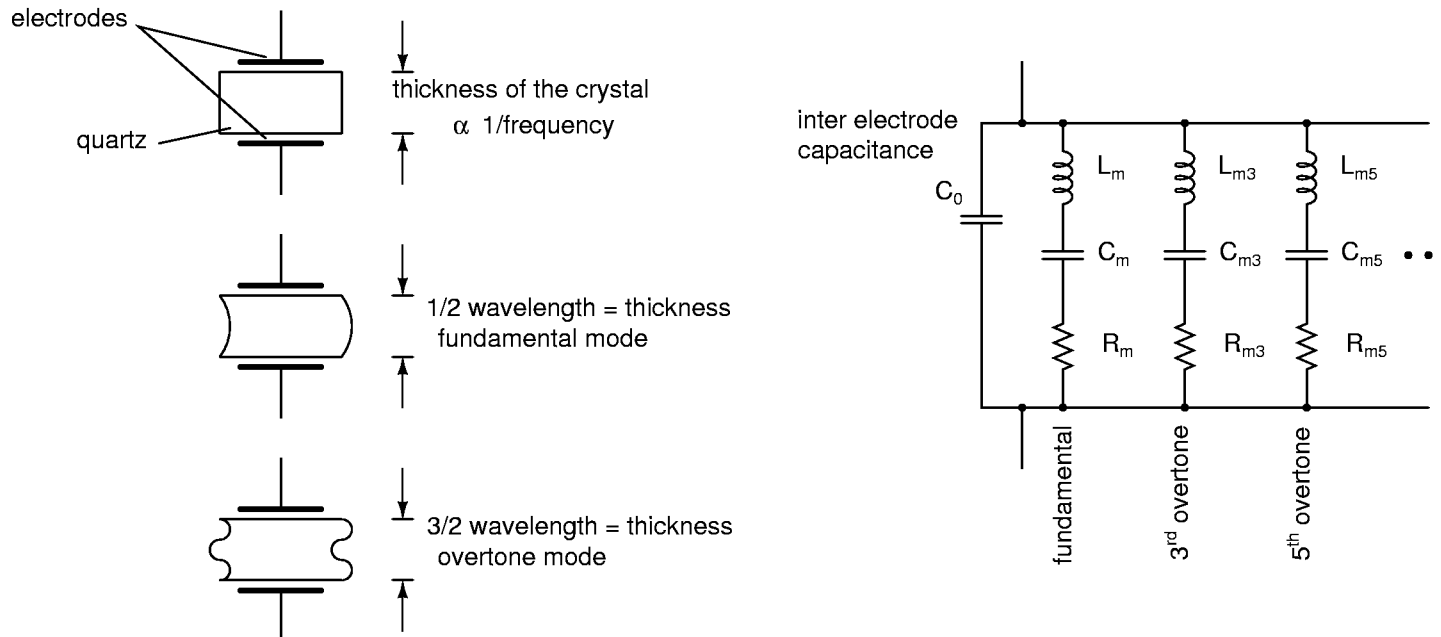
- Crystal oscillator
- Accurate frequency, low drift

Crystal equivalent circuit



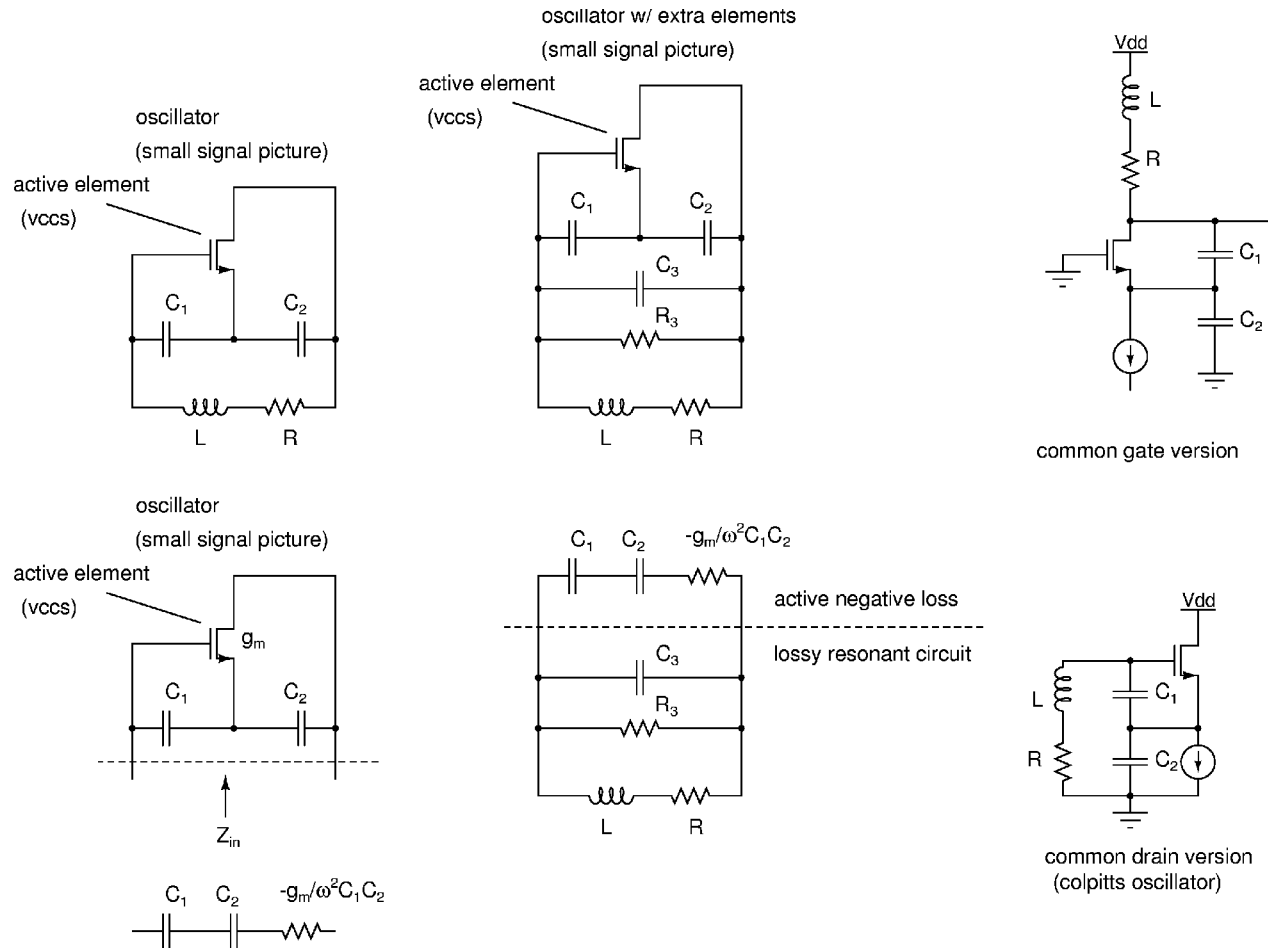
- Series(ω_s) and parallel(ω_p) resonance
- Extremely high Q $\sim 10,000$ s
- Oscillator freq. usually between ω_s and ω_p

Crystal equivalent circuit



- Overtone modes present in the crystal
- Can oscillate at these frequencies
- Overtone modes need to be suppressed

Oscillator principle

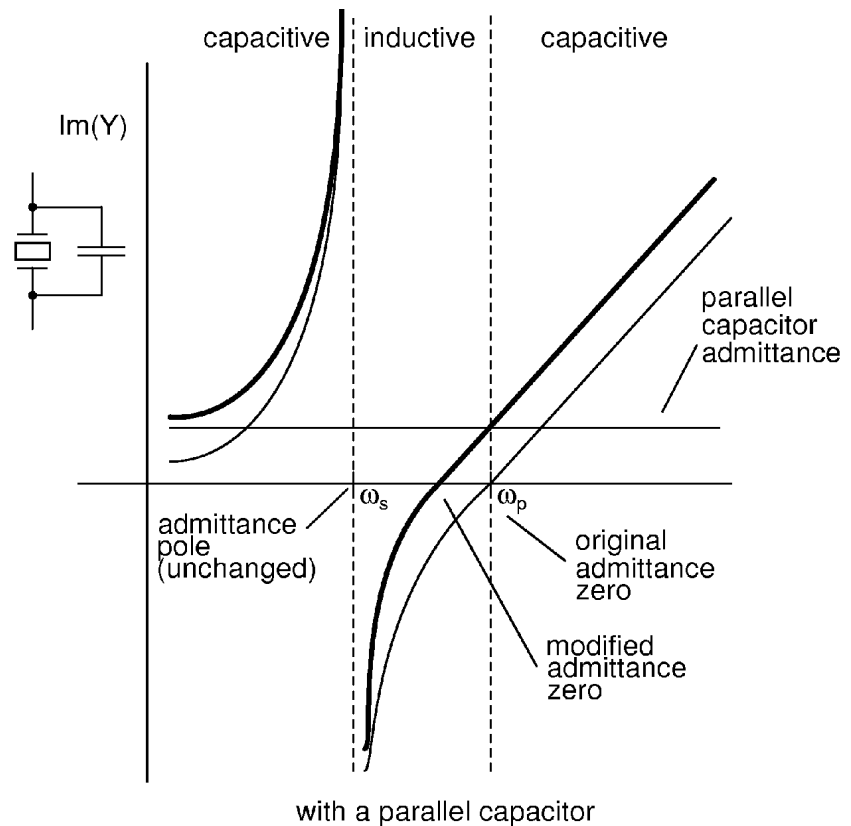
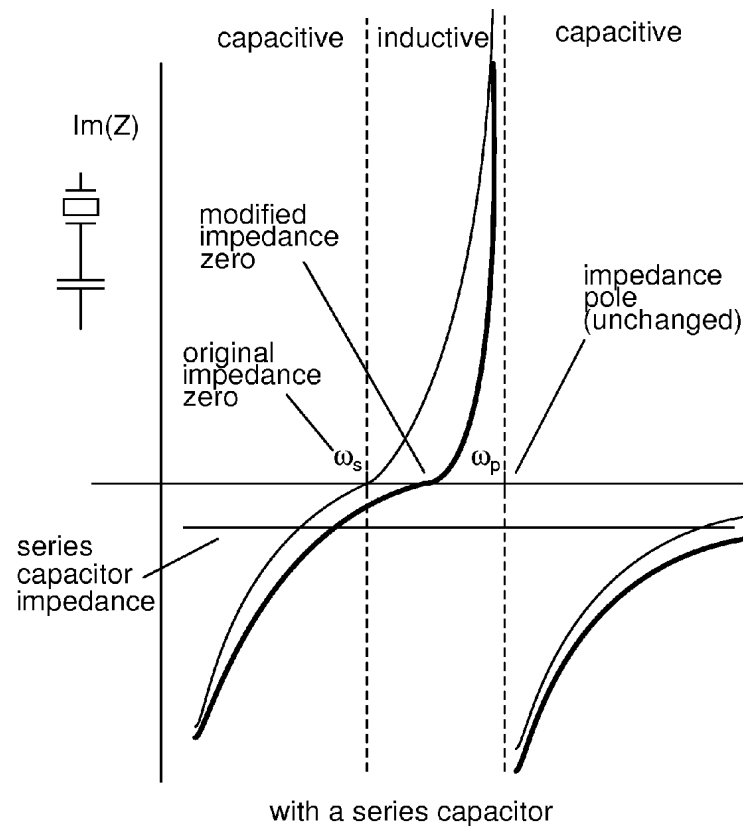


- C_1 , C_2 , g_m result in a negative resistance and compensate resonator loss.

Oscillator principle

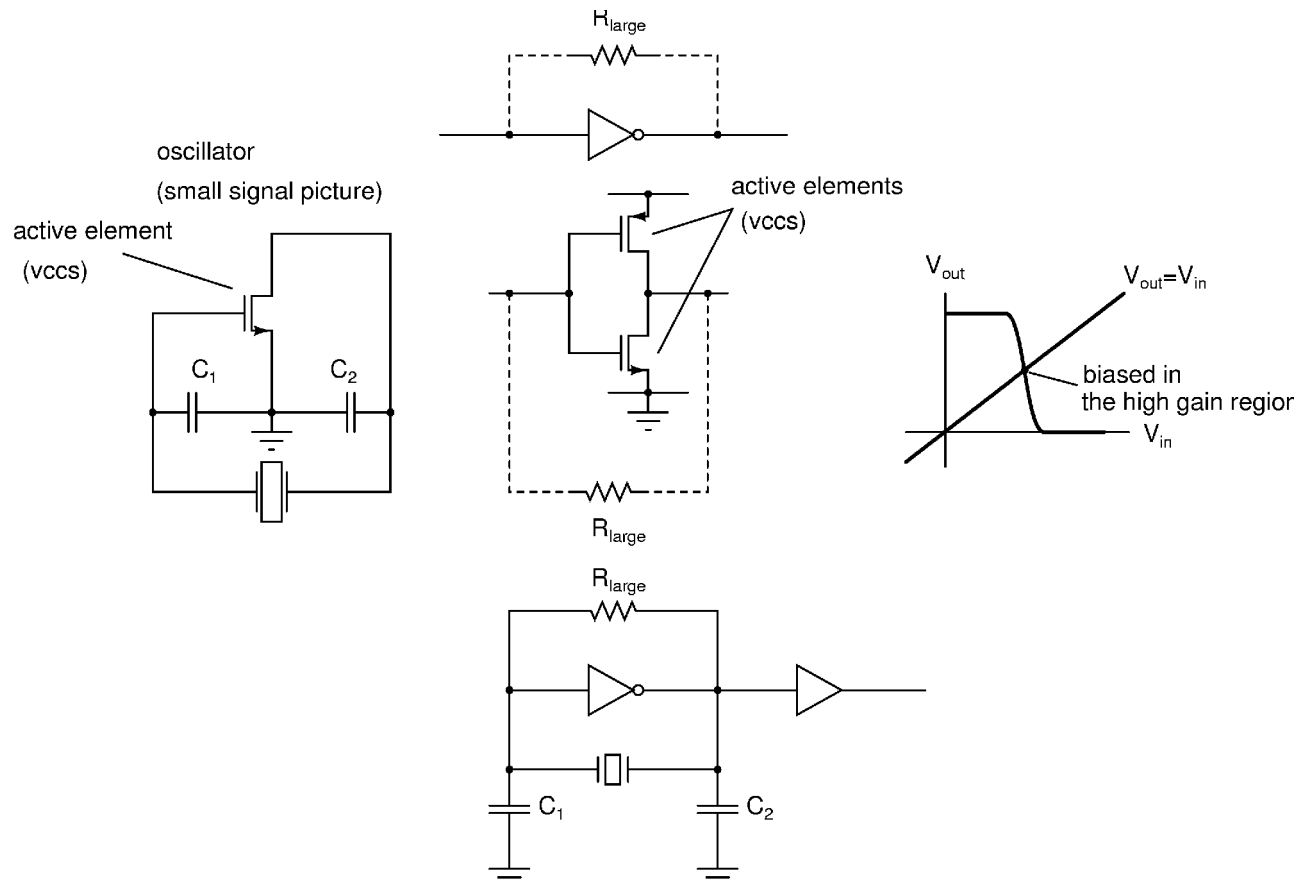
- Circuit oscillates at a frequency of net zero reactance
 - Impedance zero (series mode)
 - Admittance zero (parallel mode)
- Series/shunt capacitors can tune the oscillation frequency slightly
- Oscillation frequency between ω_s and ω_p
- $|g_m / \omega^2 C_1 C_2|$ increases \Rightarrow greater loss compensation (greater oscillator loop gain)
- g_{ds} results in extra loss; minimize

Oscillator principle



- Pole/zero of impedance and admittance lie between ω_s and ω_p

Crystal oscillators



- Crystal replaces inductor-parallel mode
- Inverter biased in high gain region acts as a g_m

CMOS crystal oscillators

Package Size		DS26	DS15	DS10	
Nominal frequency	F_L	32.768	32.768	32.768	kHz
Load capacitance ¹⁾	C_L	8.2	8.2	8.2	pF
Frequency tolerance ²⁾	$\Delta F/F$	+/-20	+/-20	+/-20	ppm
	$\Delta F/F$	+/-30	+/-30	+/-30	ppm
	$\Delta F/F$	+/-100	+/-100	+/-100	ppm
Series resistance typ./max.	R_S	30 / 42	35 / 50	45 / 60	k Ω
Motional capacitance typ.	C_1	2.1	2.1	2.1	fF
Static capacitance typ.	C_0	0.9	0.9	0.9	pF
Drive level max.	P	1.0	1.0	1.0	μ W
Quality factor min.	Q	55'000	45'000	38'000	
Insulation resistance min.	R_i	500	500	500	M Ω
Aging first year max.	$\Delta F/F$	+/-3	+/-3	+/-3	ppm
Turnover temperature	T_0	25 +/-5	25 +/-5	25 +/-5	$^{\circ}$ C
Frequency vs. temperature	$\Delta F/F_0$	$-0.035 \text{ ppm}/^{\circ}\text{C}^2 (T - T_0)^2$			+/-10% ppm

1) Other load capacitances on request.

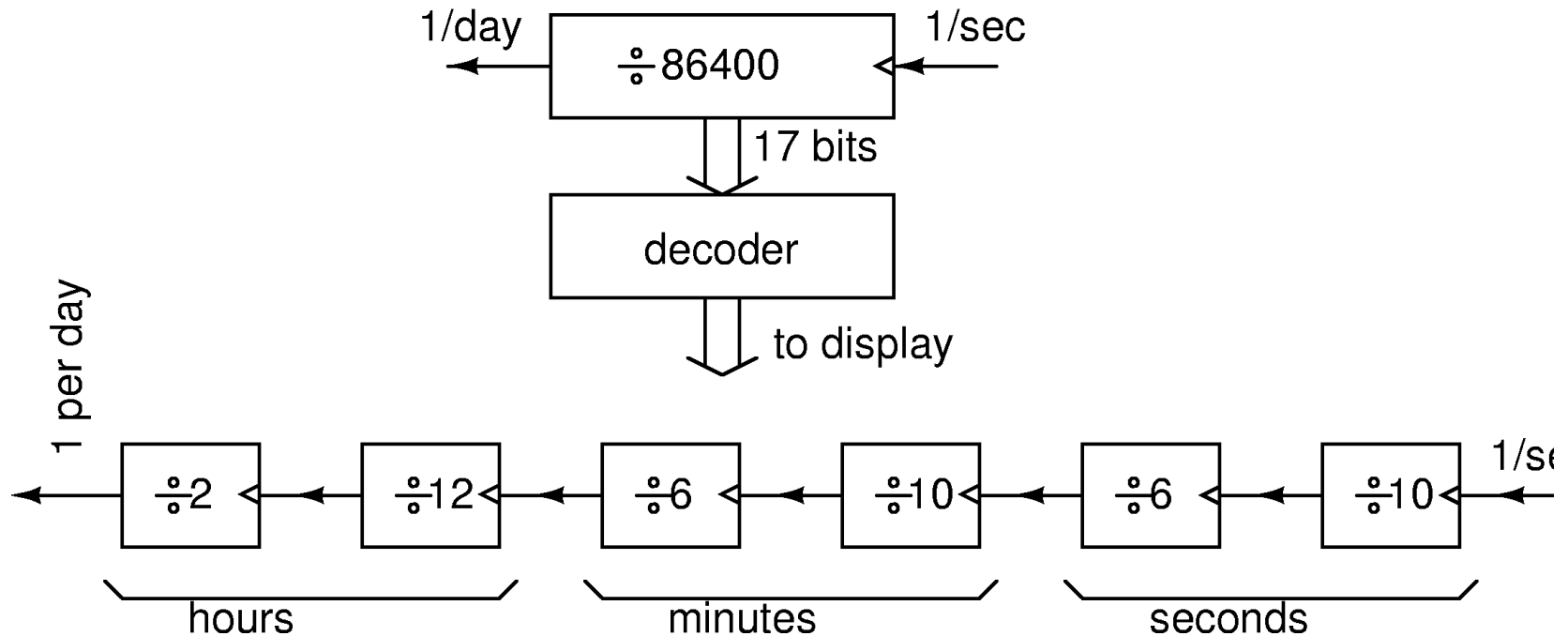
2) Tighter and wider frequency tolerances on request.

- Crystal power dissipation in parallel resonant mode $\sim V_{\text{rms}}^2 / R_s \cdot 1 / (1 + Q^2 (C_m / 2C_0)^2)$

CMOS crystal oscillator design

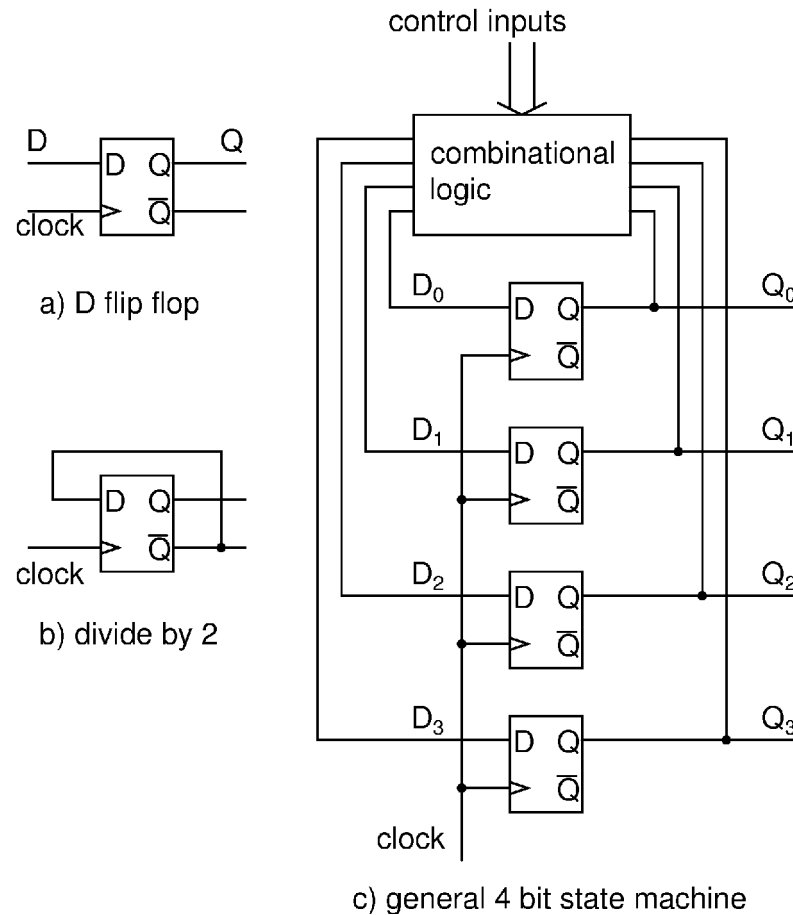
- 32,768Hz crystal: suitable for a digital clock
- Determine C_m , L_m , R_m from crystal specs.
Crystal can be modeled using these.
- Design a suitable active element for the oscillator. e.g. inverter
- Variable C_1 or C_2 useful for trimming the frequency.
- Calculate crystal power dissipation. Ensure that it is within specs.

Digital clock: dividers



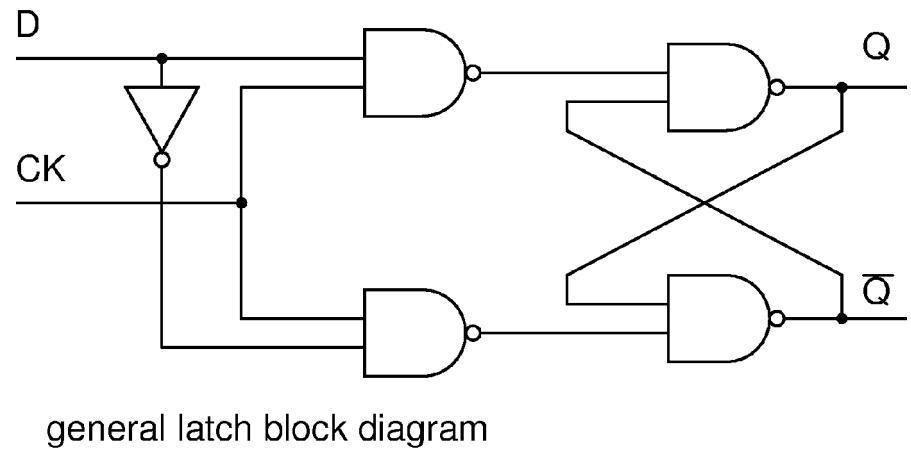
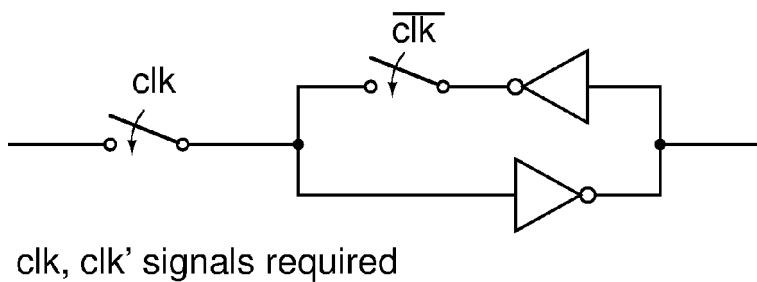
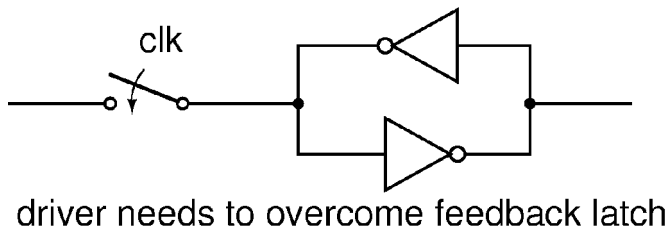
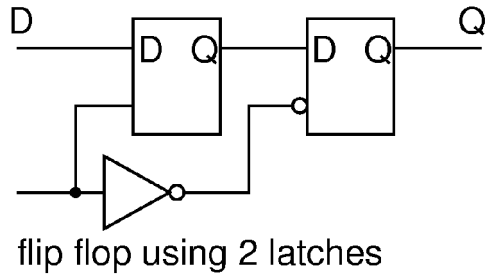
- Cascade structure

Digital clock: dividers



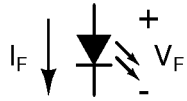
- Dividers: simple state machines
- Avoid glitches

Digital clock: latches

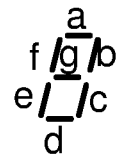


- Low speed-static latches

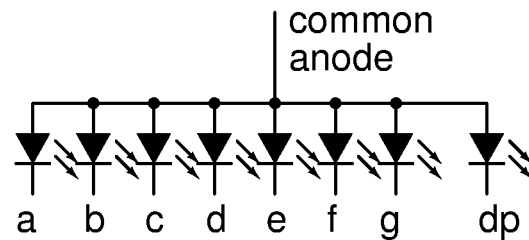
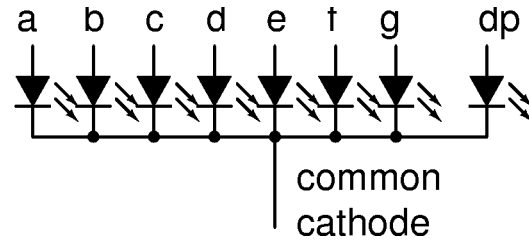
Digital clock: displays



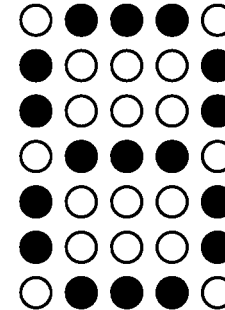
$V_F \sim 1.5 \dots 2V$
 $I_F \sim 1-10mA$;
 depends on the size



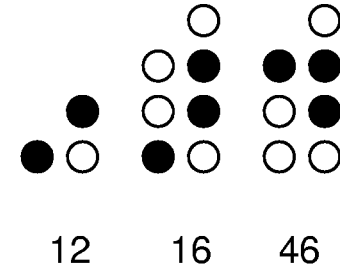
7 segment numeric display. may include decimal point



a) 7 segment display



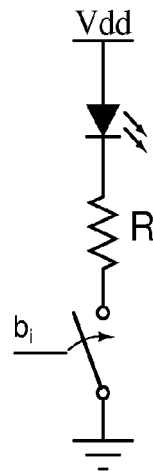
b) 5x7 array display



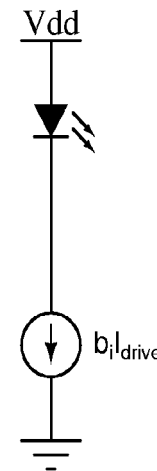
c) bcd display

- Display type: LED: bright / LCD: low power
- Interface type: 7 segment / dot matrix / anything else

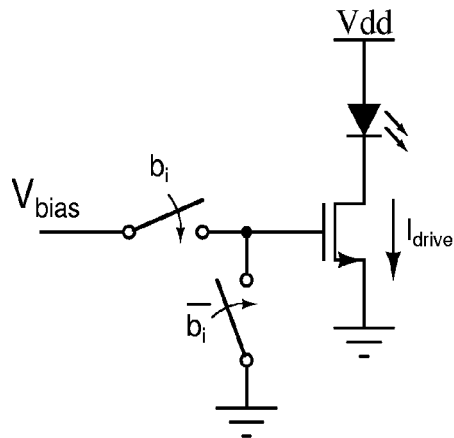
Digital clock: display drivers



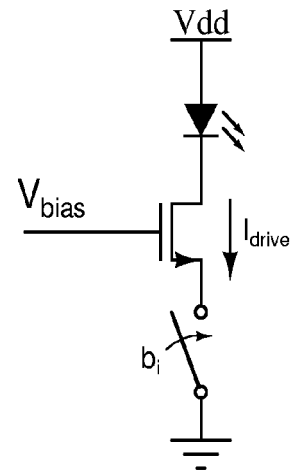
switch + current limiting resistor



current source drive



gate switching

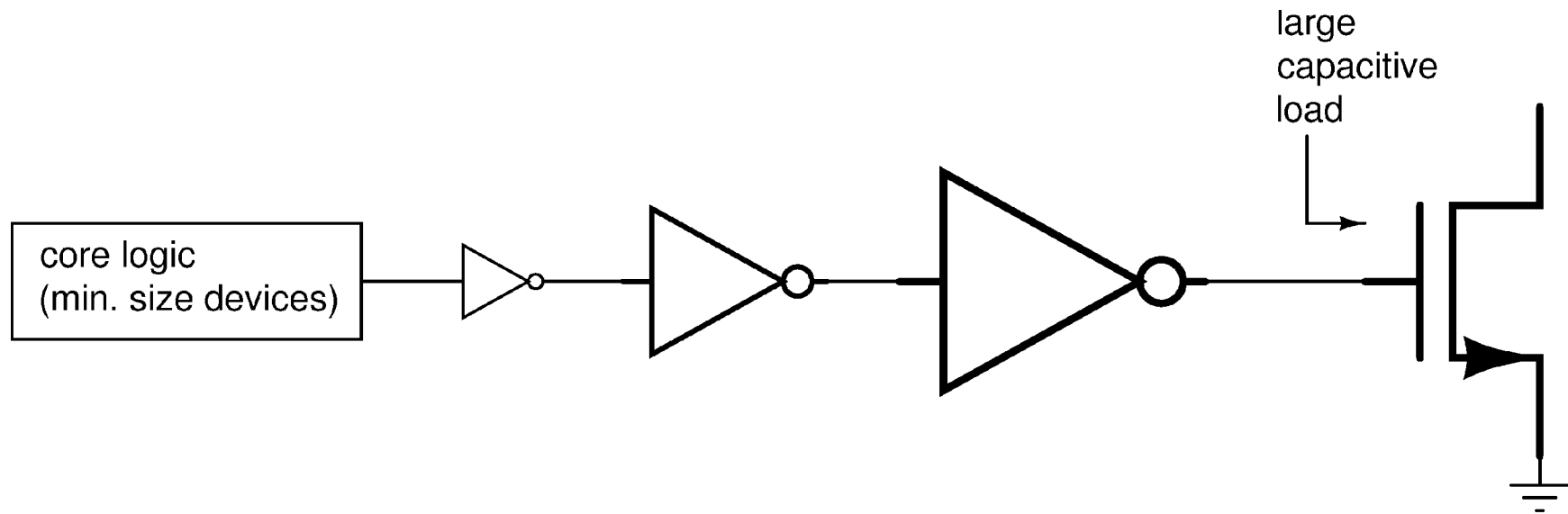


source switching

Digital clock: display drivers

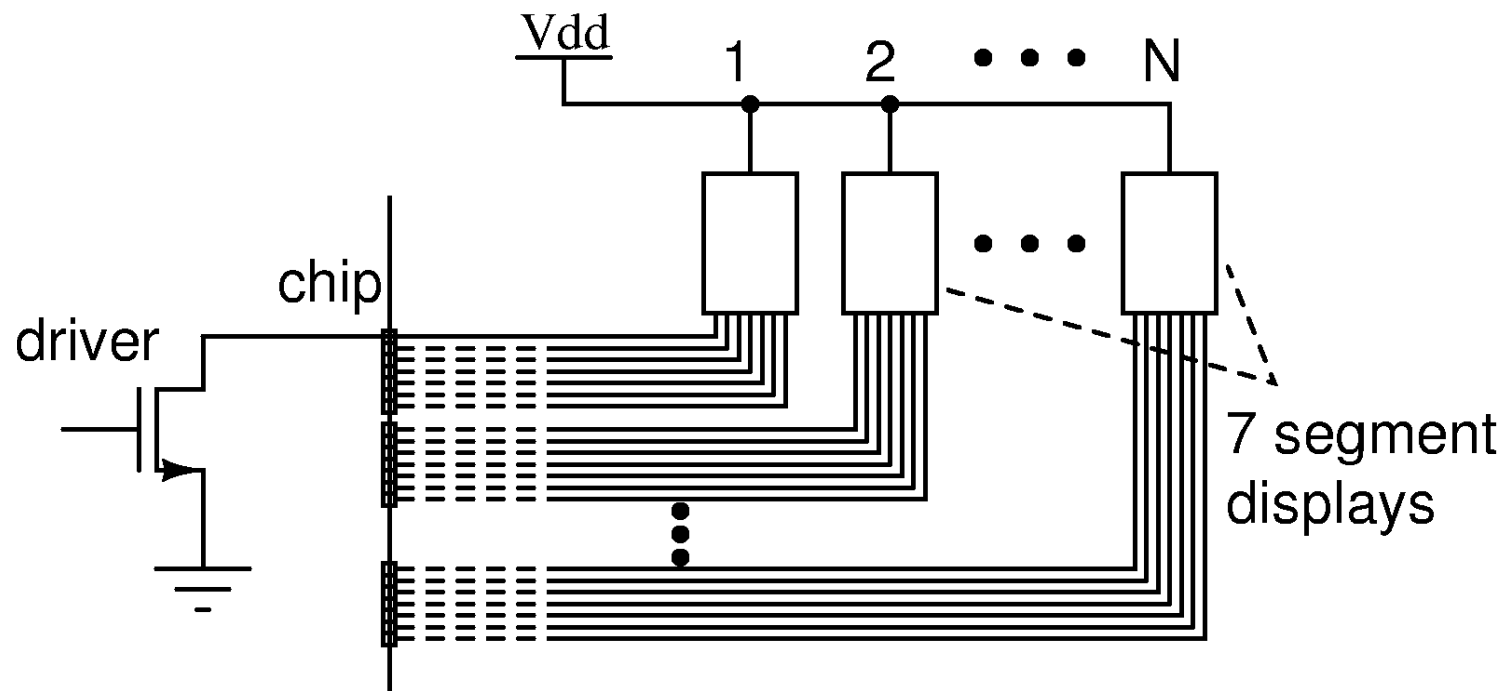
- Switch+resistor
 - Used in discrete drivers
- Current source drive
 - Easily implemented in CMOS
- Gate switching
 - Small switches, complementary switching control signals
- Source switching
 - Large switches, single switching control signal

Digital clock: display drivers



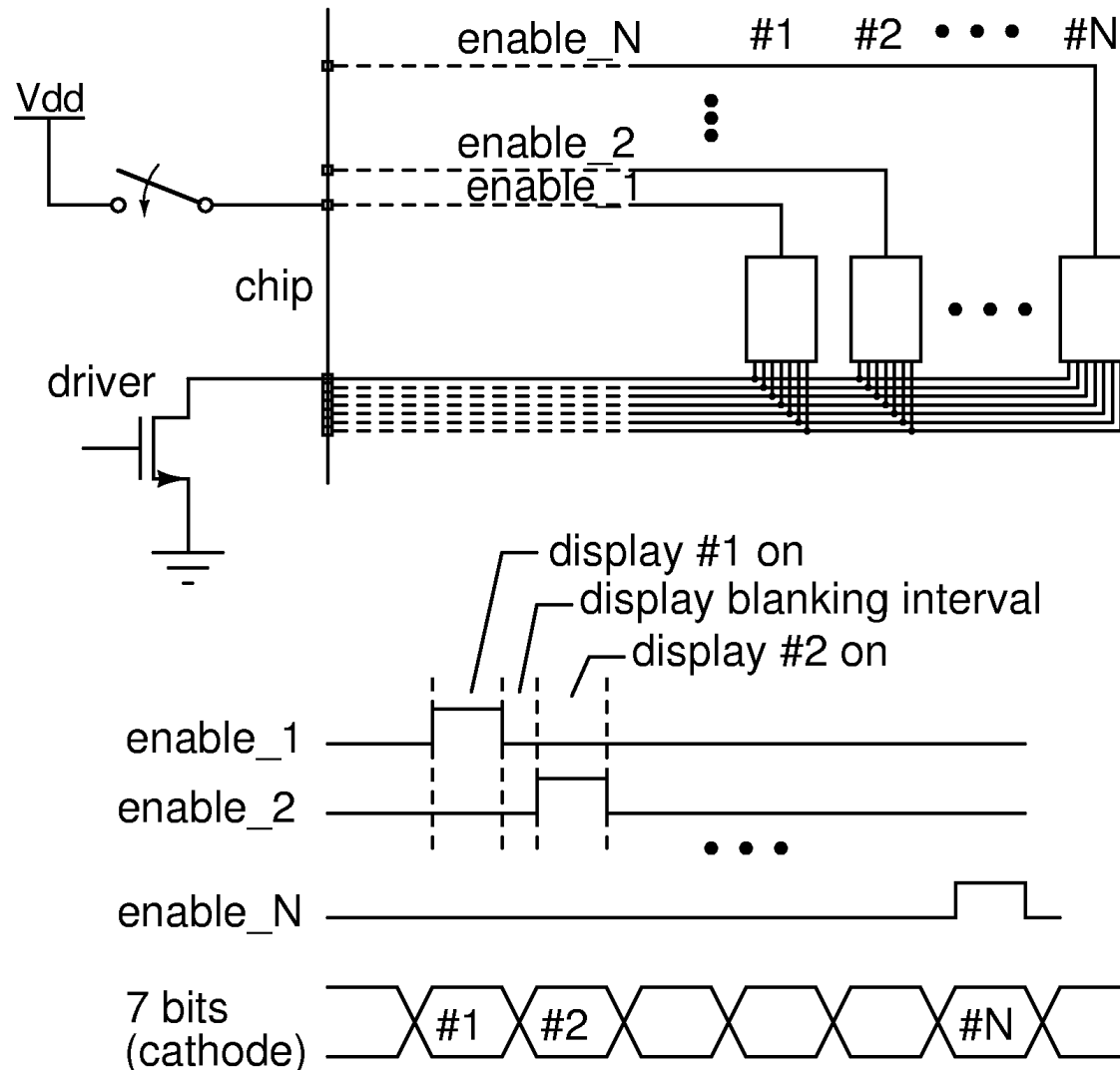
- Output current drive \sim mA (LEDs)
- Progressively larger driver for large loads

Digital clock: continuous drive



- Simple
- $7 \cdot N$ pins, drivers for N displays

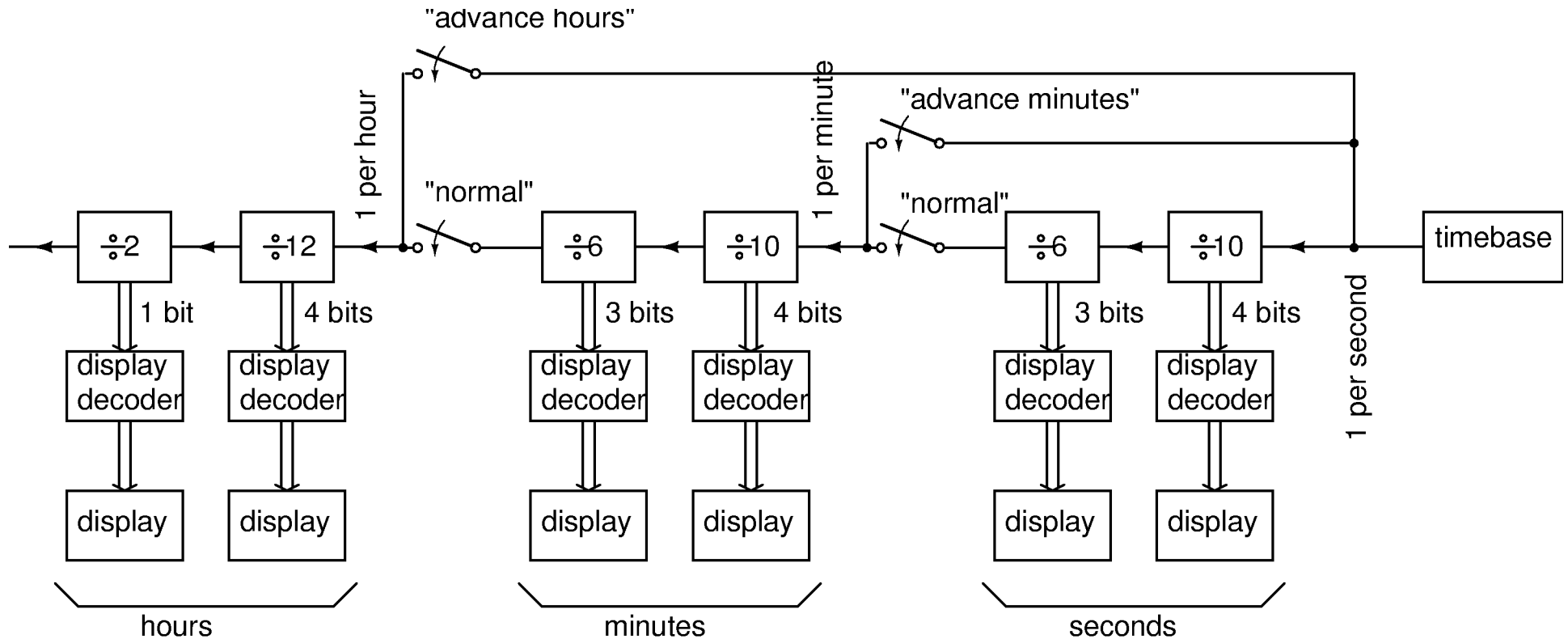
Digital clock: multiplexed drive



Digital clock: Multiplexed drive

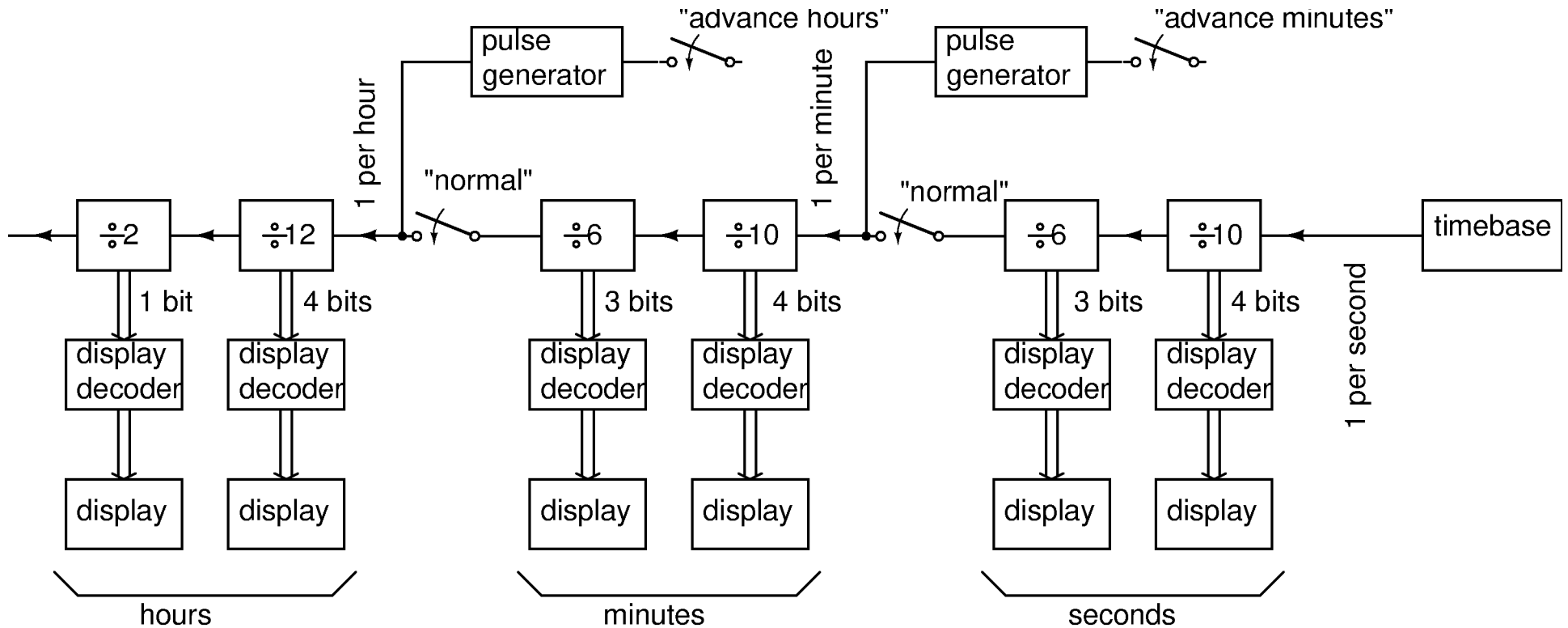
- Cycle through N displays at a high rate ~ few kHz to result in a persistent display
- N+7 pins, drivers for N displays
- Display blanking to avoid wrong digit flickering. Enable only when digit input is stable
- Larger peak current ($\sim\sqrt{N}$) to preserve brightness
- Dot matrix displays: multiplexed row/column drivers

Digital clock: Time set function



- Advance minute/hour counter @ 1/sec.

Digital clock: Time set function



- Advance minute/hour counter @ input pulse rate.

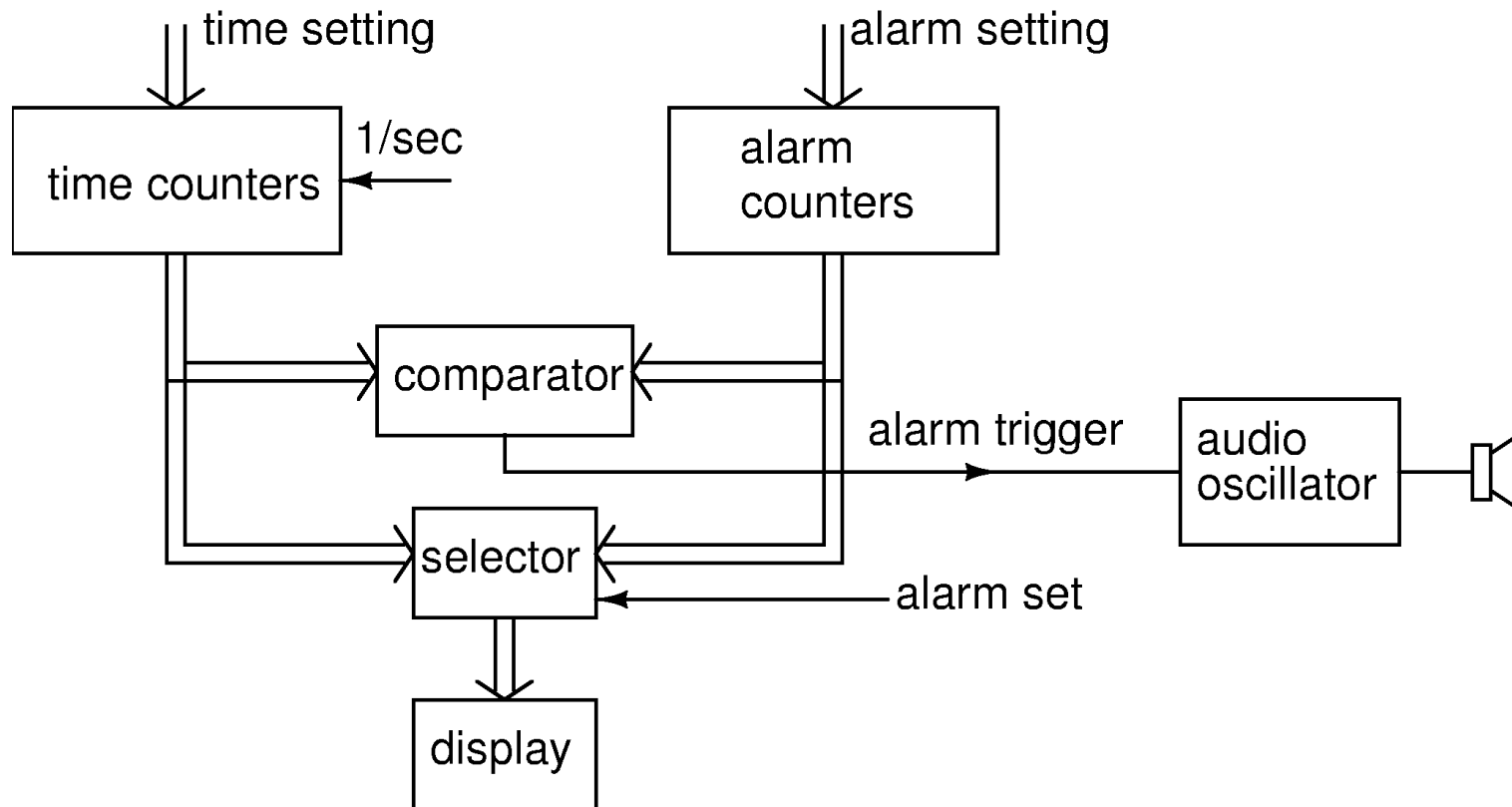
Digital clock: Time set function

- Switching between “setting” mode and “normal” mode should be glitch free-i.e. No spurious edges.
- Off chip switch inputs should be debounced.

Digital clock: Alarm function

- Digital clock, AM radio: low frequency circuits, but
 - Need to complete it!
 - Minimize power
 - Minimize supply voltage
 - etc.

Digital clock: Alarm function



- Alarm circuitry core same as clock circuitry.

Digital clock: Design review

- Present details of
 - Timebase
 - Supply voltage
 - Dividers
 - Display
 - Decoders
 - Display drivers
 - Time setting
 - Alarm
 - Anything else you want to put in

Digital clock: design flow

- Dividers, decoders, drivers ...
- Prioritize essential blocks.