Packaging
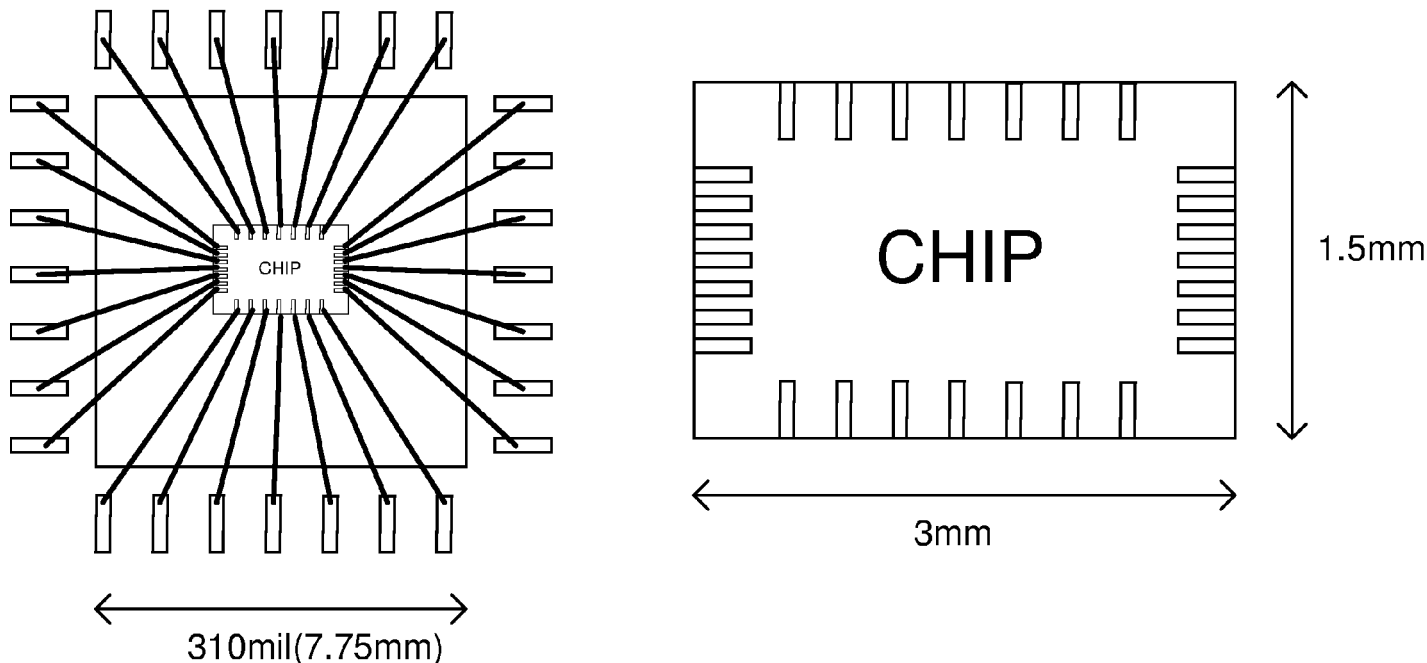
- Need to choose a package
  - 28pin DIP(Dual in line package)
  - 40pin DIP
  - 65pin PGA(pin grid array; not sure of availability-wait for me to confirm)

- Determine the bonding diagram
  - Connections of the chip pad to the pins

Packaging

- Need to choose a package
  - 28pin DIP(Dual in line package)
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  - 65pin PGA(pin grid array)
- Determine the bonding diagram
  - Connections of the chip pad to the pins
  - Need this for PCB design
- Chip area(including pads): 1.5mmx3.0mm
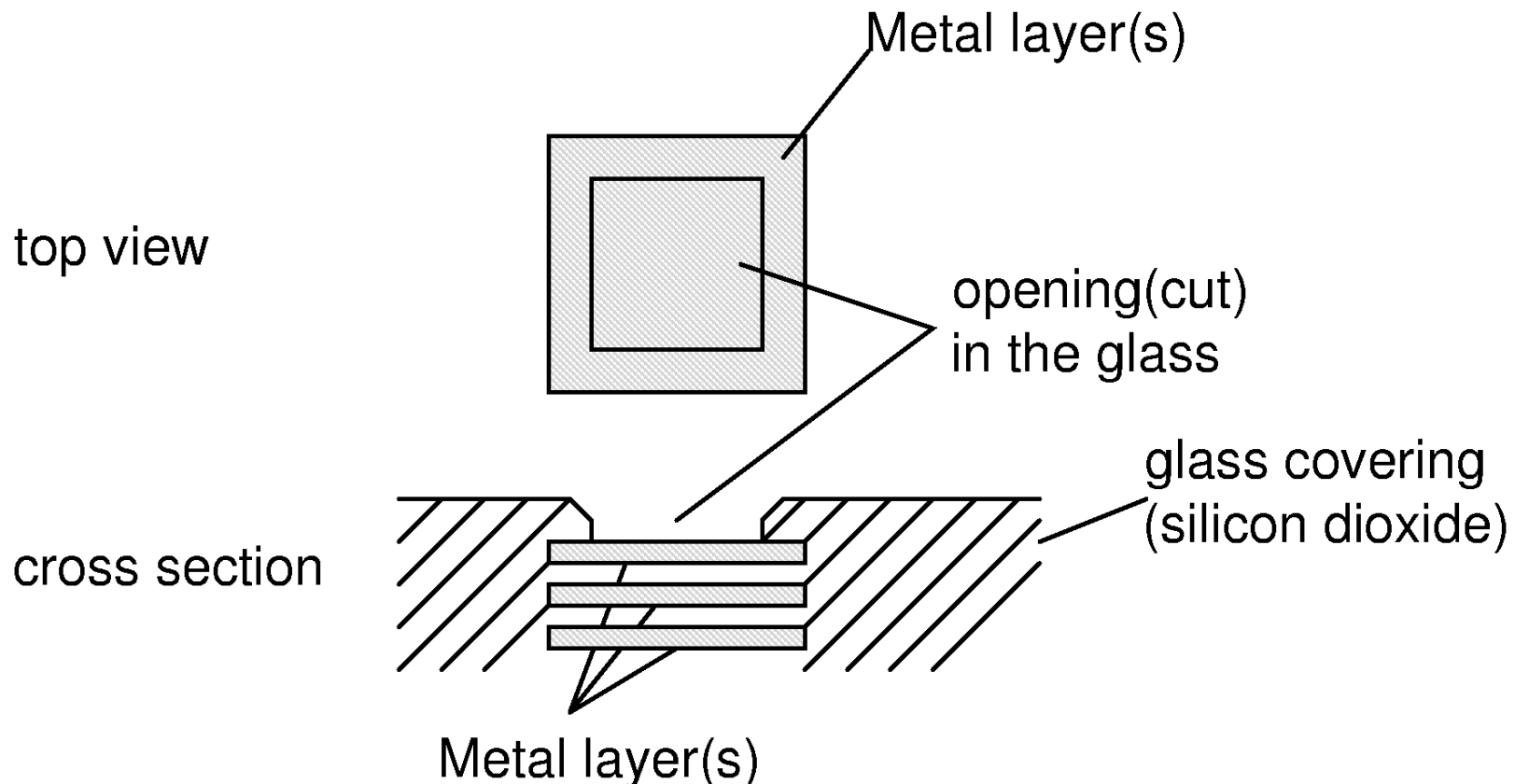- Package cavity size: 310mil(7.75mm, for 28pin and 40pin DIPs)

Bonding diagram example

- Sketch of chip inside the package and associated bondwires
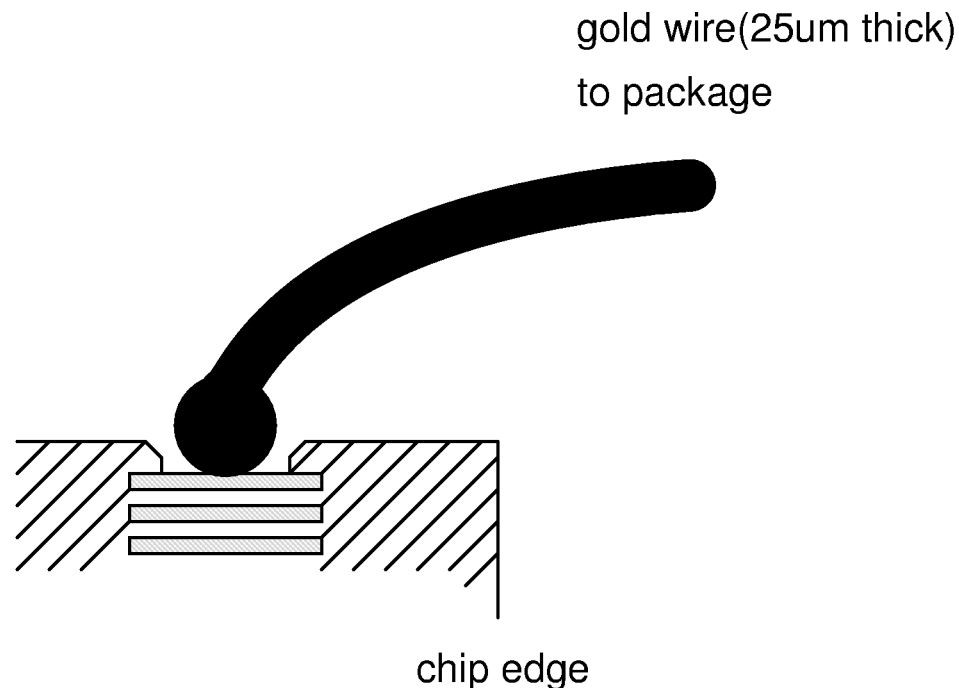- Clearly show the "north" of the chip and package orientation

CHIP

310mil(7.75mm)

CHIP

1.5mm

3mm

Chip bondpads

- Pads: connection points to the outside world

top view

Metal layer(s)

opening(cut)
in the glass

cross section

glass covering
(silicon dioxide)

Metal layer(s)

Chip bondpads

- Input/outputs on opposite sides
- Shorter wires(bondwire+package) for critical signals

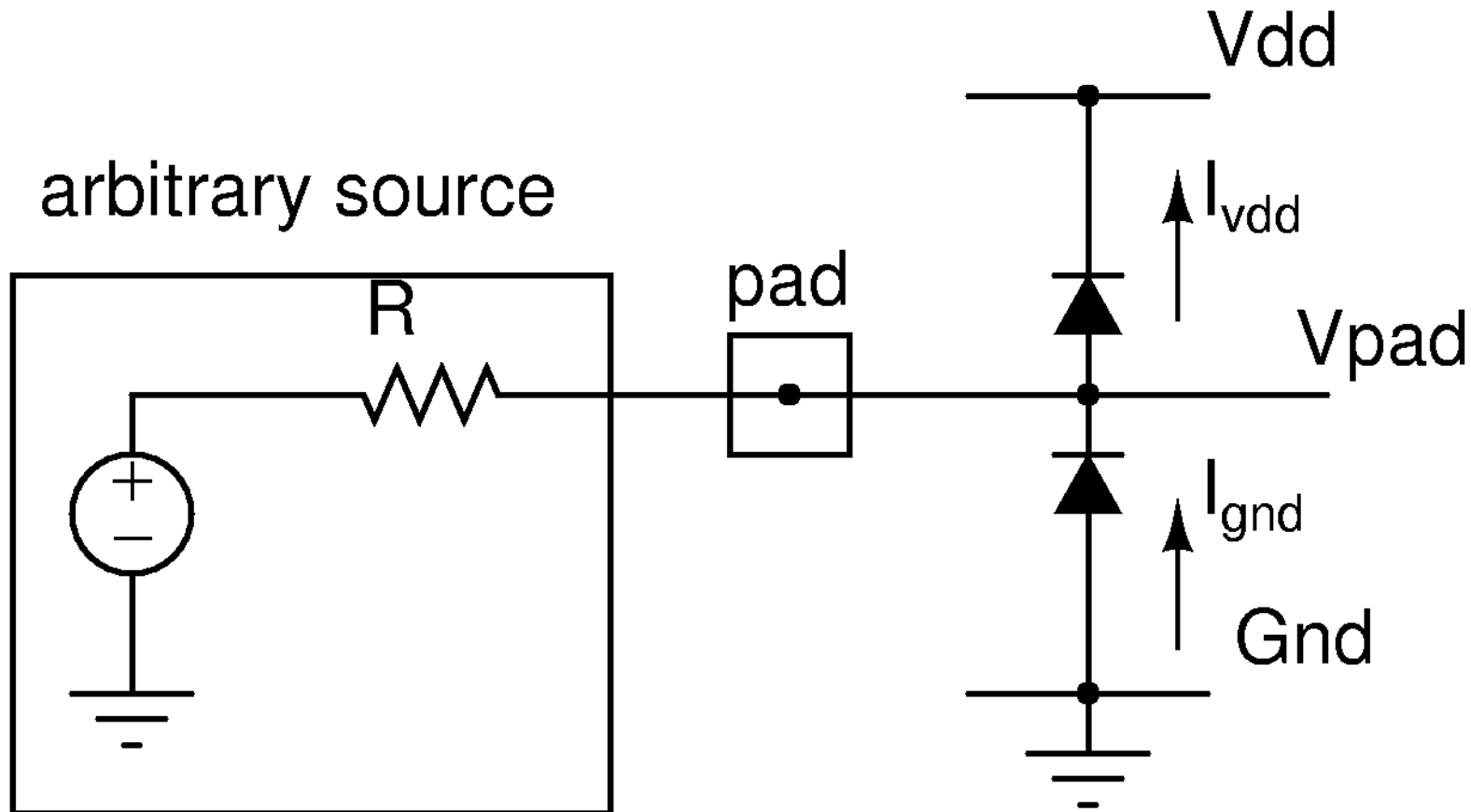gold wire(25um thick)

to package

chip edge

AMI050 pads

- Readymade layouts available
- 1.5mmx1.5mm padframe available
  - Pad rows
  - Corner pieces
  - VDD/GND lines for ESD protection connections
- Make 3mmx1.5mm from the above padframe
- Pads
  - GND(PadGnd)
  - VDD(PadVdd)
  - Digital input signal(PadIO)
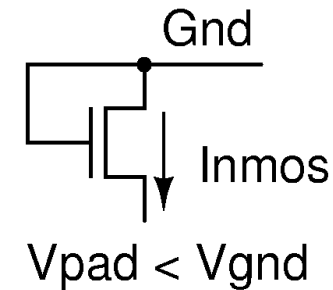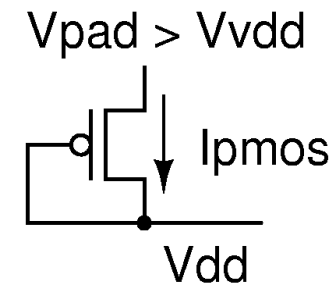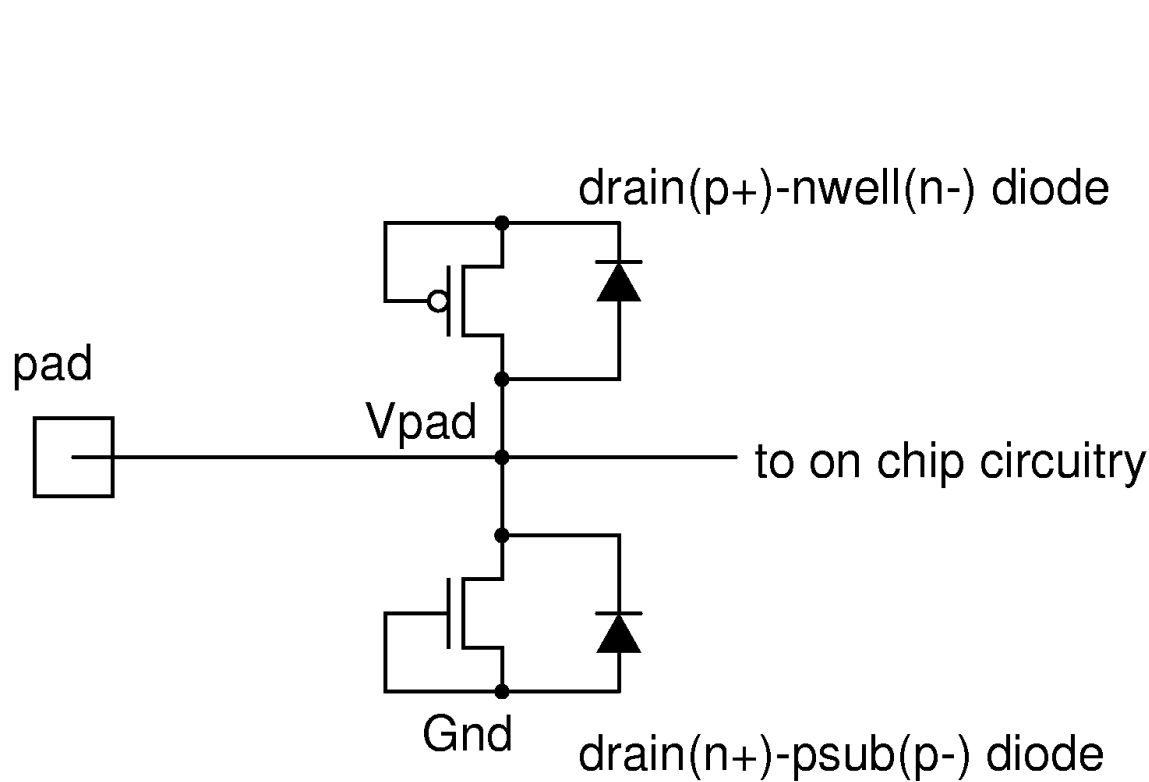 - General purpose(PadAref)

ESD protection

- ESD protection circuitry prevent on chip voltages from going too high or low and damaging the device
  - Manual handling of the device-e.g. During assembly/test

- Clamping circuitry to limit the voltage

- Clamping circuitry presents (nonlinear) capacitance to the circuit-can affect its operation
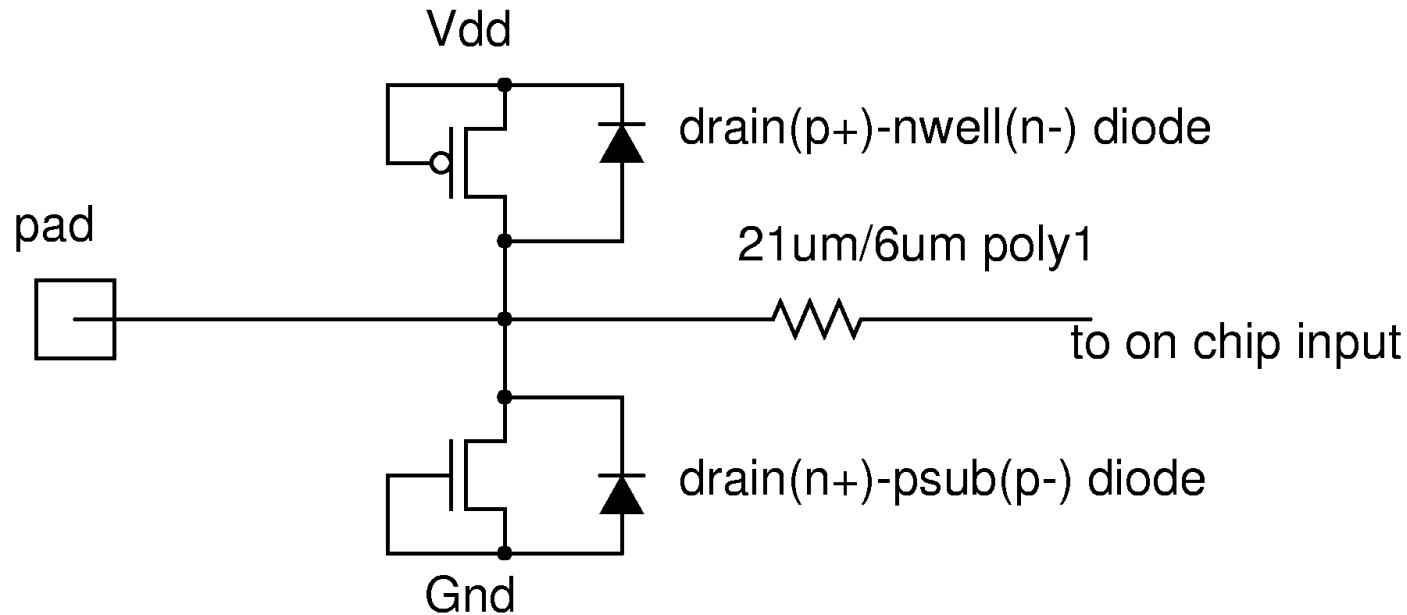
Basic ESD protection circuitry

- Vpad limited to (-0.7V, Vdd+0.7V)

AMI050: ESD protection-general

Vpad > Vvdd

Ipmos

Vdd

drain(p+)-nwell(n-) diode

pad

Vpad

to on chip circuitry

Gnd

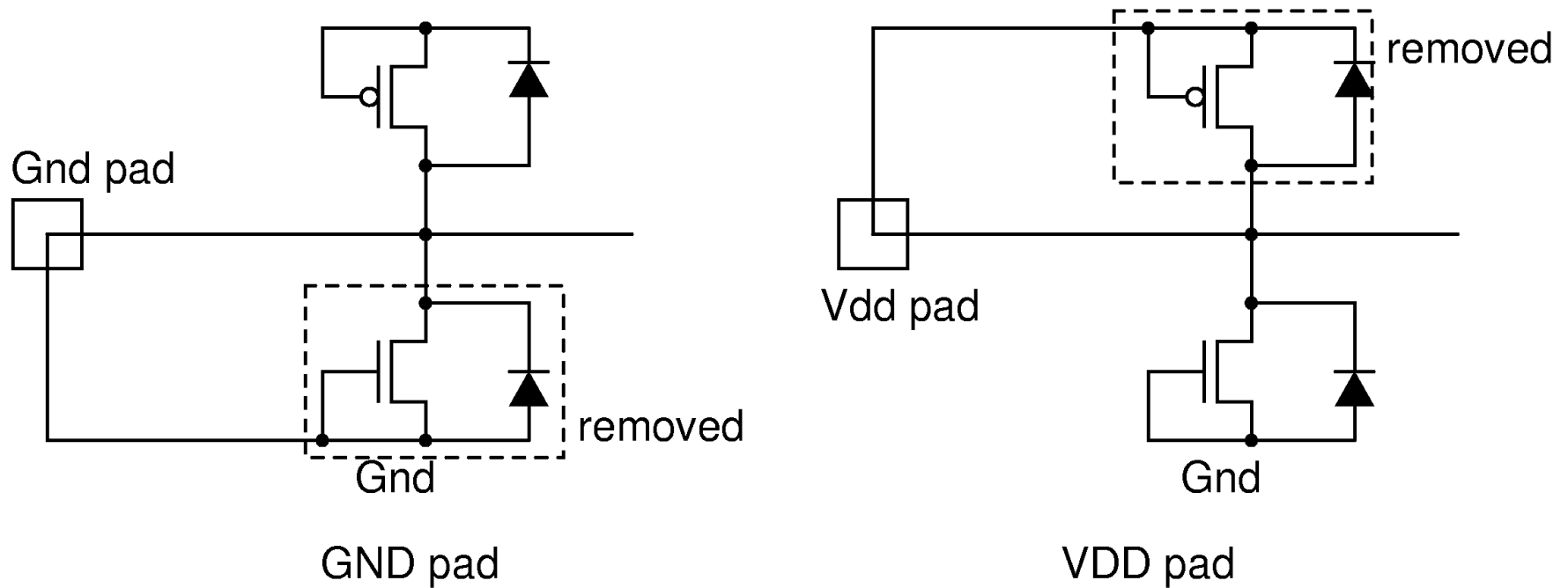drain(n+)-psub(p-) diode

Gnd

Inmos

Vpad < Vgnd

- Mechanisms:
  - Diode current
  - nMOS/pMOS current

AMI050: ESD protection-input

- R at the input slows down voltage buildup at the gate

AMI050: ESD protection-vdd,gnd

Gnd pad

removed

Gnd

removed

GND pad

Vdd pad

Gnd

VDD pad

AMI050: pads

- Pads:
  - PadAref: digital outputs, all analog inputs/outputs
  - PadIO: digital inputs
  - PadVdd: Vdd
  - PadGnd: Gnd
- Use only the above pads
- Currently not DRC clean-soon will be so