# Spring 2005; E4332: VLSI Design Laboratory; HW1

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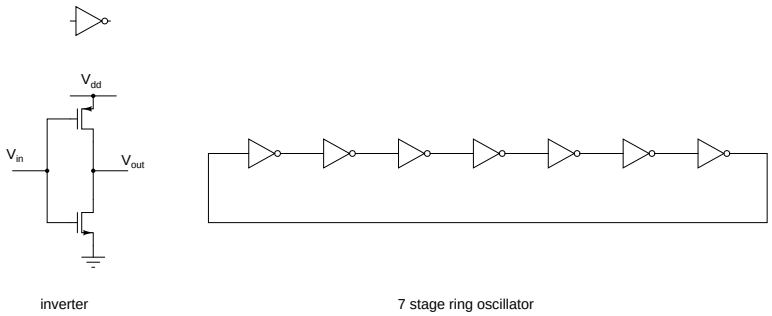


Figure 1:

1. Design a CMOS inverter with minimum length p- and n-channel devices with equal widths.

   (a) Simulate the DC characteristics with a 5 V supply. What $V_{IH}$, $V_{IL}$, assuming that the output low and high voltages away from their ideal values by 10% of the supply voltage.

   (b) Design a 7 stage ring oscillator using the inverters designed above. What is the oscillation frequency? Repeat the simulations with supply voltages from 2.5 V to 4.5 V in increments of 0.5 V and determine the oscillation frequency in each case.

2. Design an inverter with p- and n-channel MOS device widths such that the transition in the inverter's characteristics is in the middle of the 5 V supply rail. Repeat the DC and transient simulations specified in the previous problem with this inverter.

3. Determine "textbook" $I_D$ vs. $V_{DS}$ ($0 \leq V_{DS} \leq 5$ V) curves (Fig. 2(a)) for $V_{GS}$ from 1 V to 5 V in increments of 0.5 V. Do this for transistors of lengths 0.5 $\mu$m, 1 mum, and 2 mum (three sets of curves for p- and n- channel transistors). Use $W/L = 10$ in each case. In each of the curves, determine the slope in the saturation region, and the corresponding output resistance of the transistor.

4. Determine "textbook" $I_D$ vs. $V_{GS}$ ($0 \leq V_{GS} \leq 5$ V) curves (Fig. 2(b)) with $V_{DS} = 3$ V. Do this for transistors of lengths 0.5 $\mu$m, 1 mum, and 2 mum (three sets of curves each for p- and n- channel transistors). Use $W/L = 10$ in each case. From the curves, determine the current factors $K_{n,p}$ and the threshold voltages $V_{THN}$, $V_{THP}$.

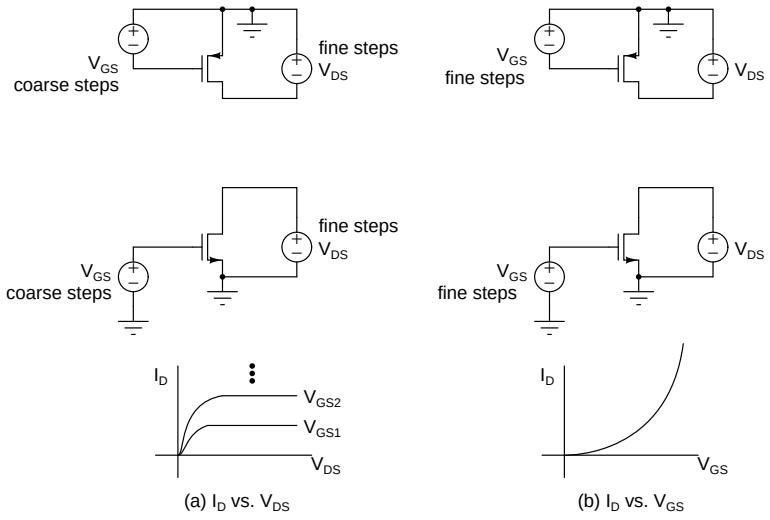


Figure 2:

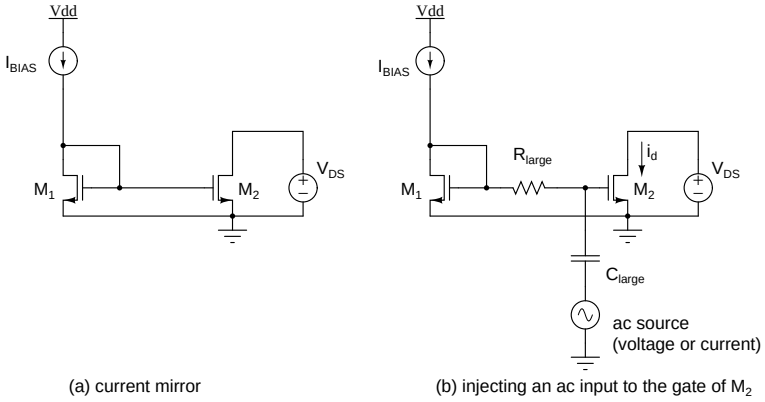


Figure 3:

5. For the circuit in Fig. 3, carry out a parametric simulation as $I_{in}$ from $1\,\mu$A to $100\,\mu$A in 7 logarithmically spaced steps. Plot a) the DC value of $V_{GS}$, b) the inherent dc gain of the transistor $g_m/g_{ds}$, and c) the unity gain frequency of the transistor gain. For c), you need to do a parametric ac analysis. Do this for n- and p-channel transistors of 0.5 $\mu$m and 2 $\mu$m channel lengths. Use $W/L = 10$ in each case.