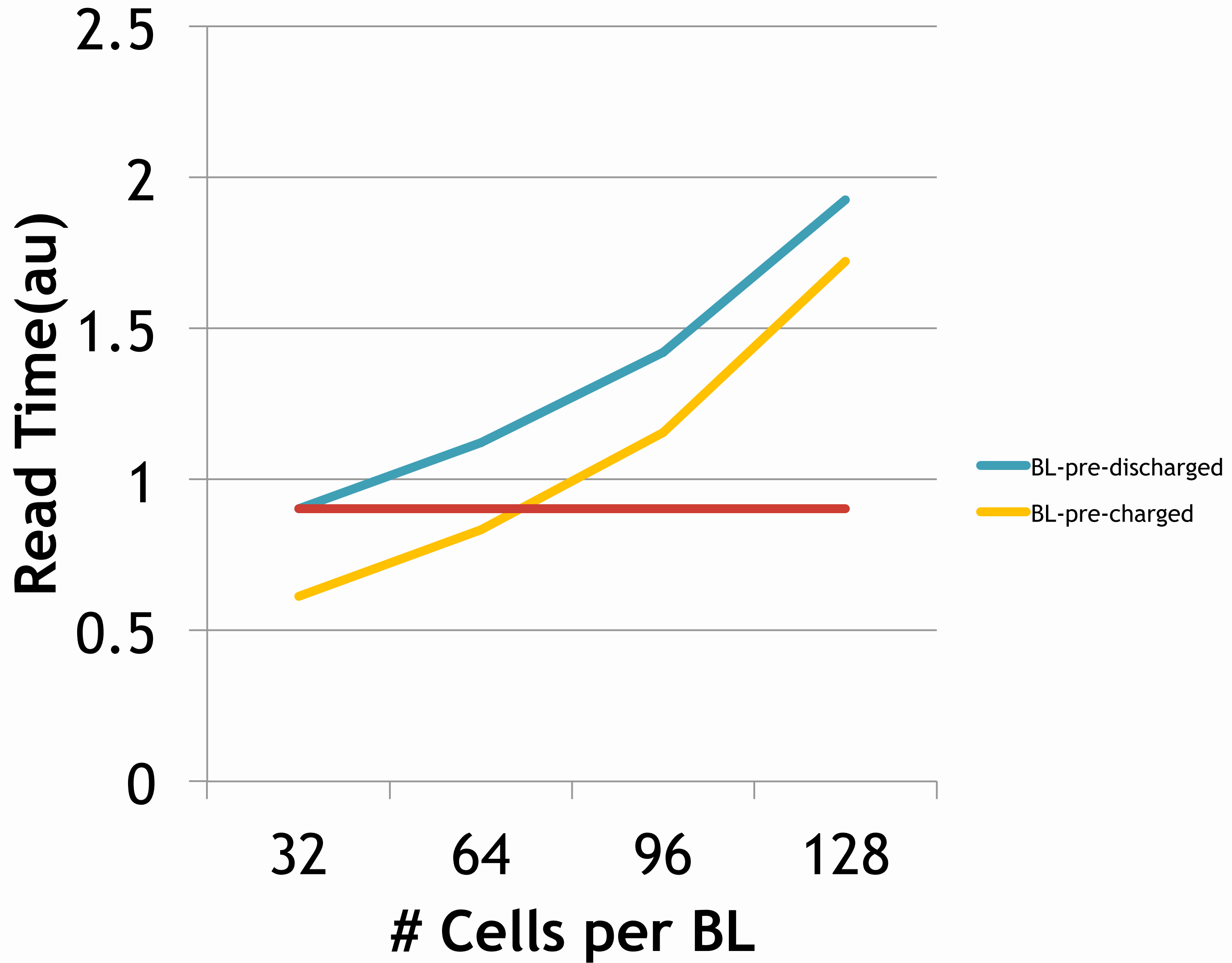
A Fast Area Efficient Sense-Amp (Case Study)

G. Fredeman et al., “A 14 nm 1.1 Mb Embedded DRAM Macro With 1 ns Access,”
in IEEE Journal of Solid-State Circuits, vol. 51, no. 1, pp. 230-239,
Jan. 2016. doi: 10.1109/JSSC.2015.2456873

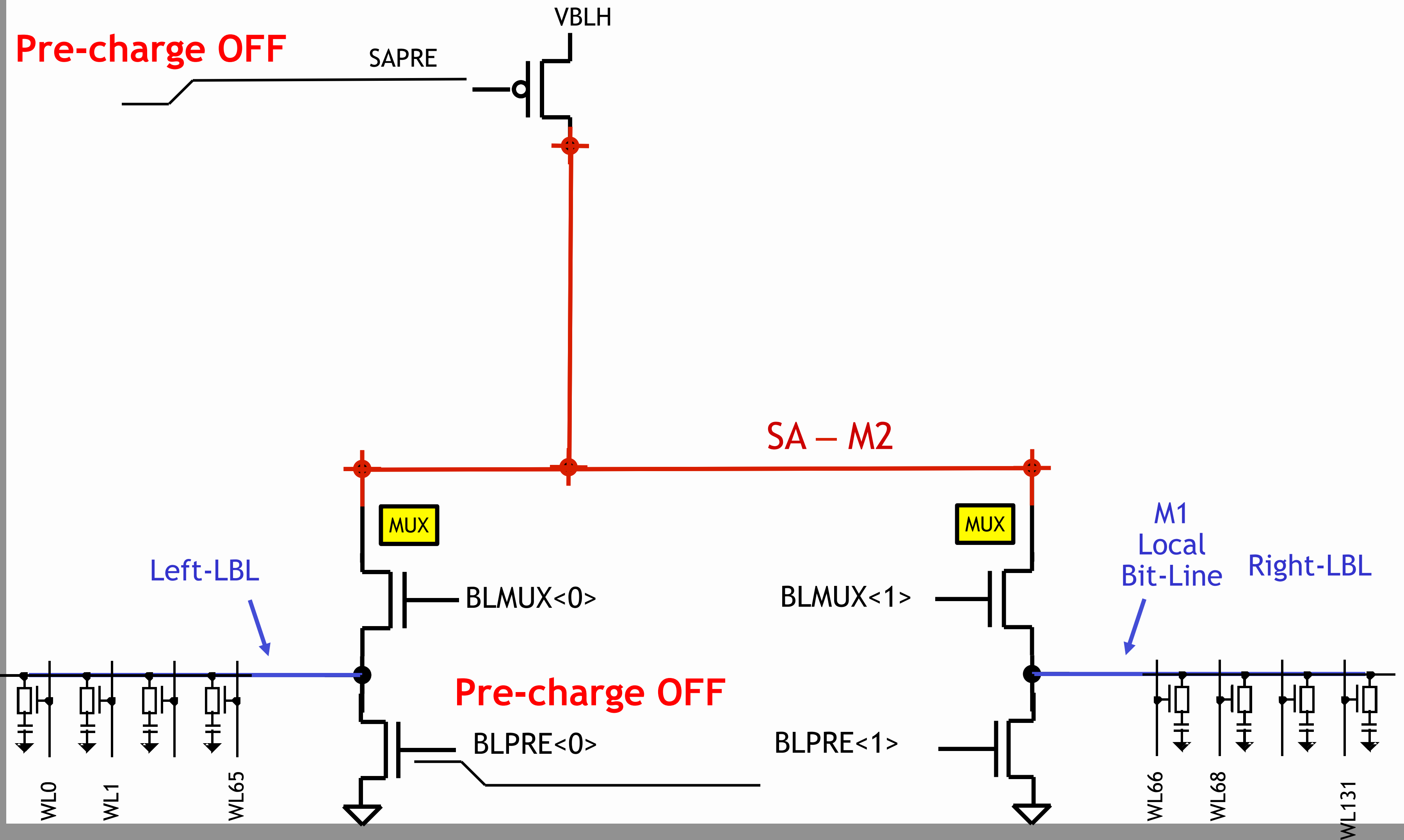
Problems with Micro Sense Amp

- By default the Sense Amp reads a 0
- Access transistor has to pull the LBL HIGH to read 1
  - Asymptotic charge up to High since Vgs keeps reducing
  - Very slow by nature
  - Need to minimize the WLs per BL(33) for performance reasons
- Cannot pre-charge LBL to High
  - Floating Body Effect affects retention
- NMOS (Access Device) is very fast when pulling down to zero
  - Can we make a Sense Amp that reads a one by default?
  - This will allow more WLs per BL

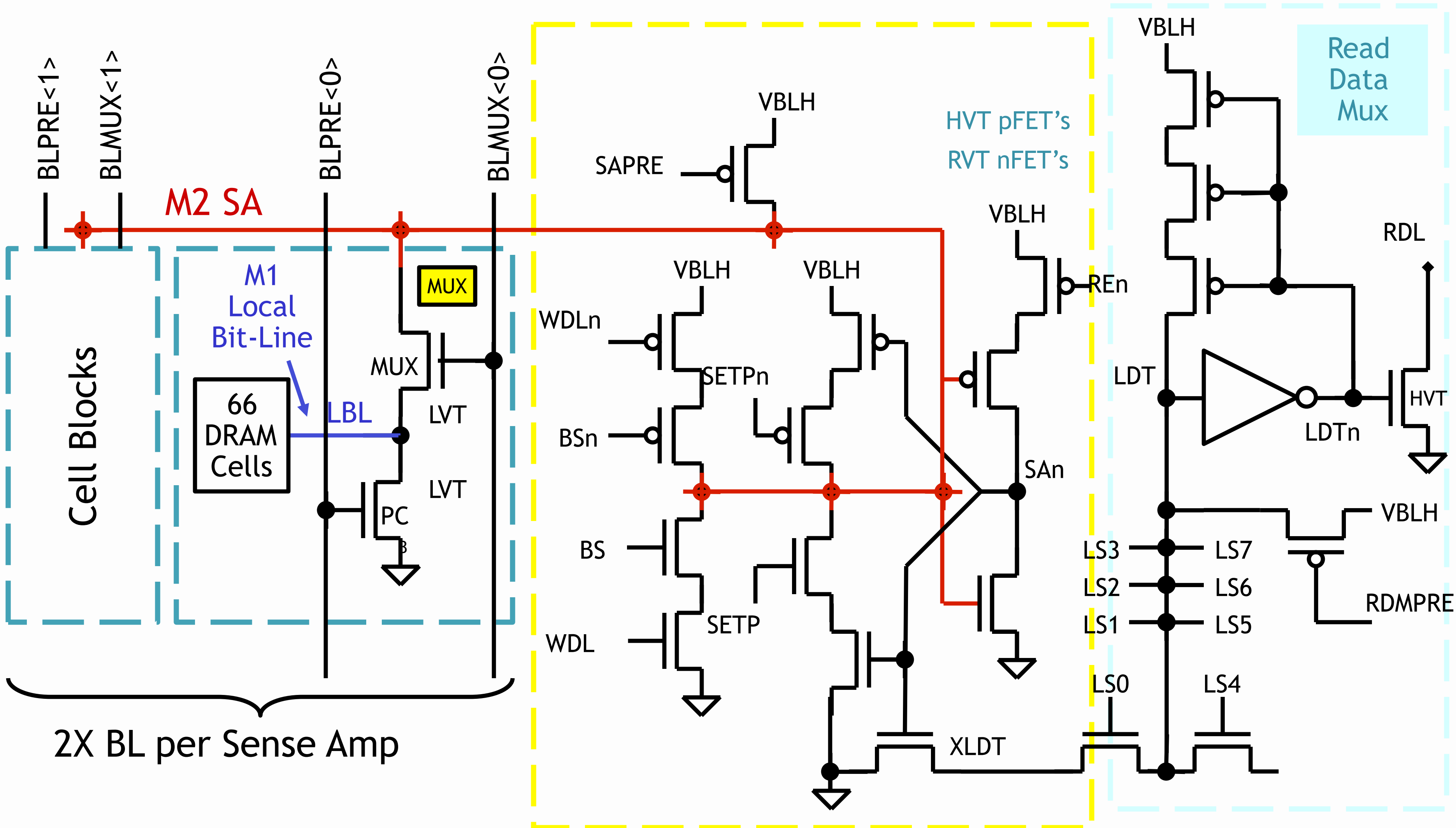
LBL Pre-charge vs Pre-discharge



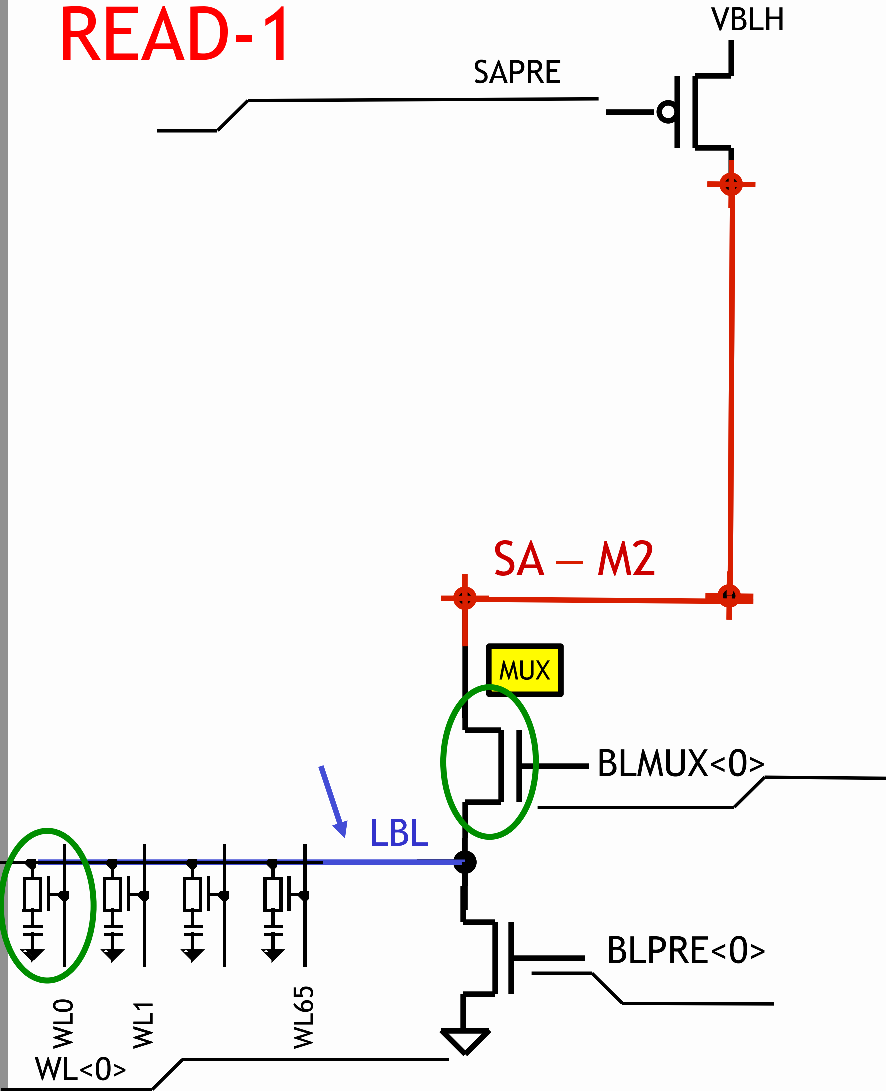
Basic Structure

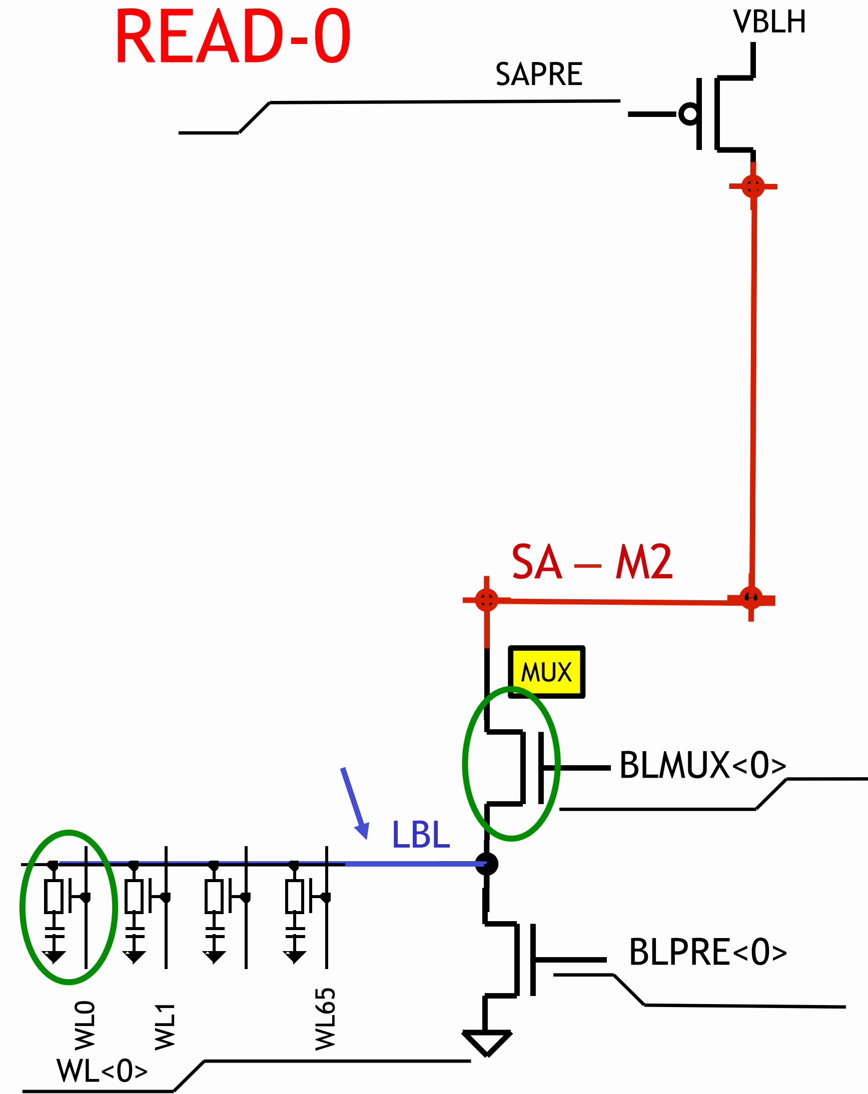


Gated Feedback Sense Amp



Gated Feedback Sense Amp – Construction





Animation

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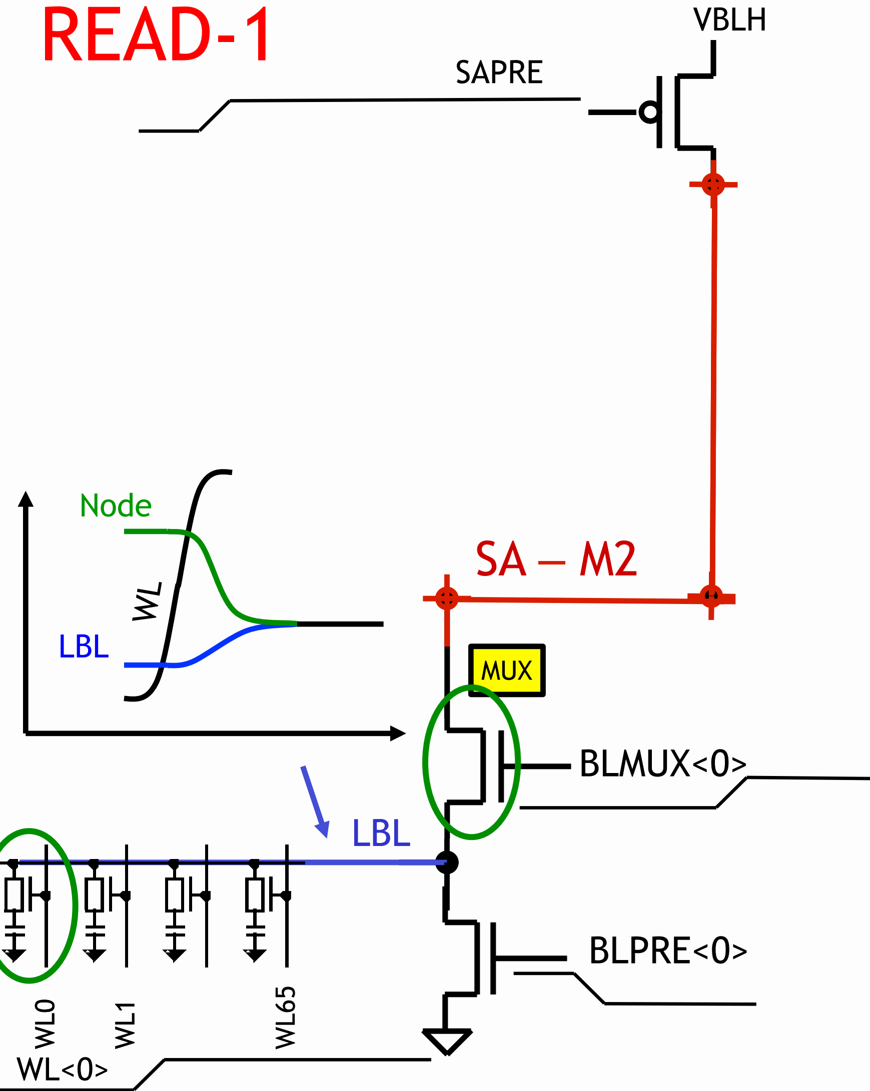
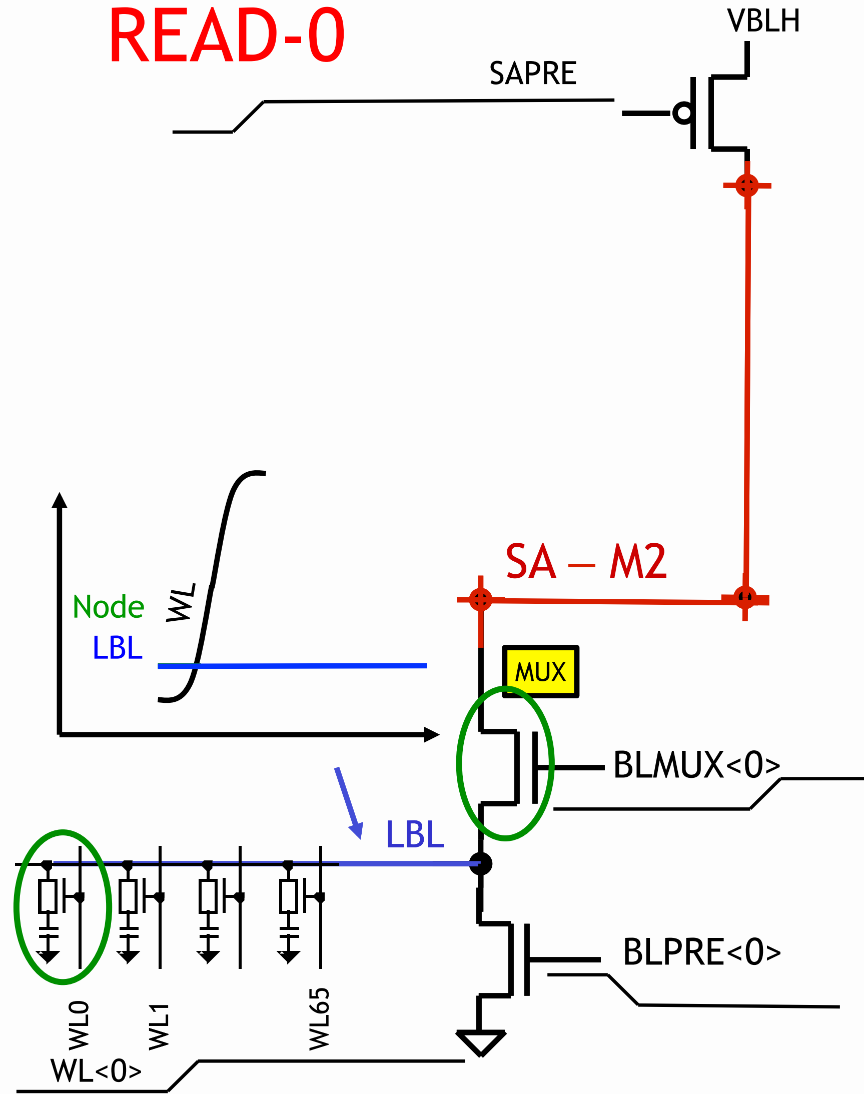


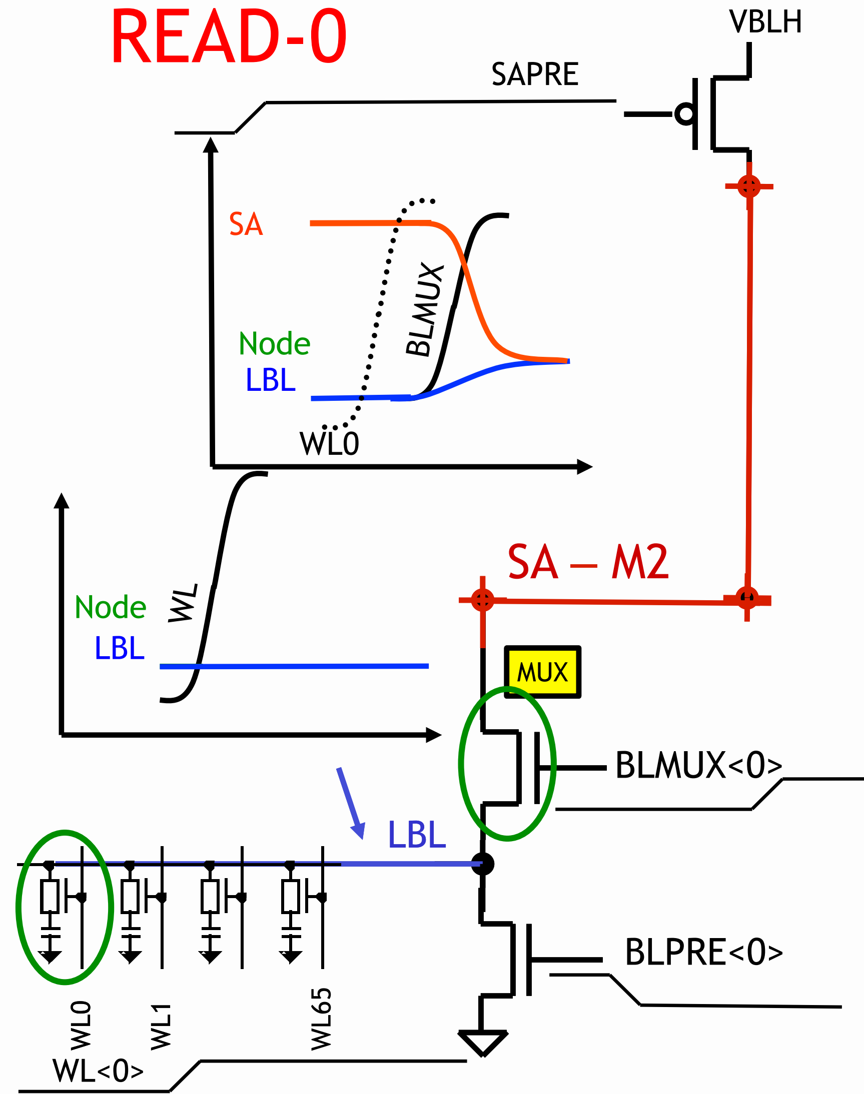


Animation

Gated Feedback Sense Amp - Construction

READ-1

VBLH
SAPRE
SA
Node
BLMUX
LBL
WL0
Node
WL
LBL
SA – M2
MUX
BLMUX<0>
LBL
BLPRE<0>
WL0
WL1
WL65
WL<0>



Animation

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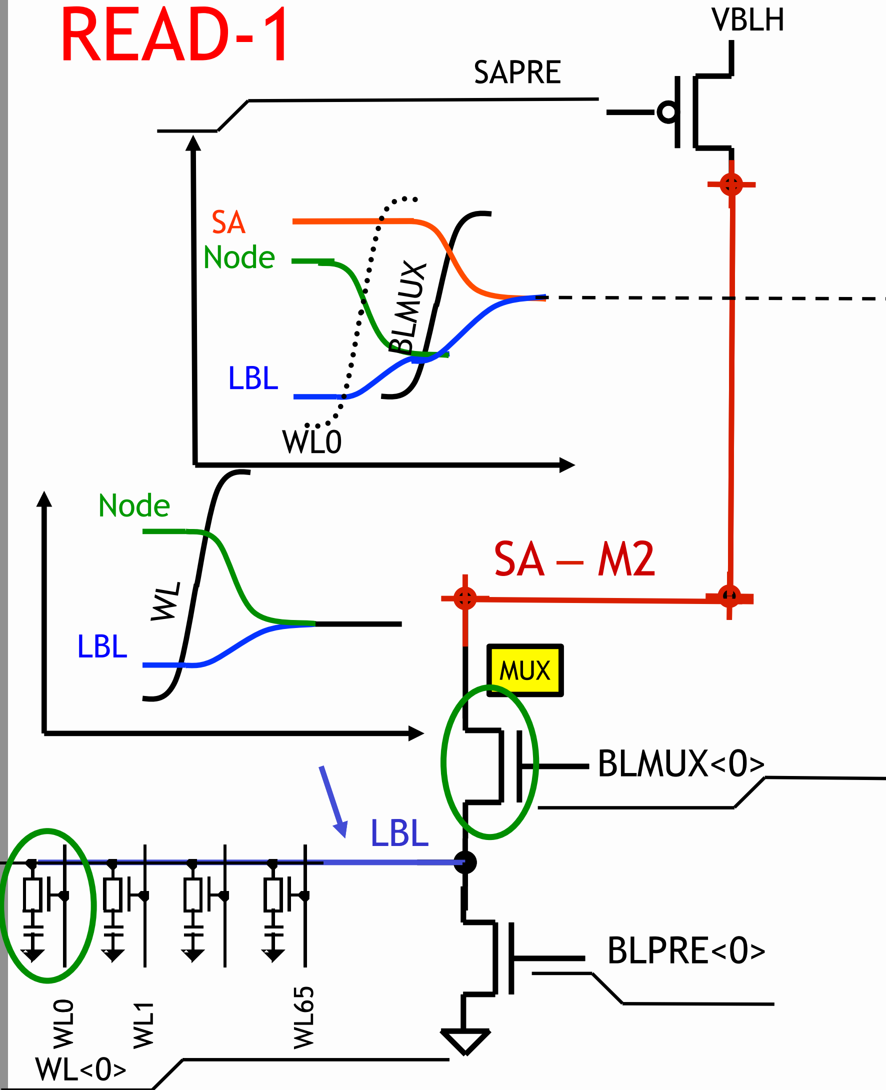

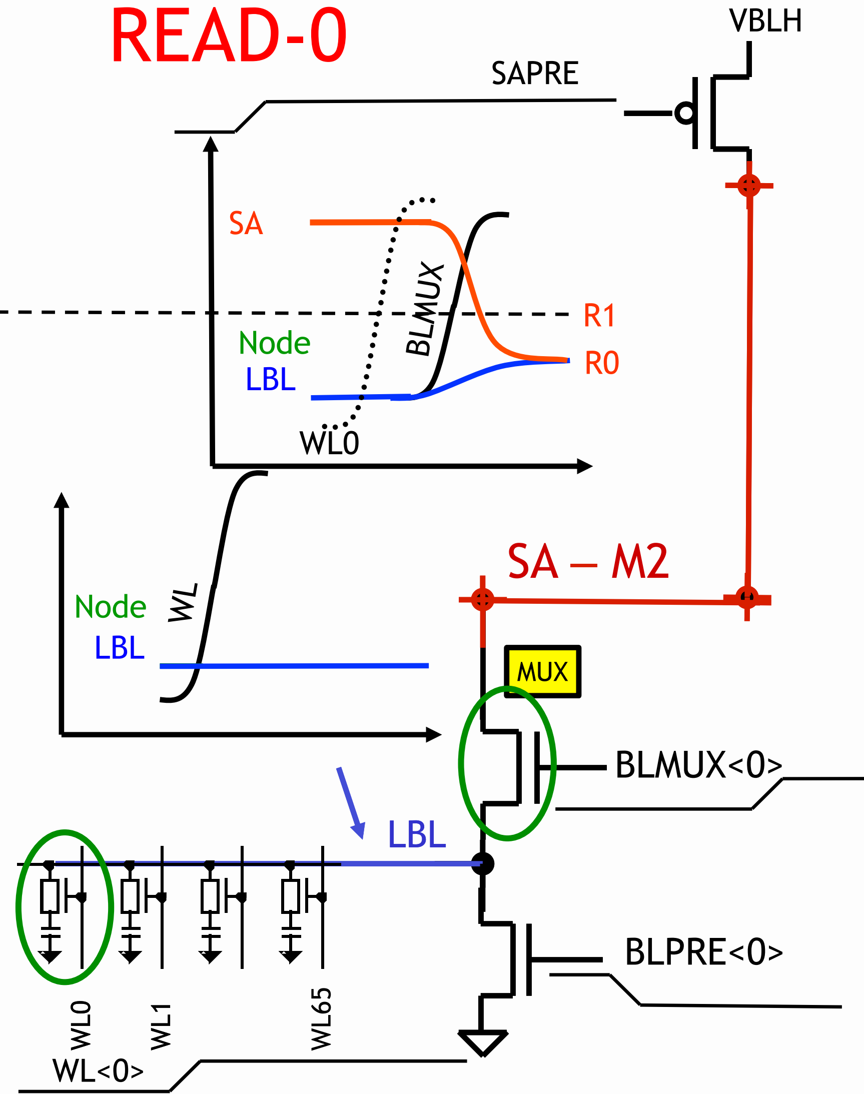

Animation

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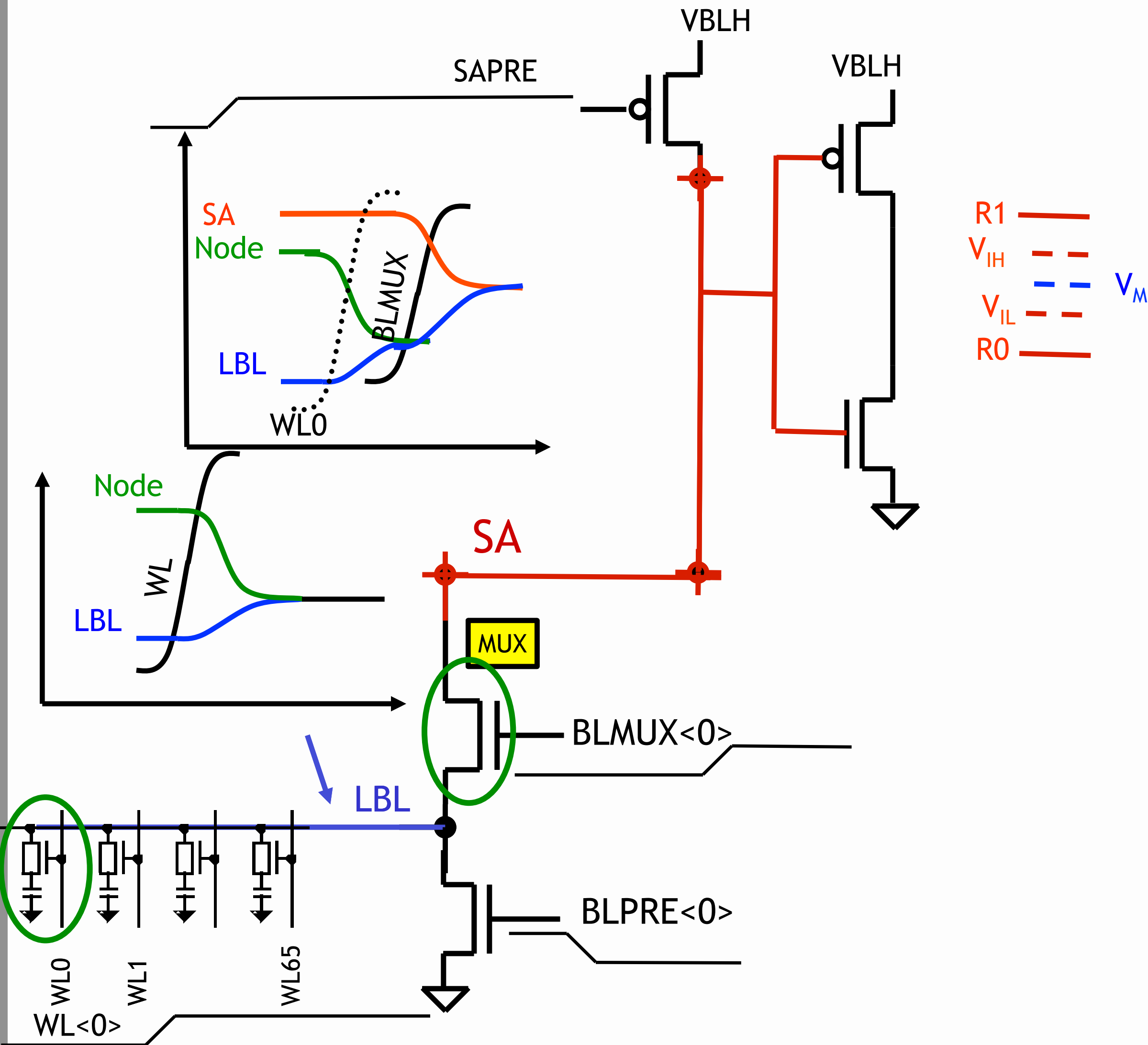

R1

V_{IH}

V_M

V_{IL}

R0

Animation

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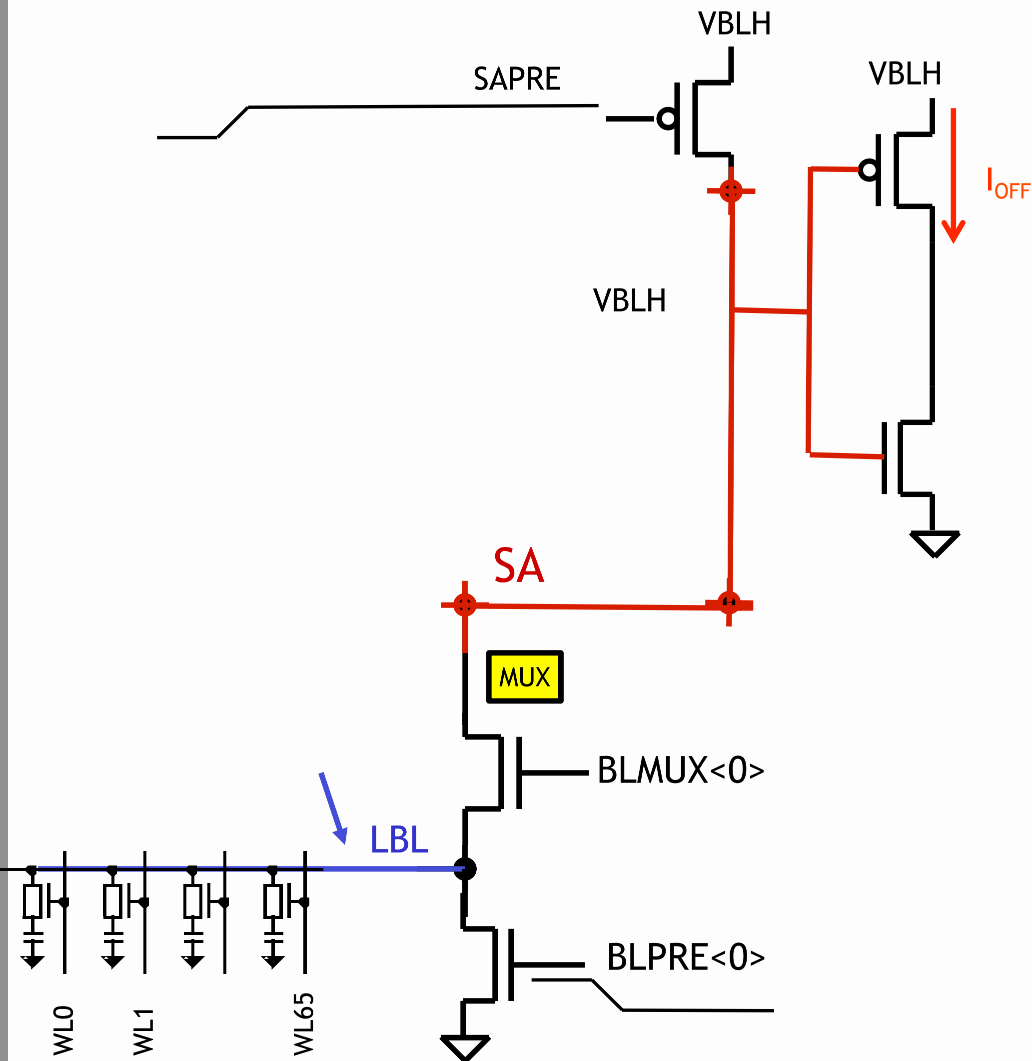

Animation

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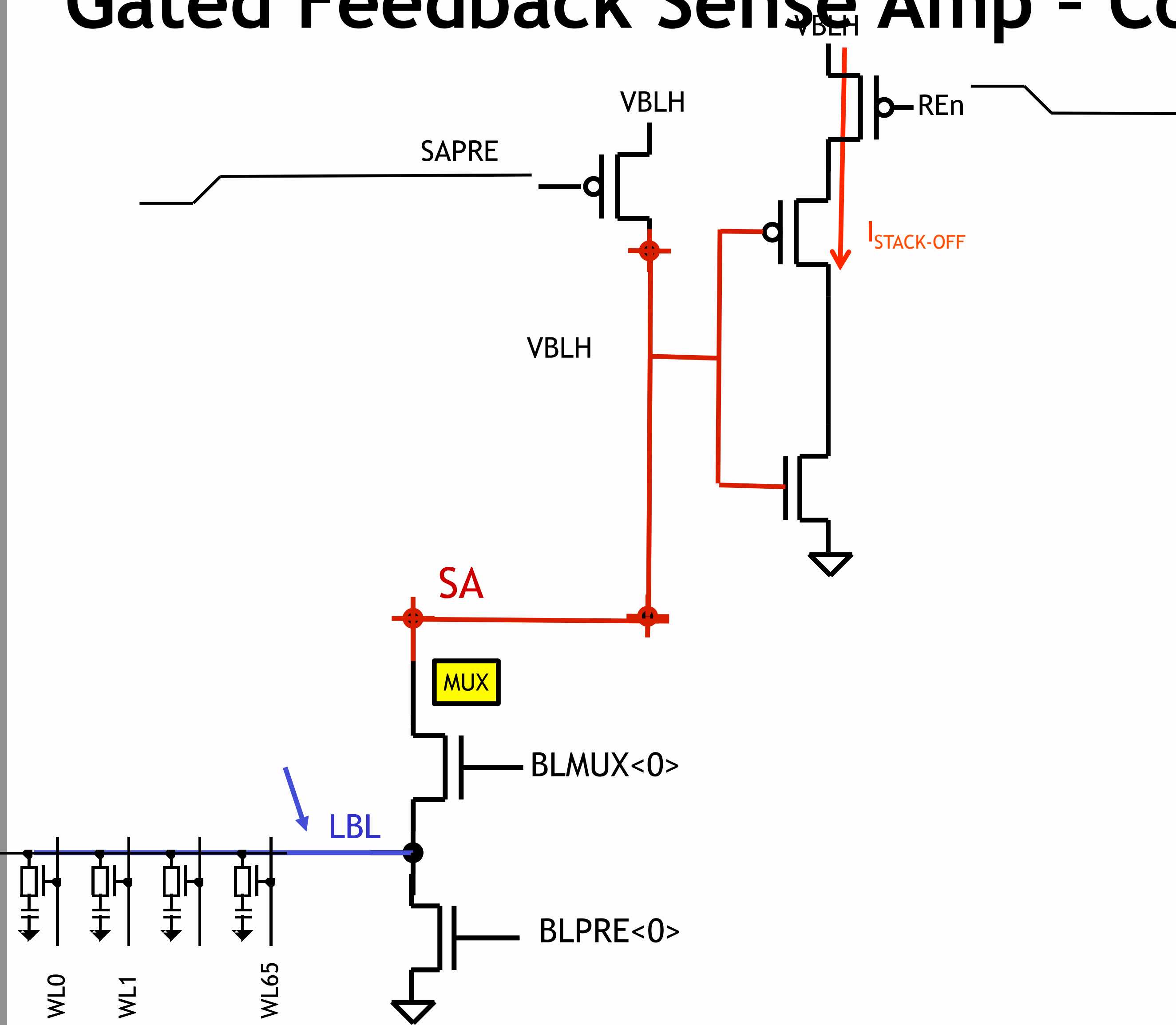

Animation

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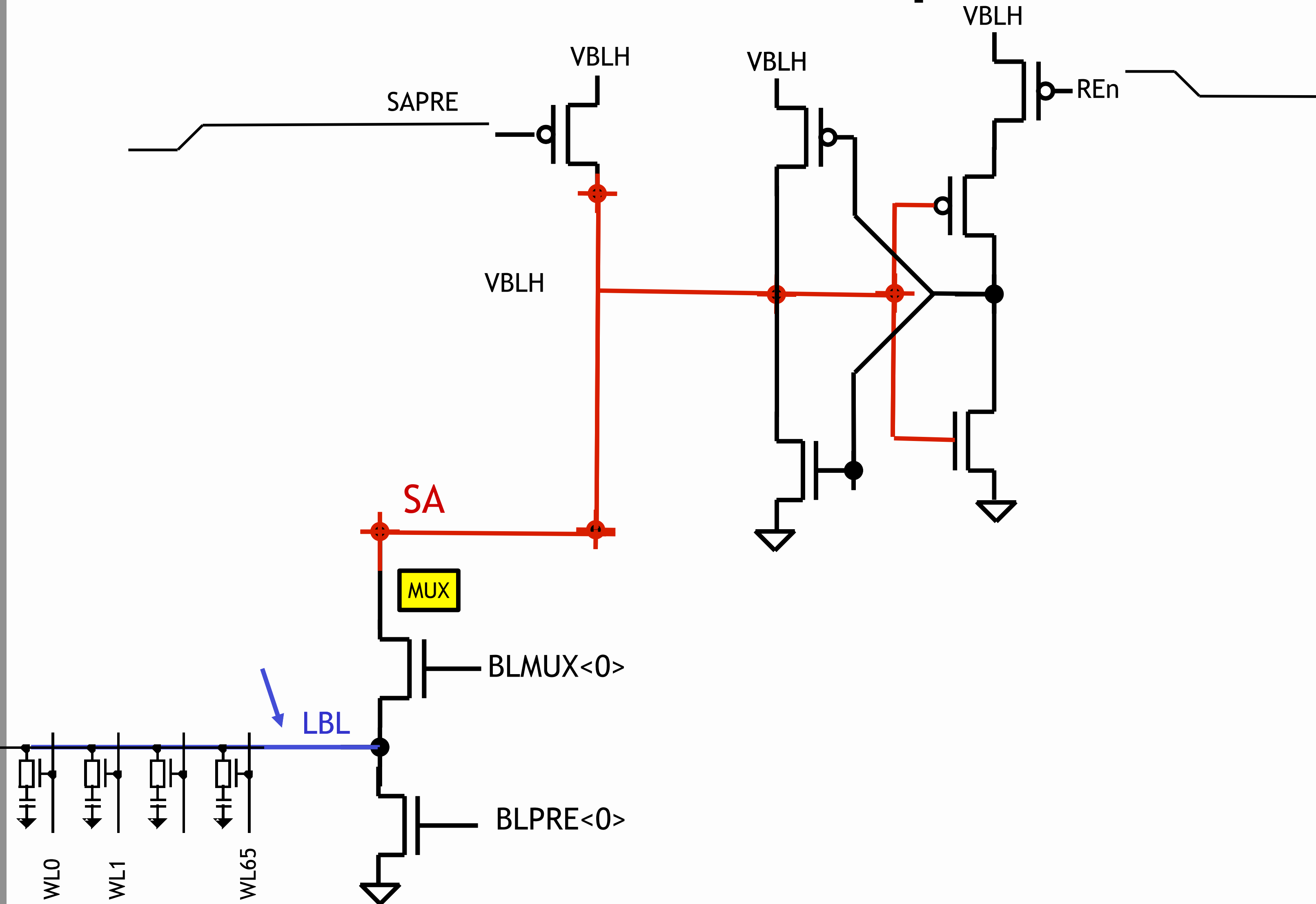

Animation

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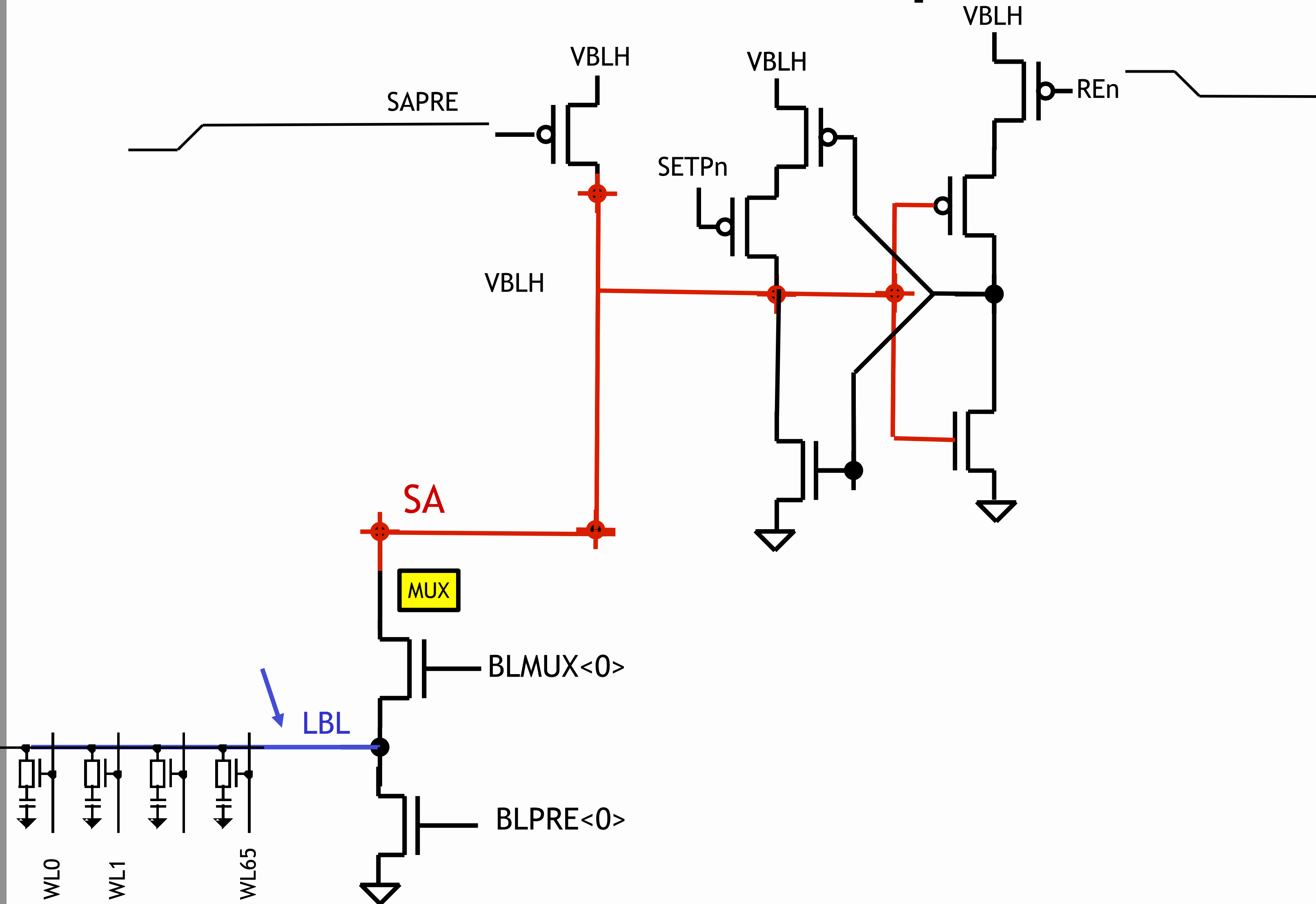
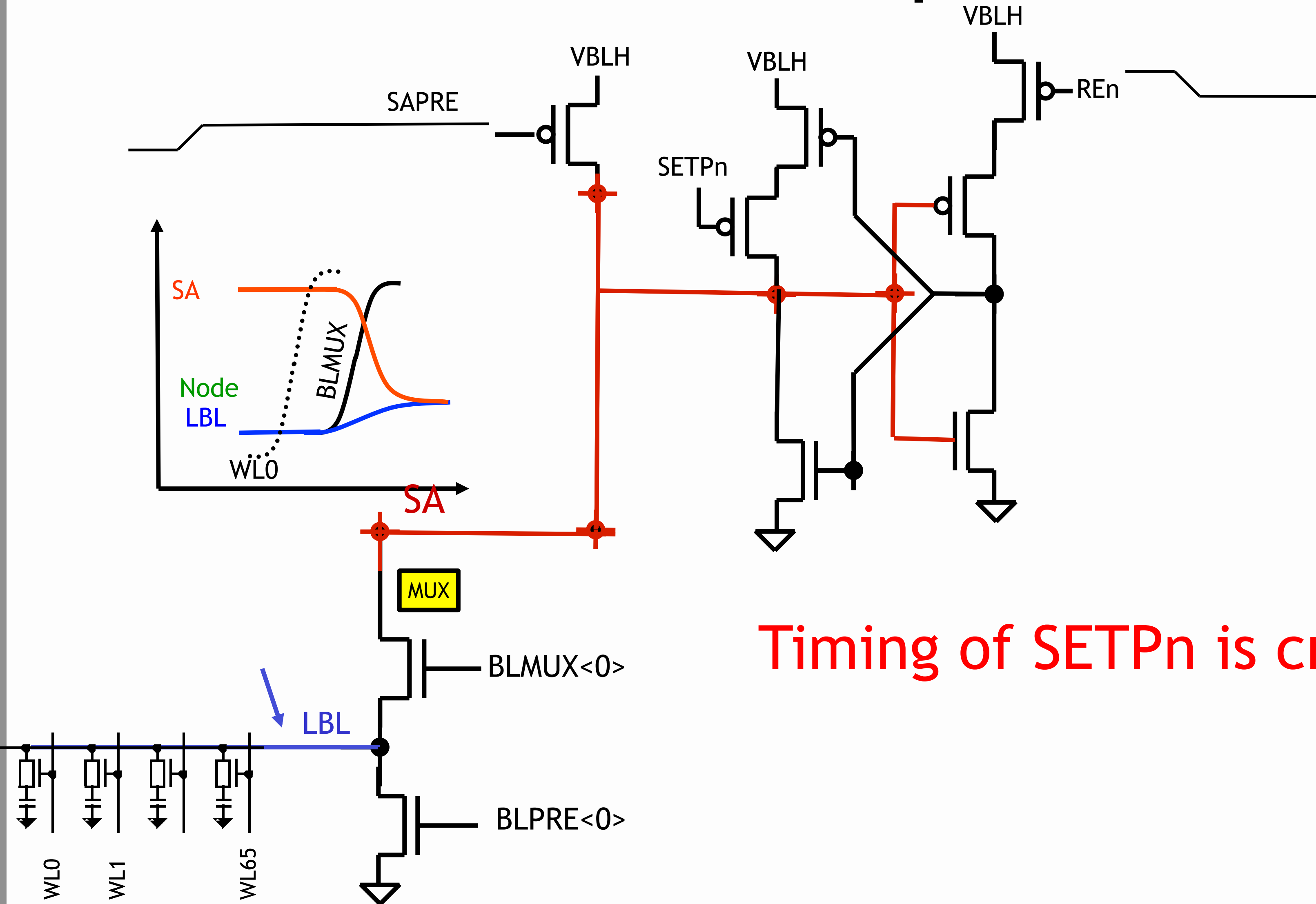


Animation

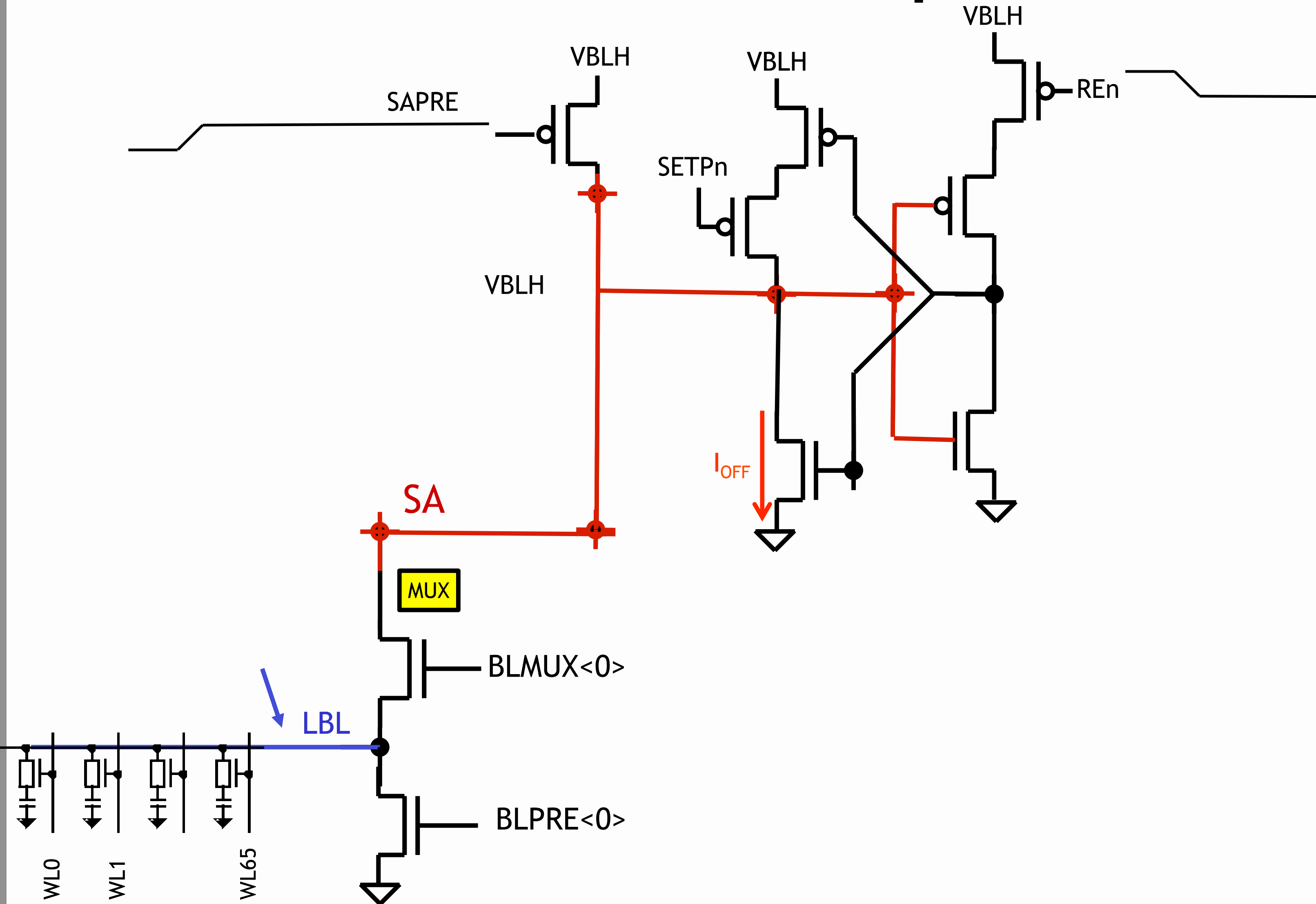
Gated Feedback Sense Amp - Construction



Timing of SETPn is critical

Animation

Gated Feedback Sense Amp - Construction



Animation

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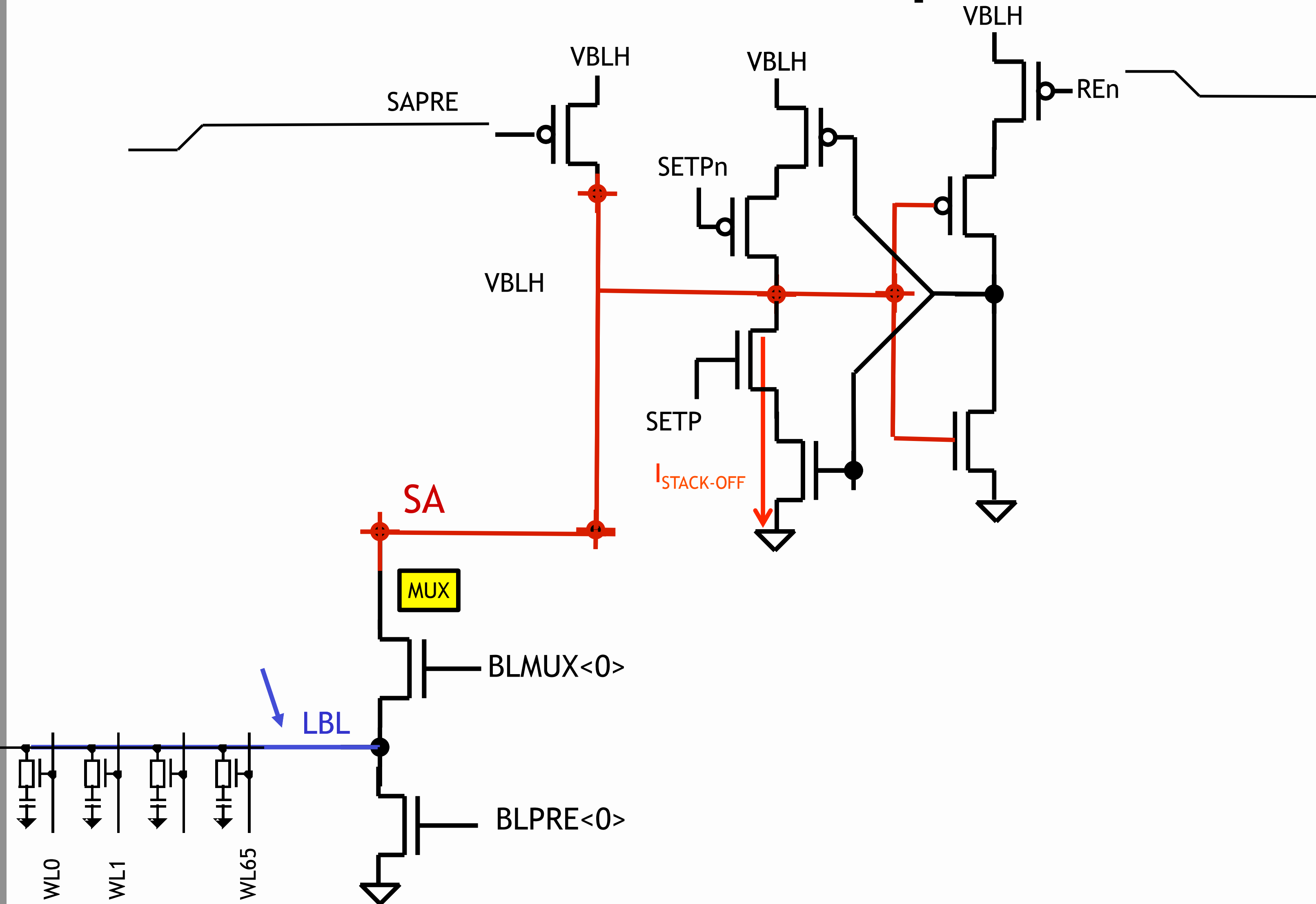

Animation

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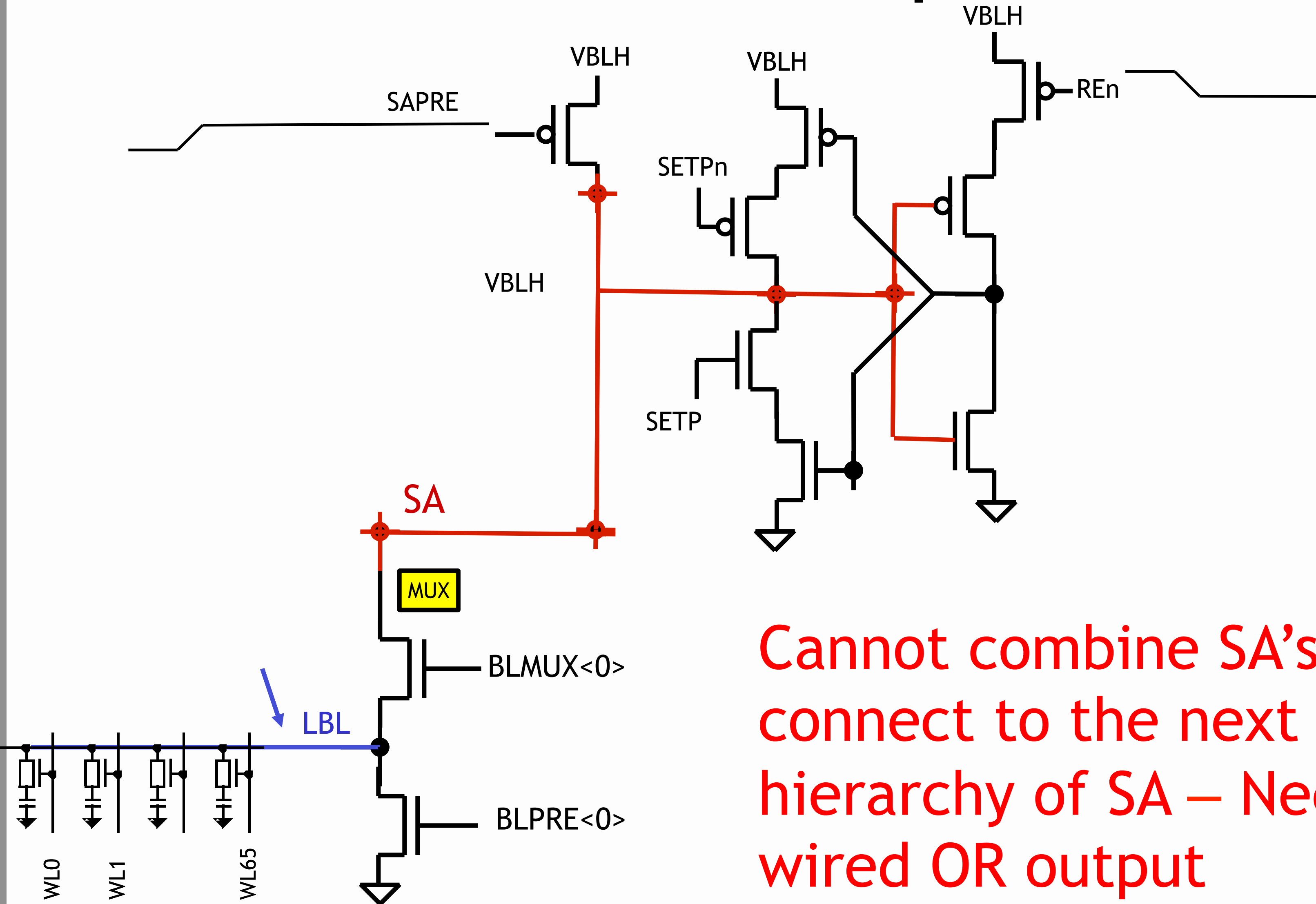
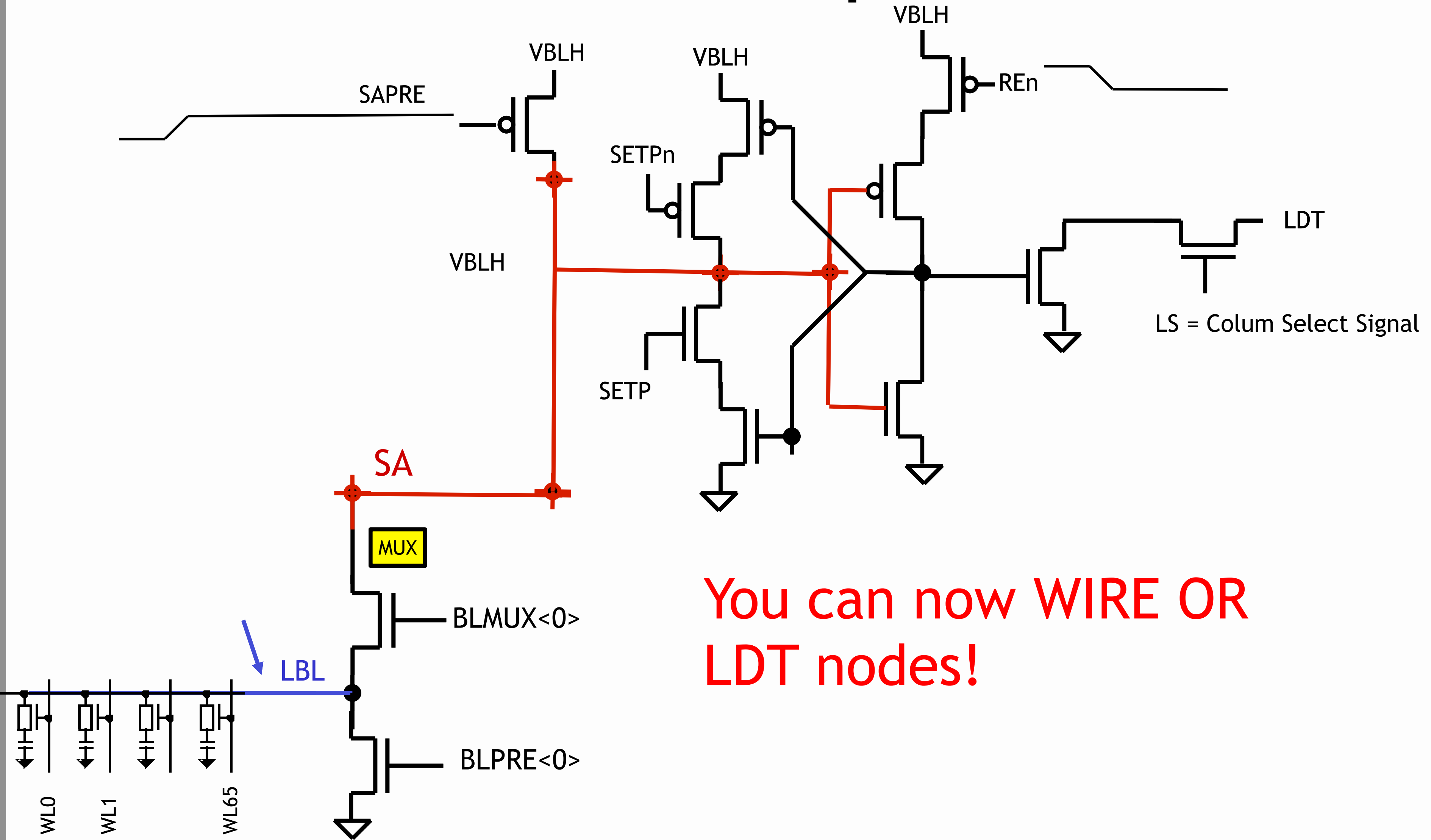


Cannot combine SA's to connect to the next hierarchy of SA – Need a wired OR output

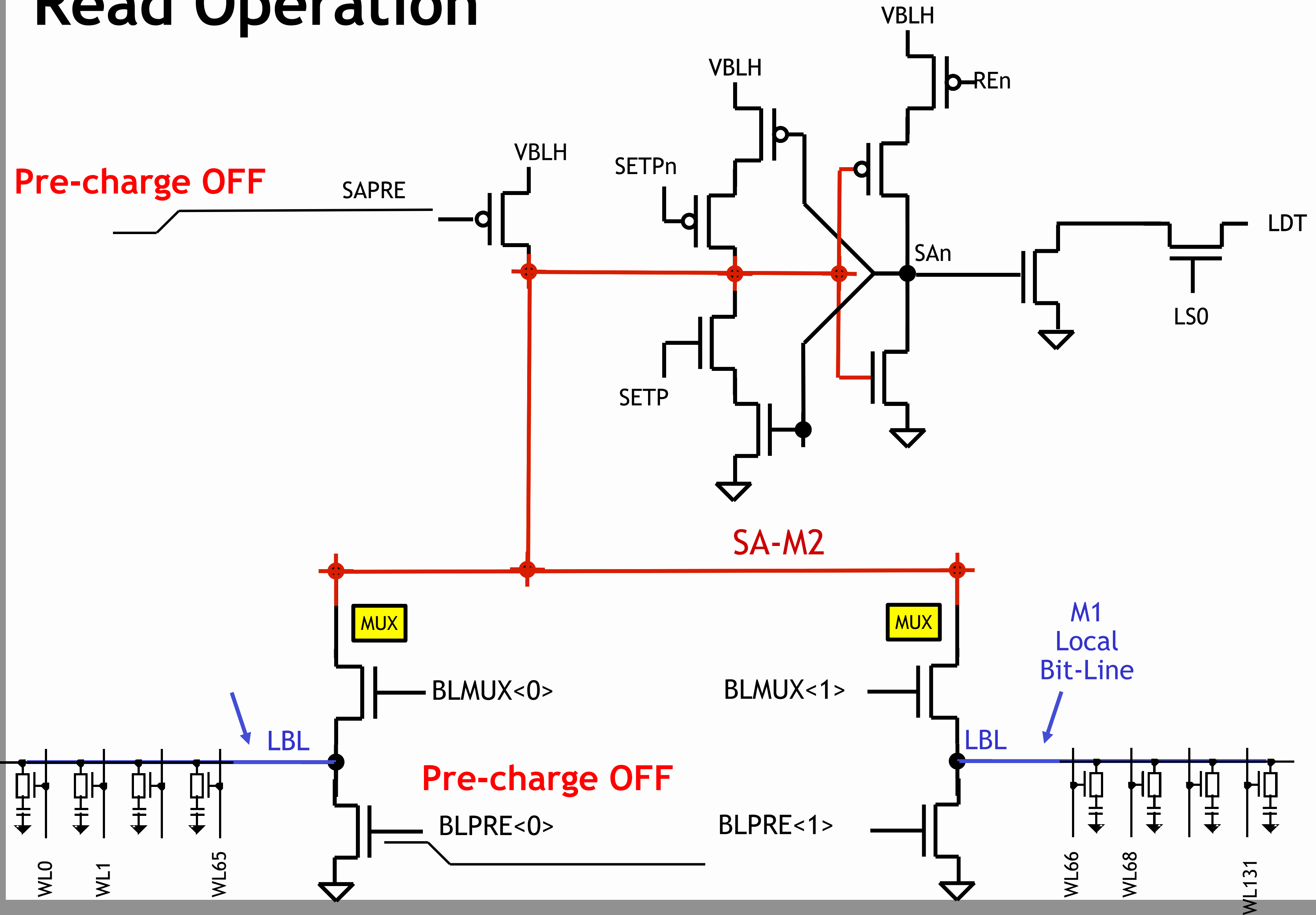
Animation

Gated Feedback Sense Amp - Construction



Animation

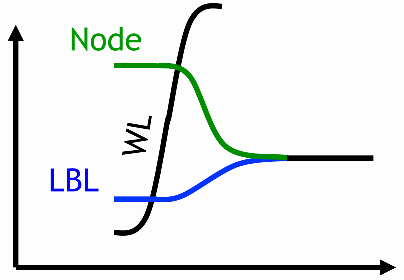
Read Operation



Animation

Read Operation

Turn ON WL



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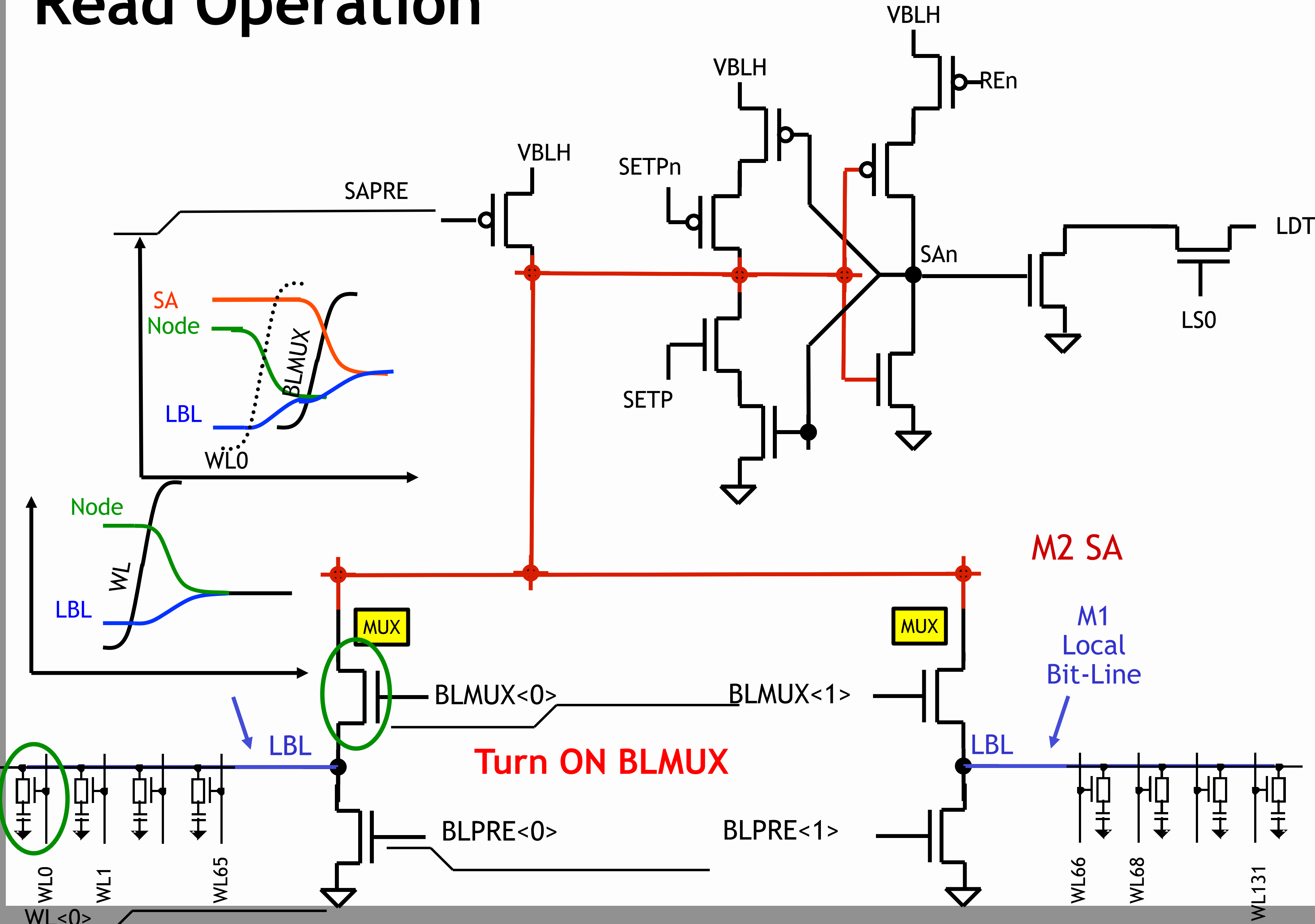
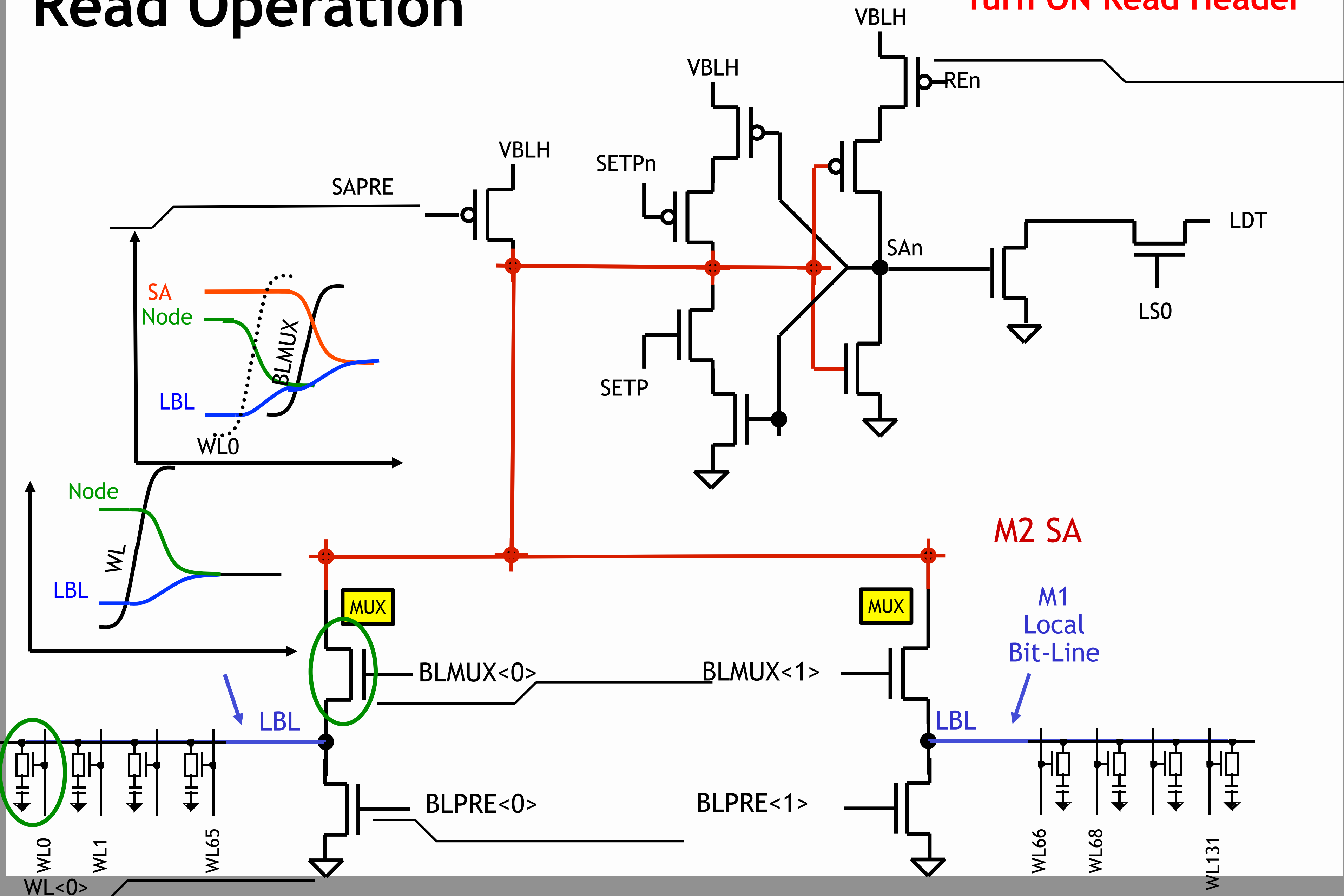


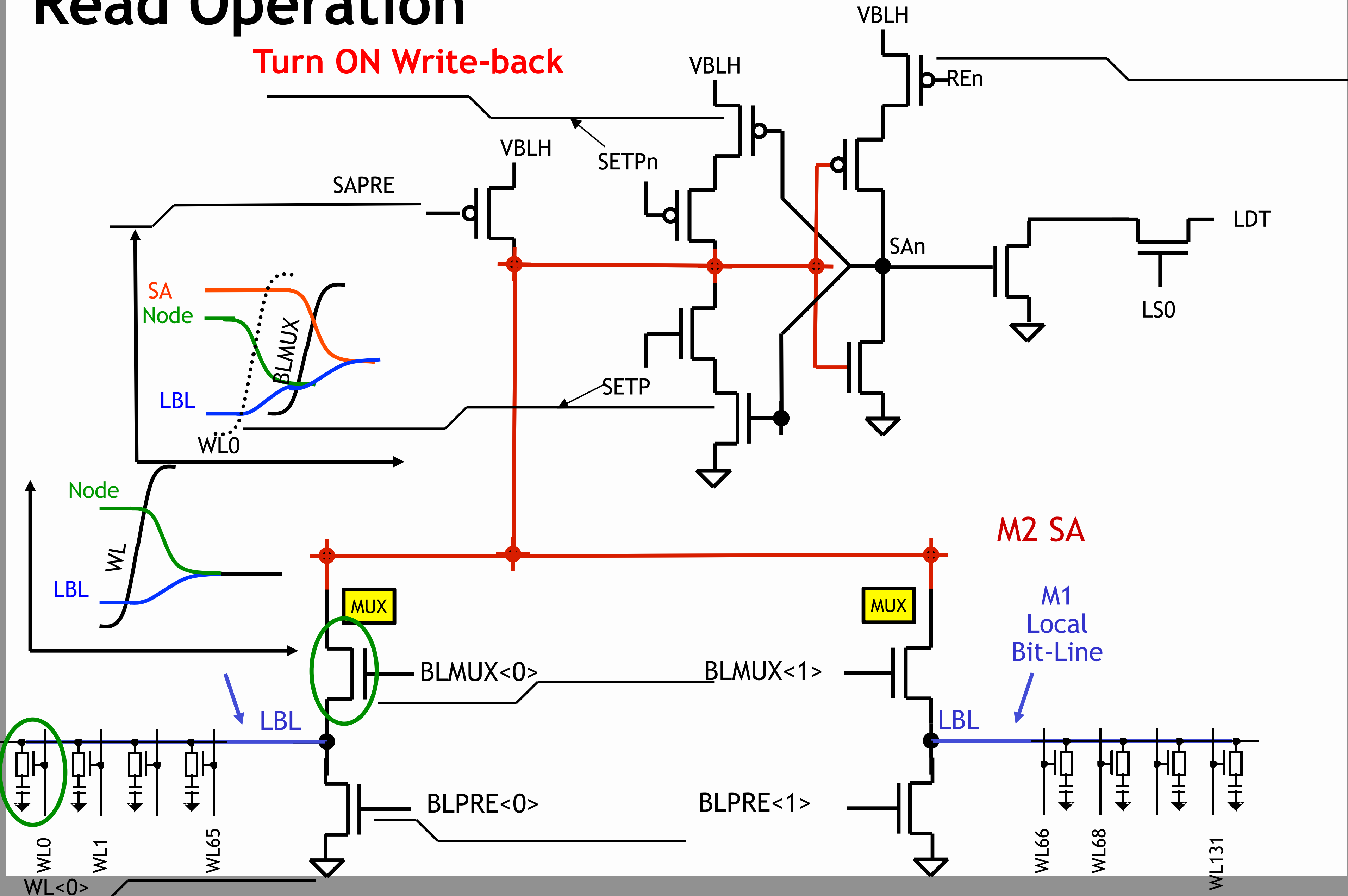
Animation

Read Operation



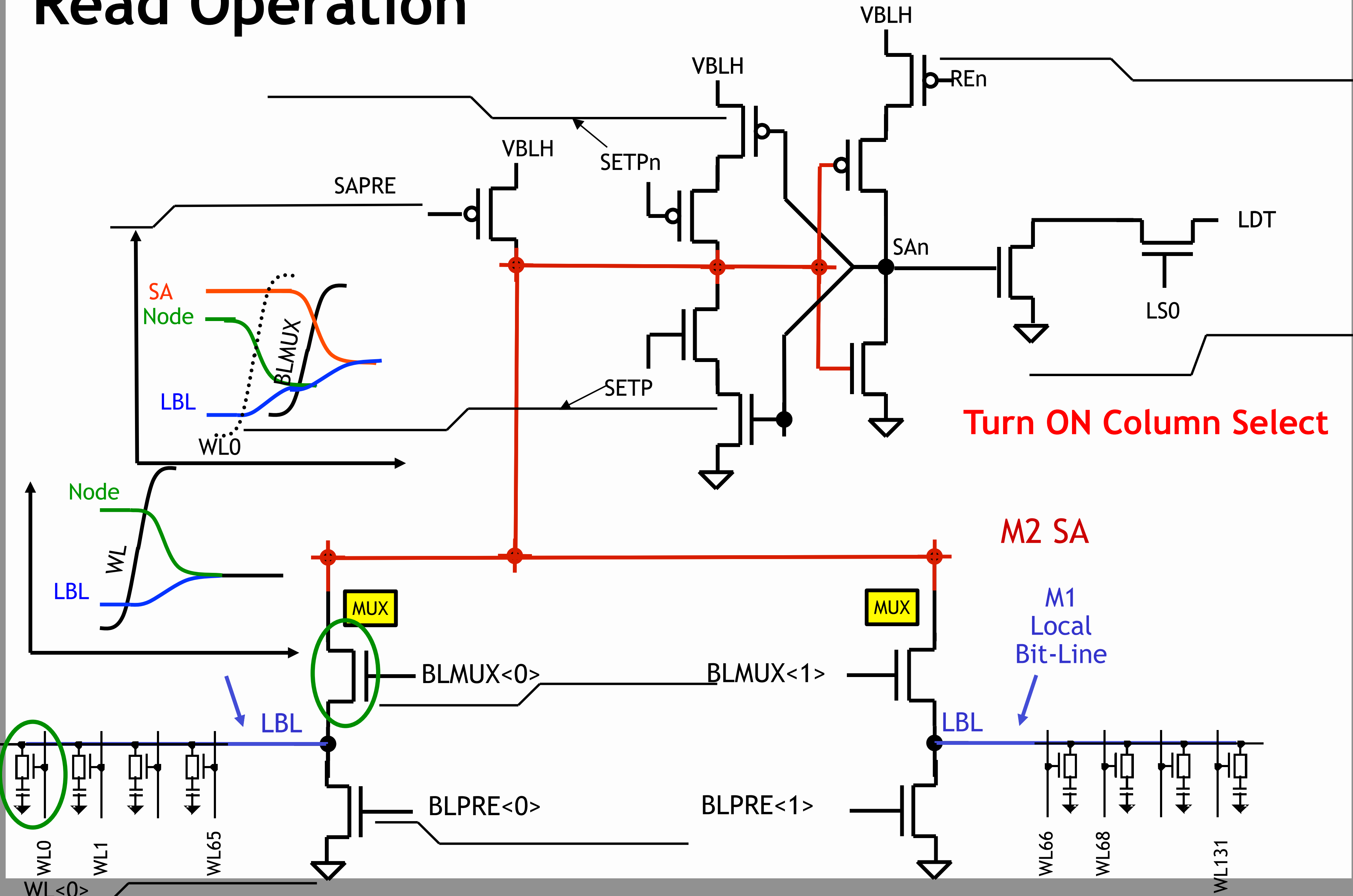
Animation

Read Operation



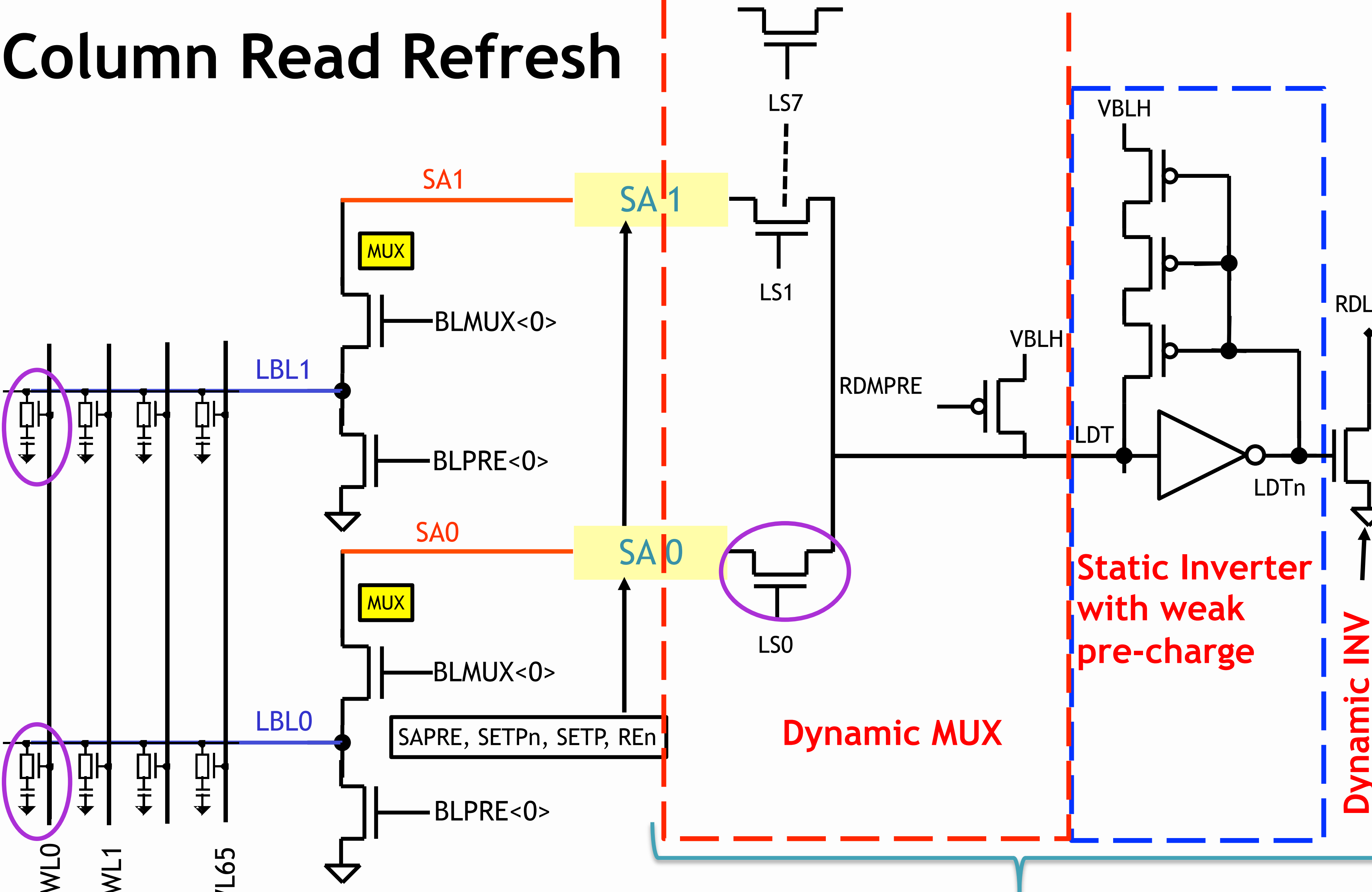
Animation

Read Operation



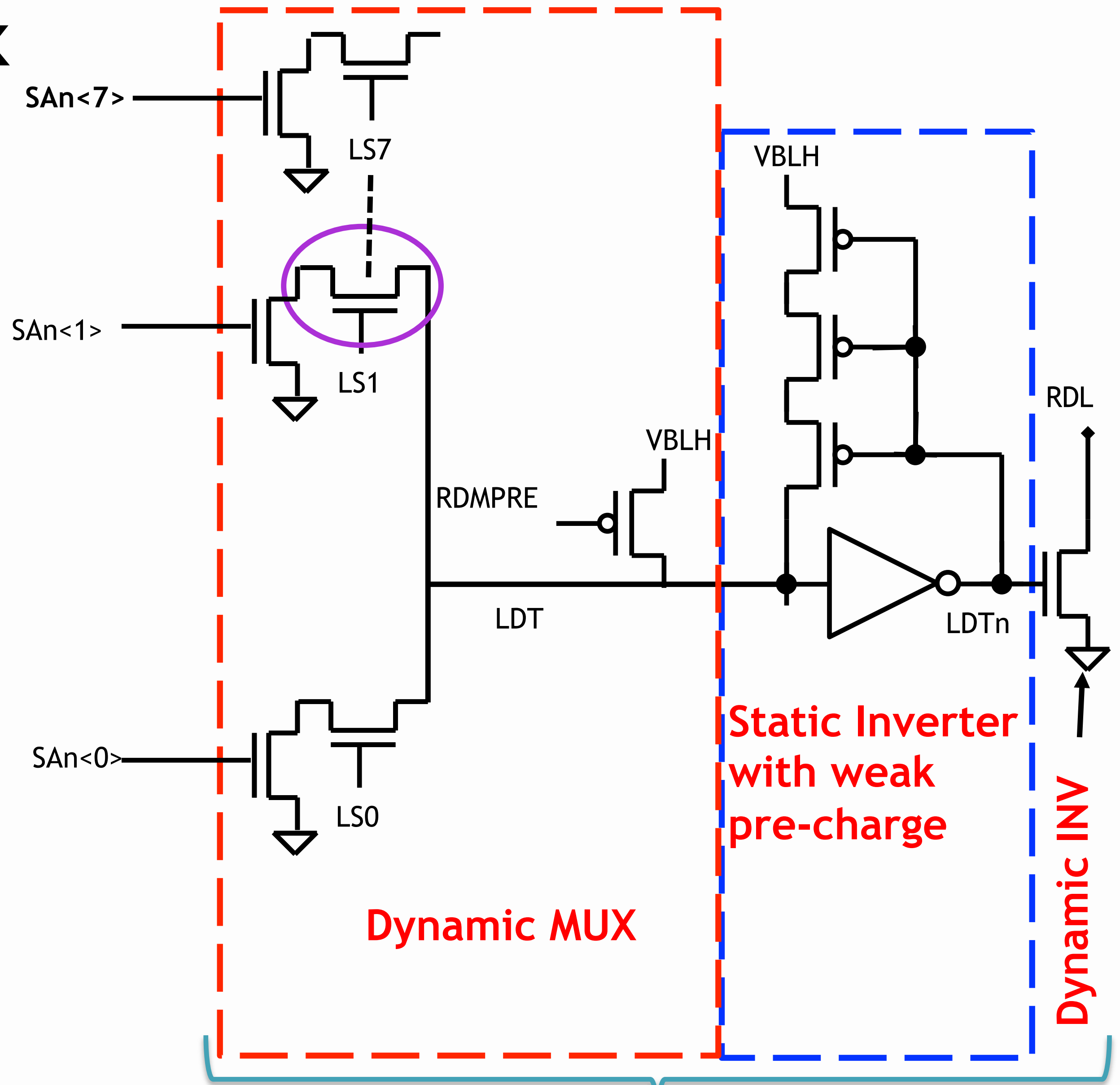
Animation

Column Read Refresh

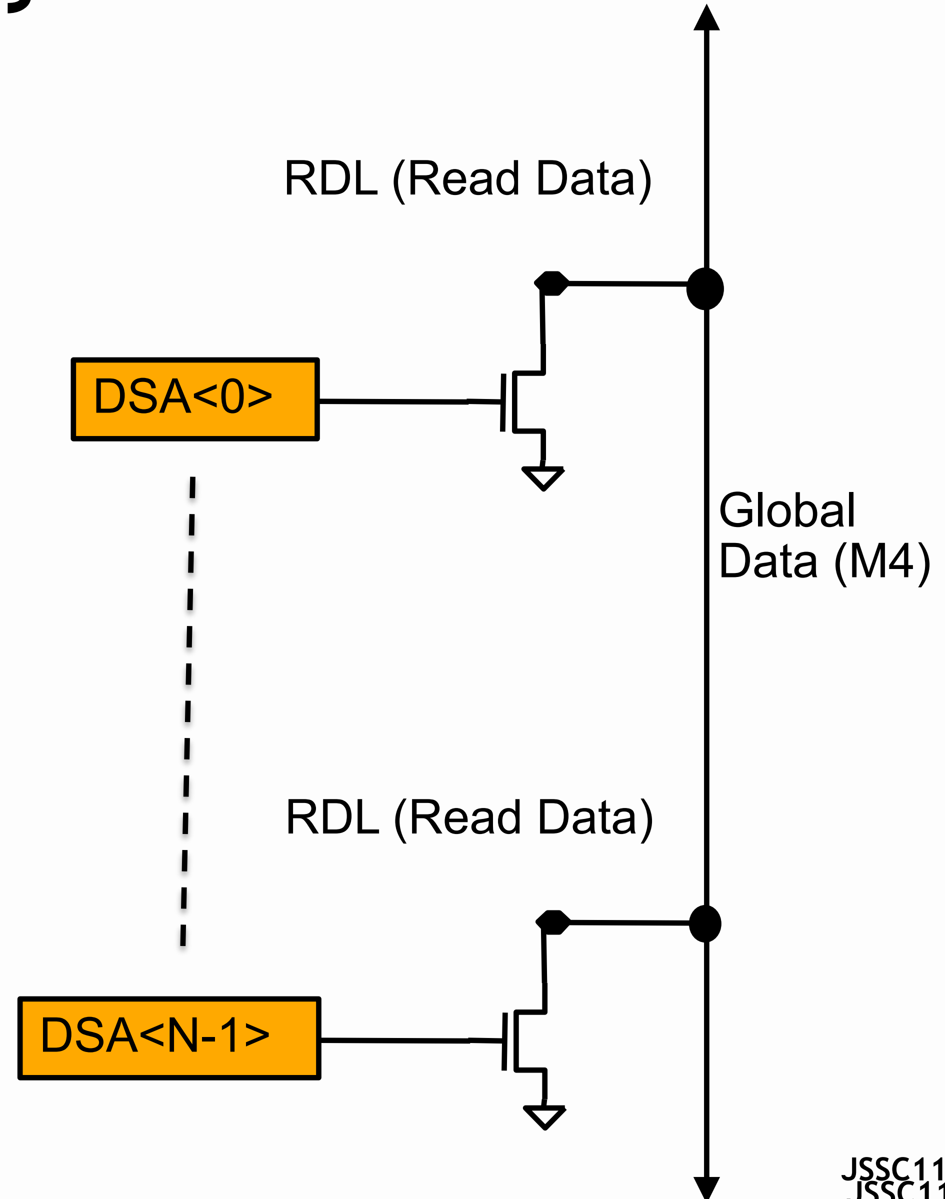


Other columns automatically get refreshed

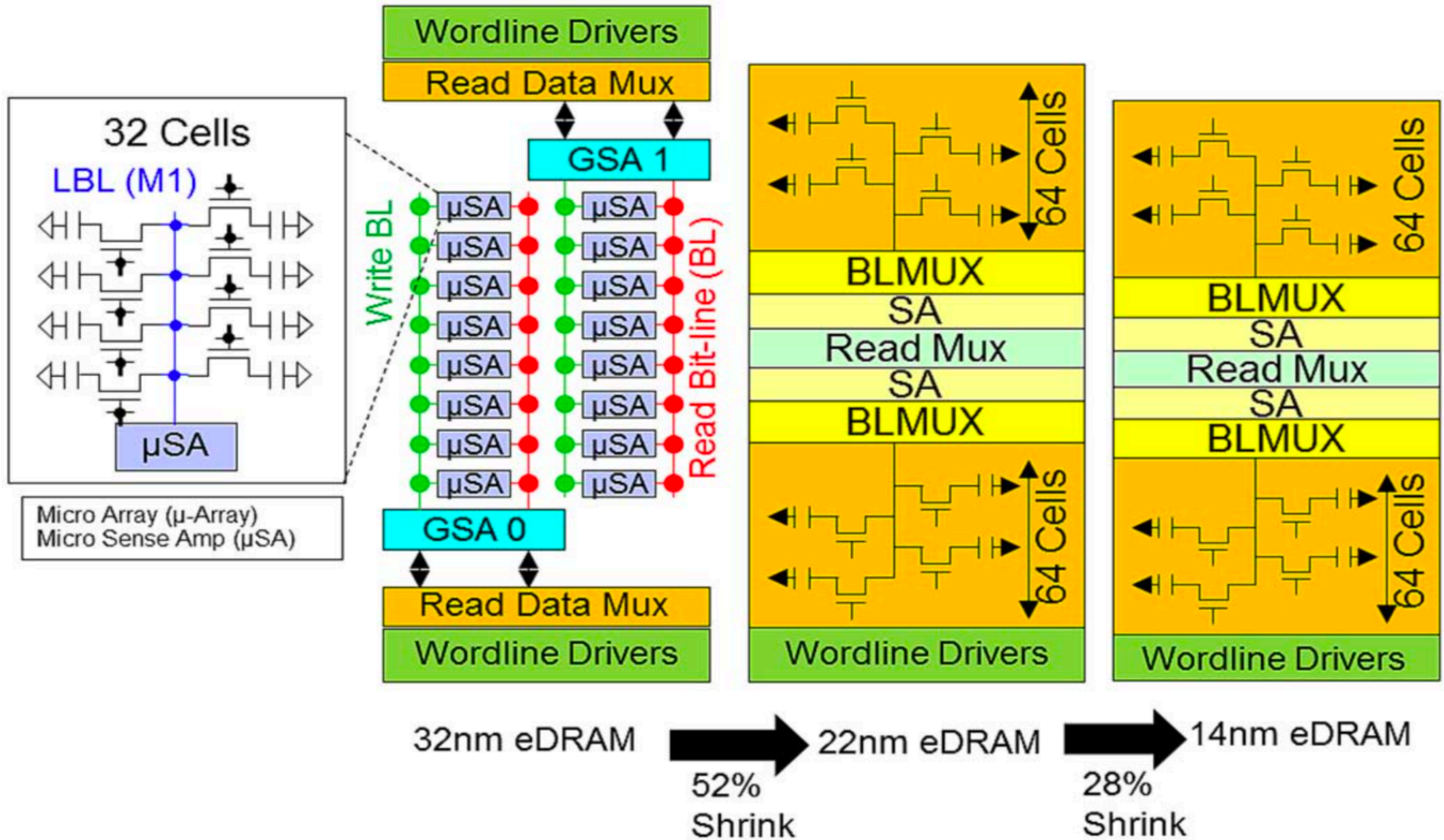
Read Data Mux



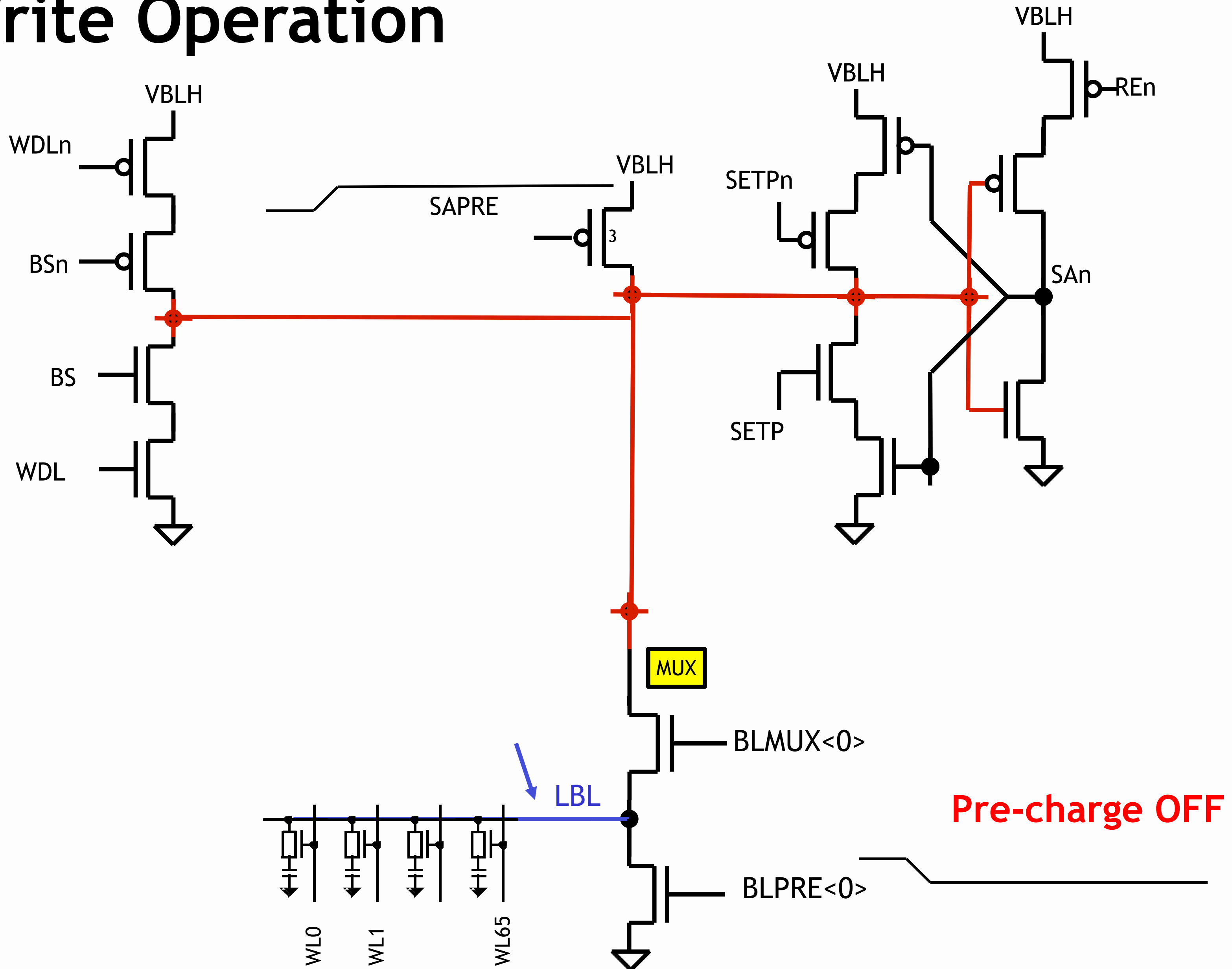
Combining RDM's- Dynamic NOR Gate



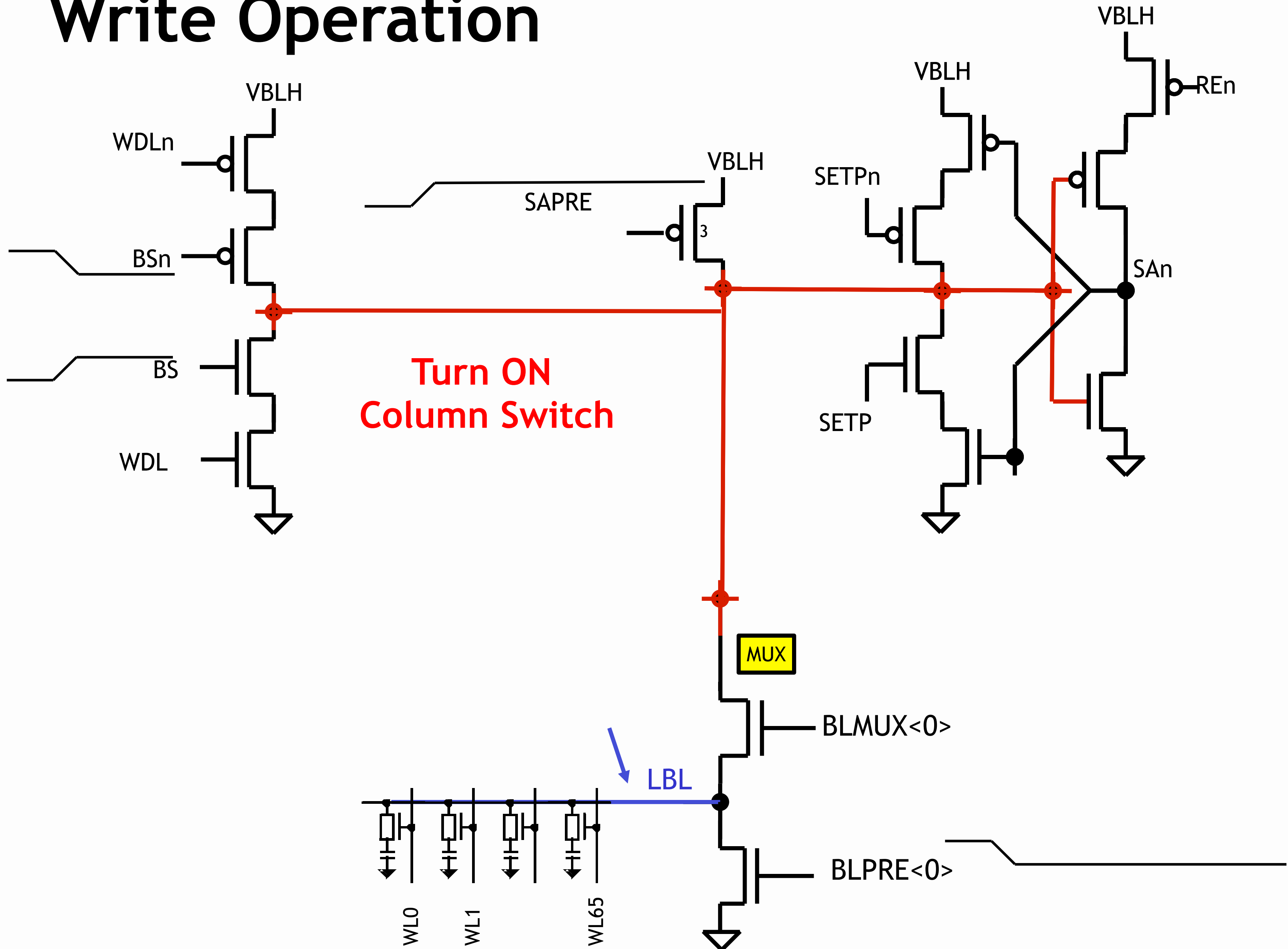
Area Savings and Comparison with 3T uSA



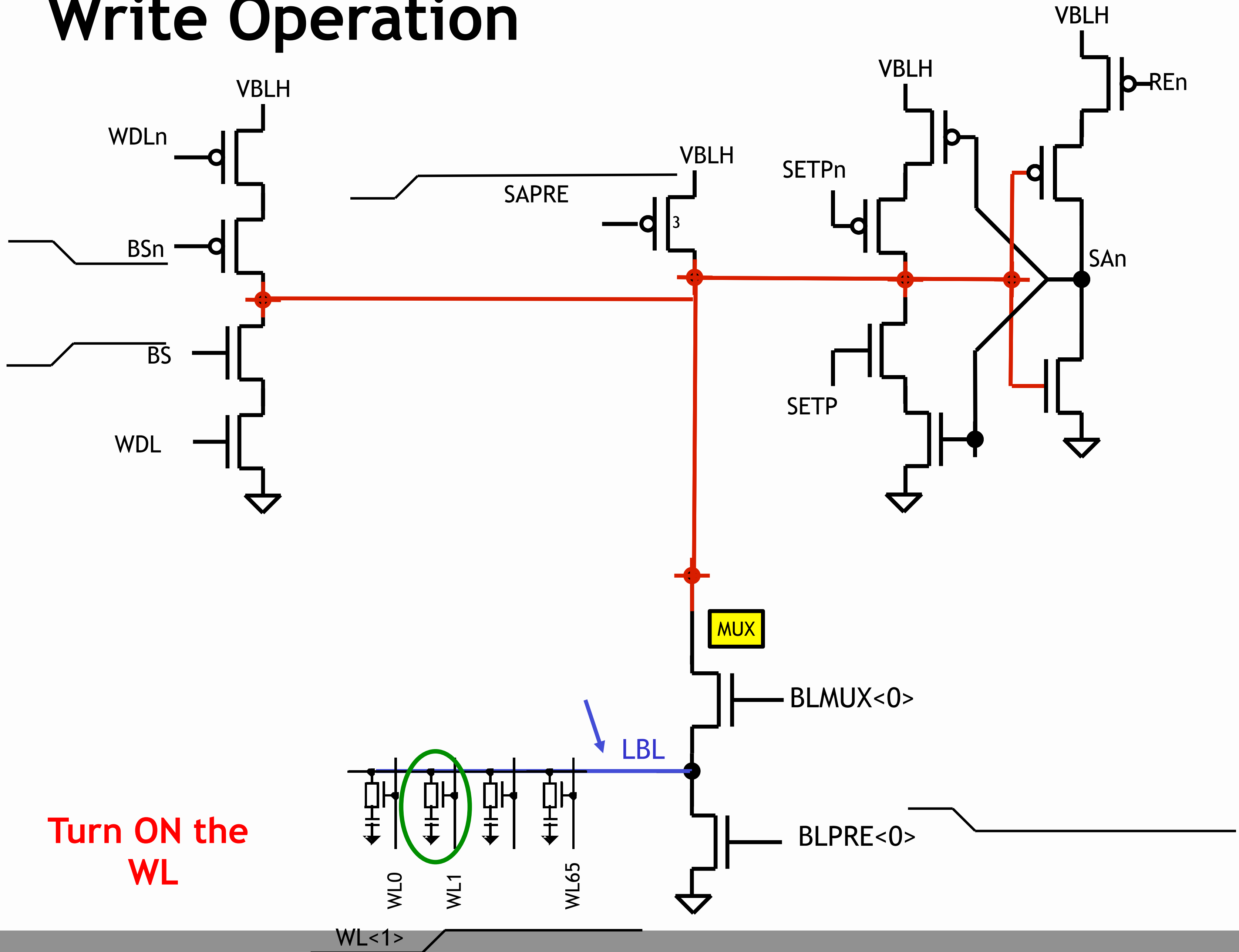
Write Operation



Write Operation



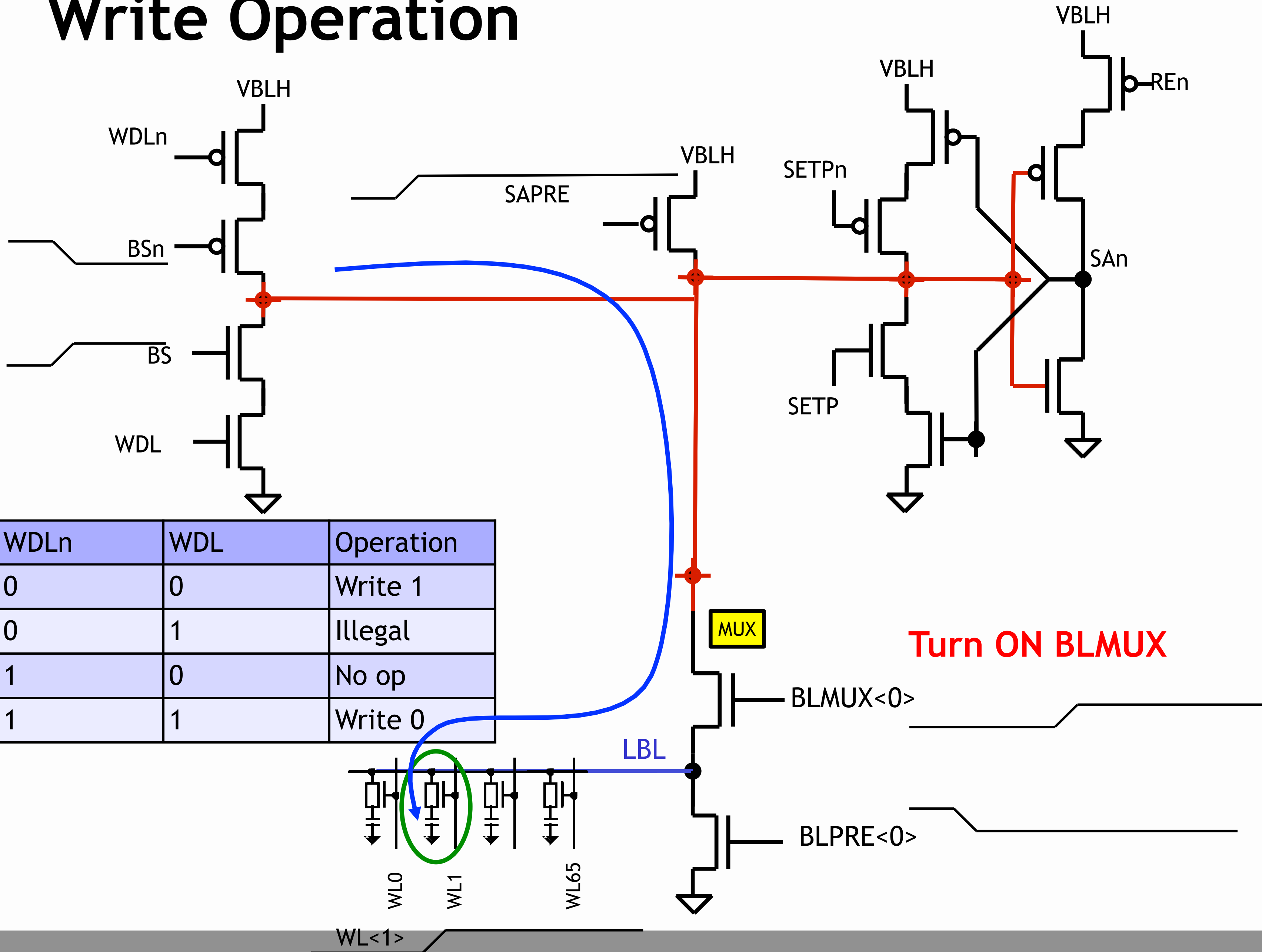
Write Operation



Turn ON the WL

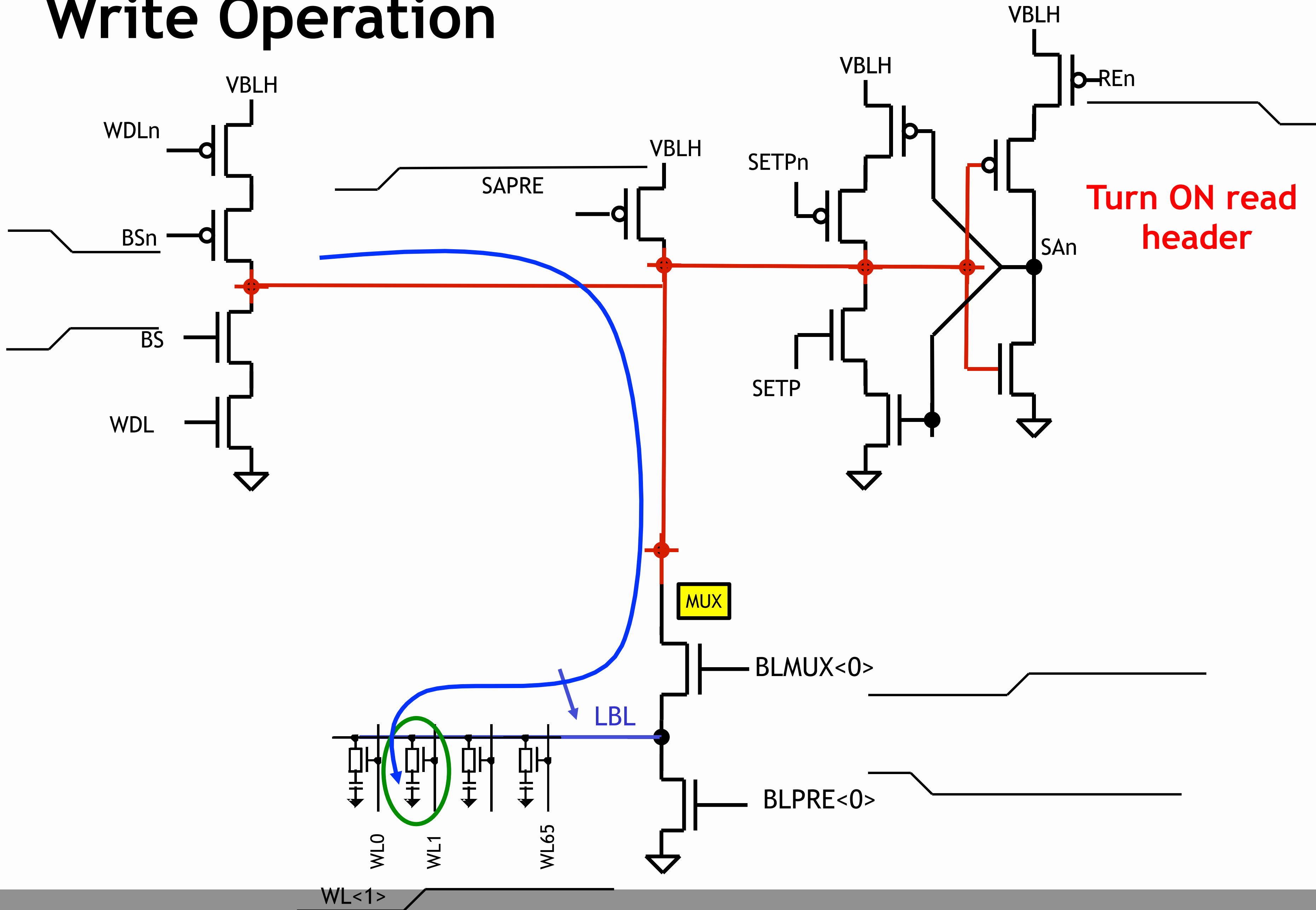
Animation

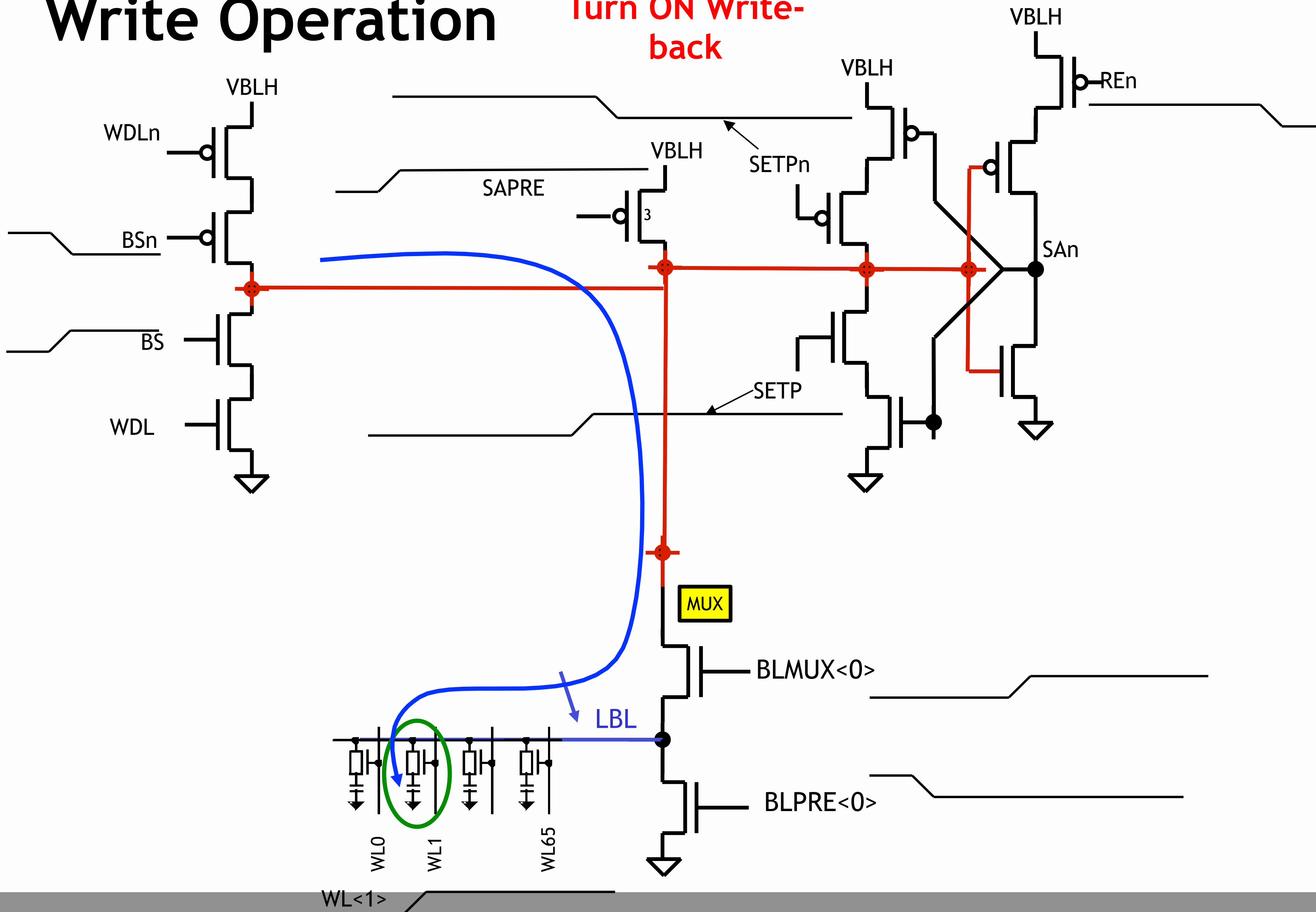
Write Operation



WDLn	WDL	Operation
0	0	Write 1
0	1	Illegal
1	0	No op
1	1	Write 0

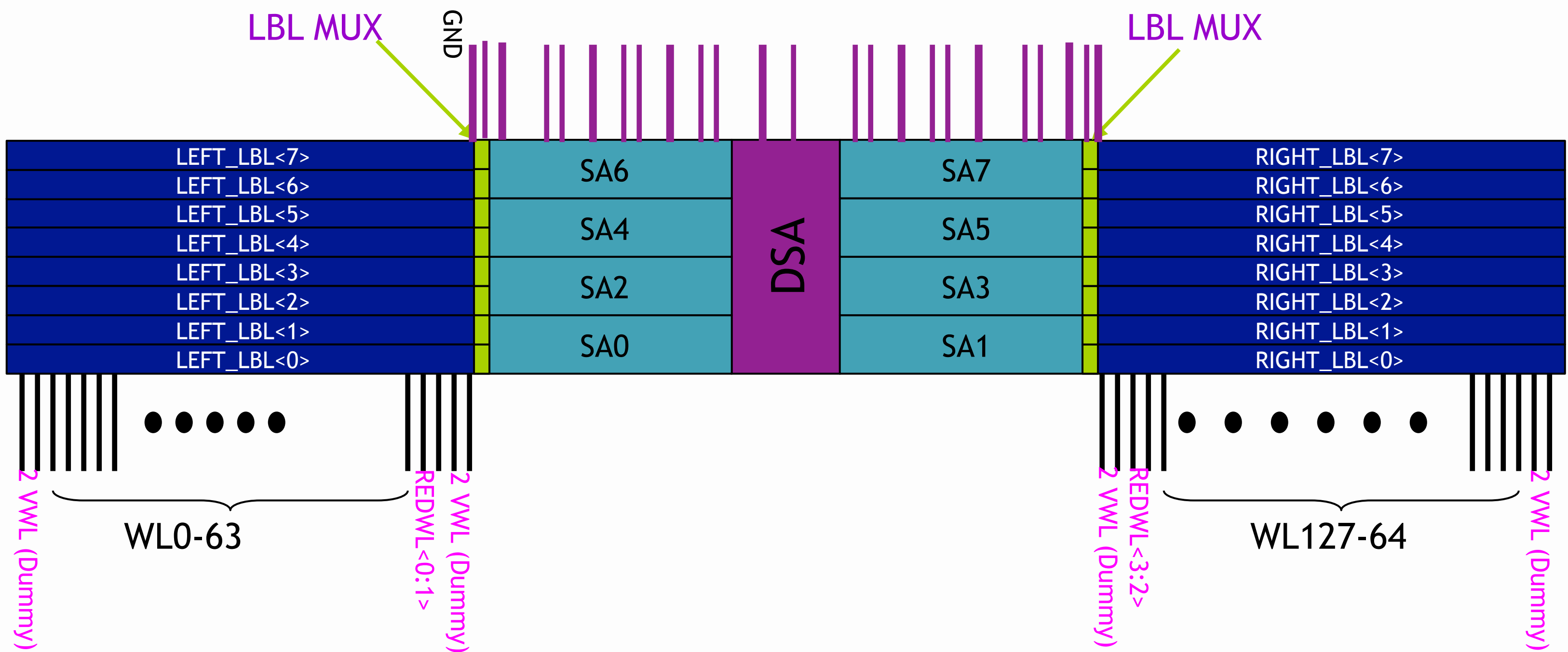
Write Operation





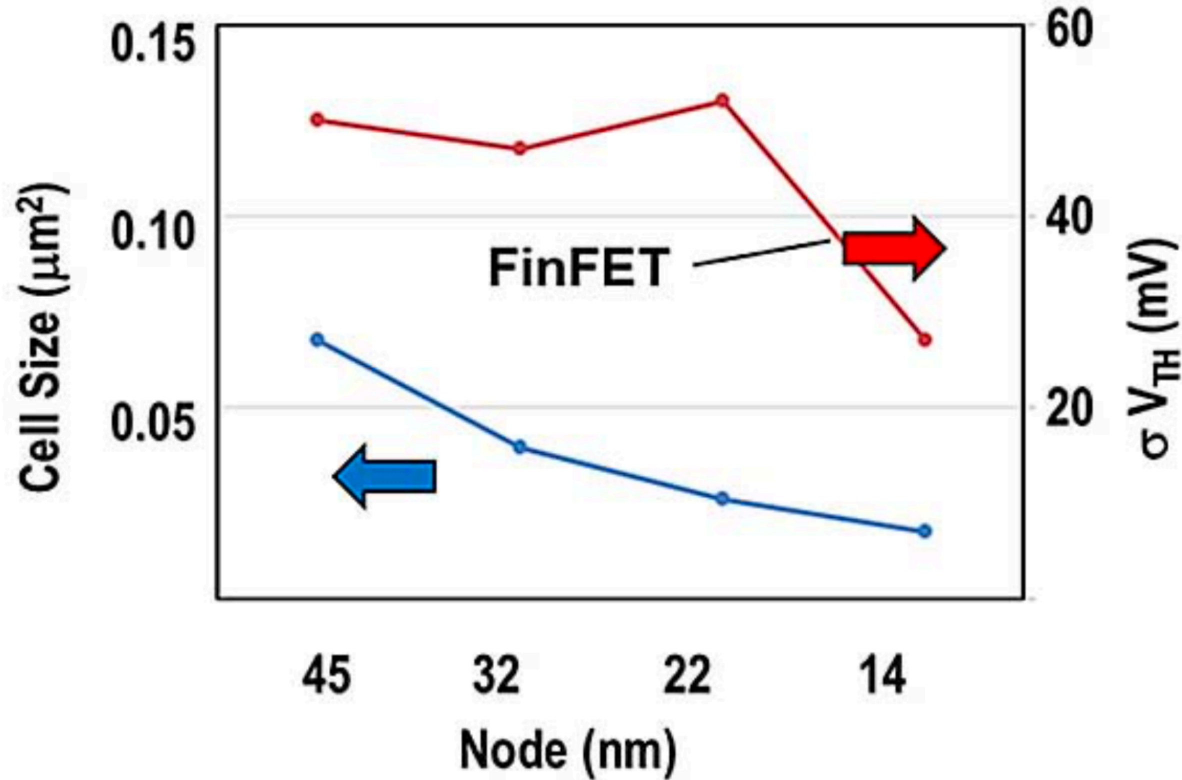
Write Operation
Turn ON Write-back
VBLH
REn
VBLH
VBLH
WDLn
SETPn
VBLH
SAPRE
3
BSn
SAn
BS
SETP
WDL
MUX
BLMUX<0>
LBL
BLPRE<0>
WL0
WL1
WL65
WL<1>

One Data Line Organization



- Single bit can be read out/ written into by selecting one of 128 rows and one of 8 columns
- The components are sized and arranged to make the layout nice and rectangular
- Repeat this structure as many as there are Data-lines

14nm FinFET Advantage

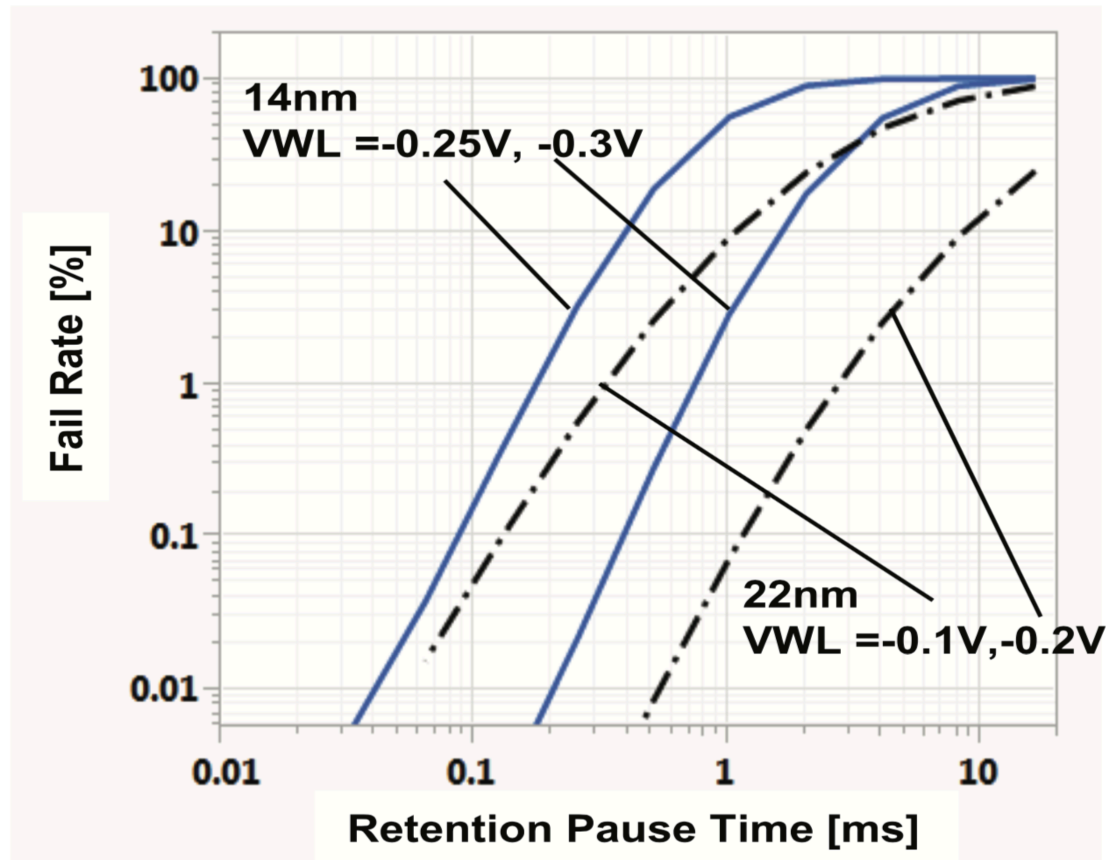


14nm Access Device is 2.5X stronger than the 22nm planar device due to

- 50% more effective width
- 42% shorter channel length
- Lower target Vth

Lower VT variation due to undoped channel

Lower Vth Variation Effect on Retention



- Write a 1 into all the cells
- Read the cells after a pause time
- Ideally (with no local variations) there should be an step jump in the #fail
    - With variations, steeper the slope lesser the variations

Conclusion

- Pulling more DRAM cache (L2,L3) inside the processor improves overall performance
- eDRAM design using logic process is a challenge
- Case study is done, covering many of the eDRAM design aspects
- Sense amp has to read a 1 by default to provide performance improvement
  - Achieved in the Gated Feedback Sense Amp

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Wang, G. et al., A 0.127 mm2 High Performance 65nm SOI Based embedded DRAM for on-Processor Applications,” International Electron Devices Meeting, Dec. 2006.

G. Fredeman et al., “A 14 nm 1.1 Mb Embedded DRAM Macro With 1 ns Access,” in IEEE Journal of Solid-State Circuits, vol. 51, no. 1, pp. 230-239, Jan. 2016. doi: 10.1109/JSSC.2015.2456873