# DRAM Operation Details (Case Study)

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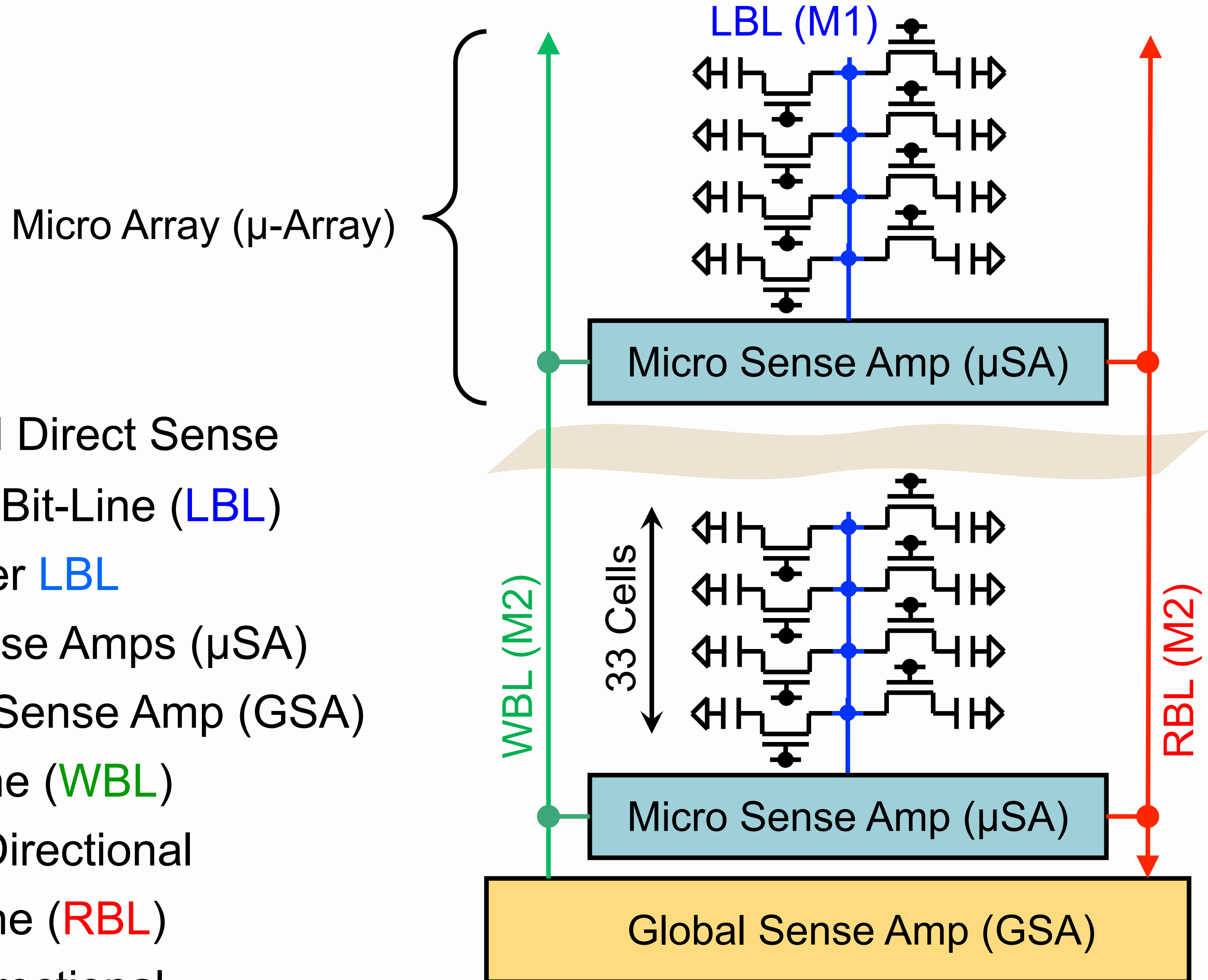
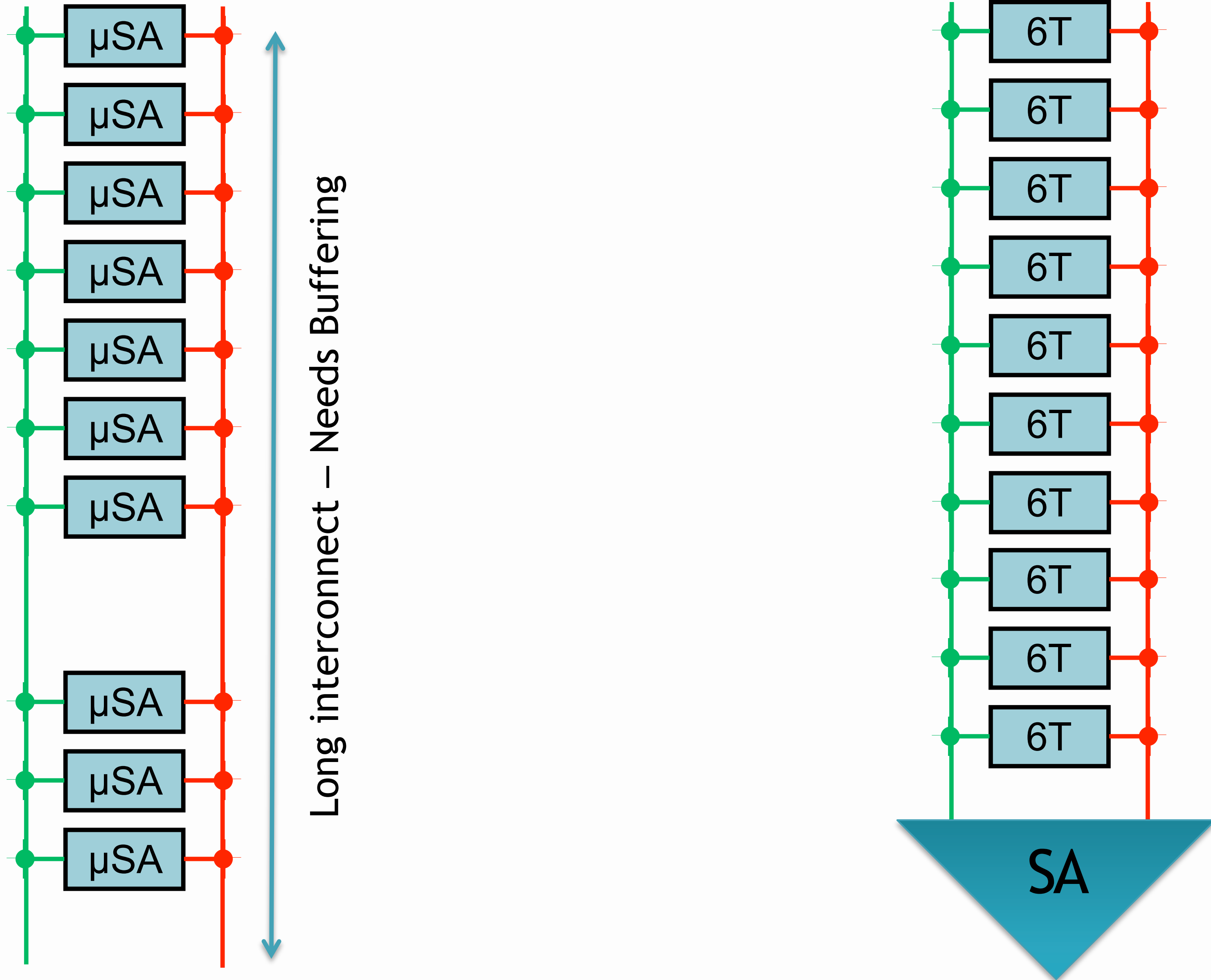
**A 500 MHz Random Cycle, 1.5 ns Latency, SOI Embedded DRAM Macro Featuring a Three-Transistor Micro Sense Amplifier (John Barth/IBM)**

# Micro Sense Architecture

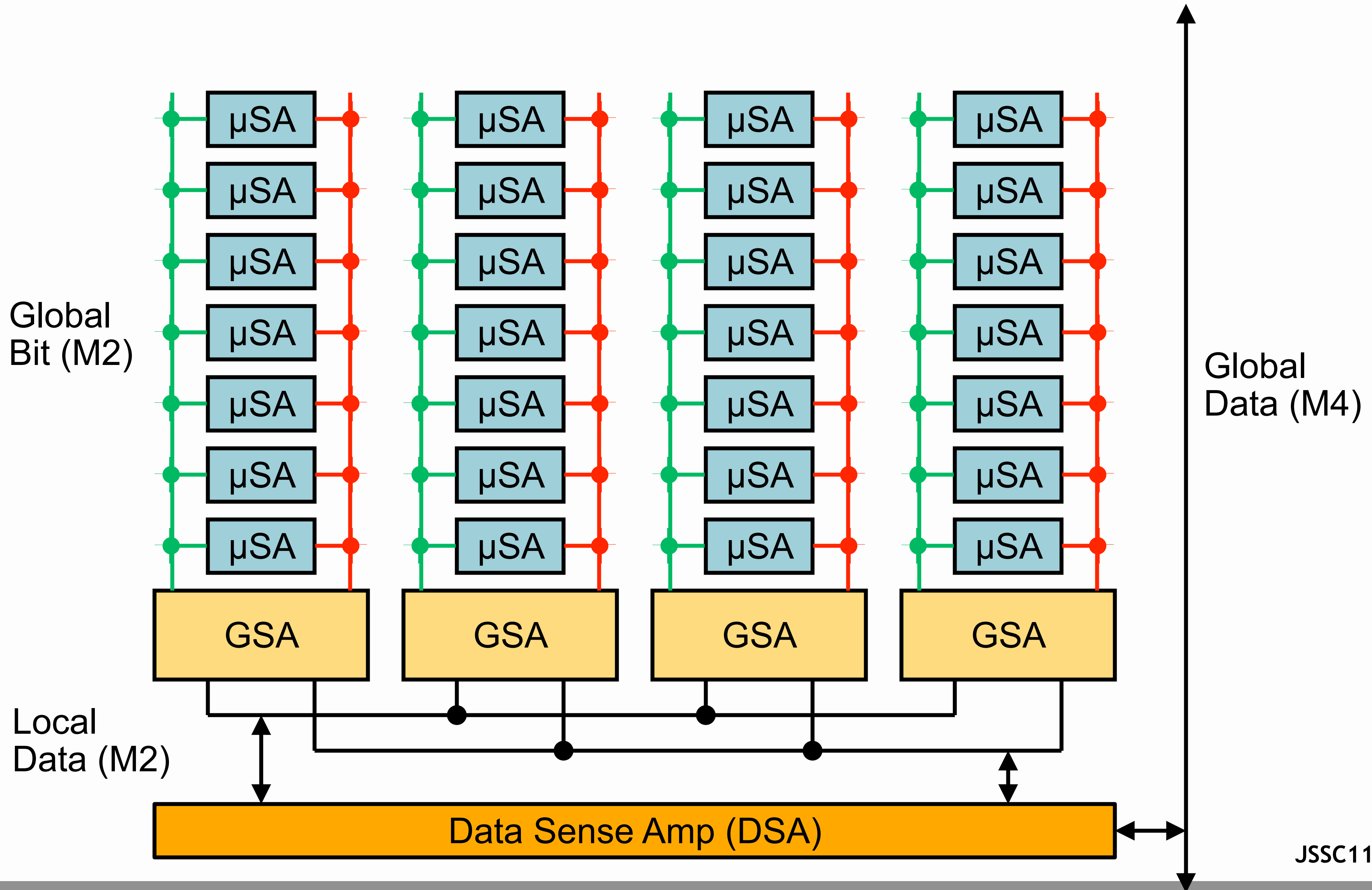



- Hierarchical Direct Sense
- Short Local Bit-Line (LBL)
  - 33 Cells per LBL
- 8 Micro Sense Amps (μSA) per Global Sense Amp (GSA)
- Write Bit-Line (WBL) Uni-Directional
- Read Bit-Line (RBL) Bi-Directional

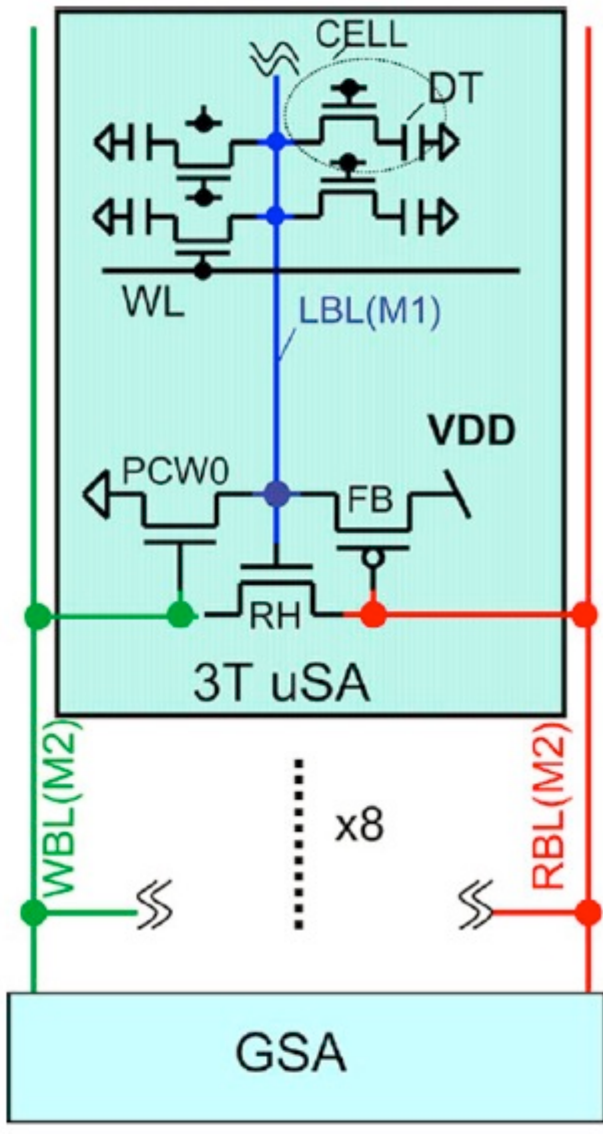
# Sense Hierarchy - Motivation



# Micro Sense Hierarchy - Three levels



# 3T uSA operation




## Pre-charge

WL is low. WBL and RBL both pre-charged to HIGH.
Next GSA drives WBL low. **LBL floats to GND level**

## Read "0"

LBL remains LOW. RBL is HIGH. Sensed as a "0"

## Read "1"

LBL is HIGH. Turns on RH, pulls RBL LOW.
+ feedback as pFET FB turns ON. Sensed as a "1"

## Write "1"

GSA pulls RBL to GND. FB pFET turns ON
Happens while WL rises (direct write)

## Write "0"

WBL is HIGH, PCW0 ON. Clamps LBL to GND
As WL activates.

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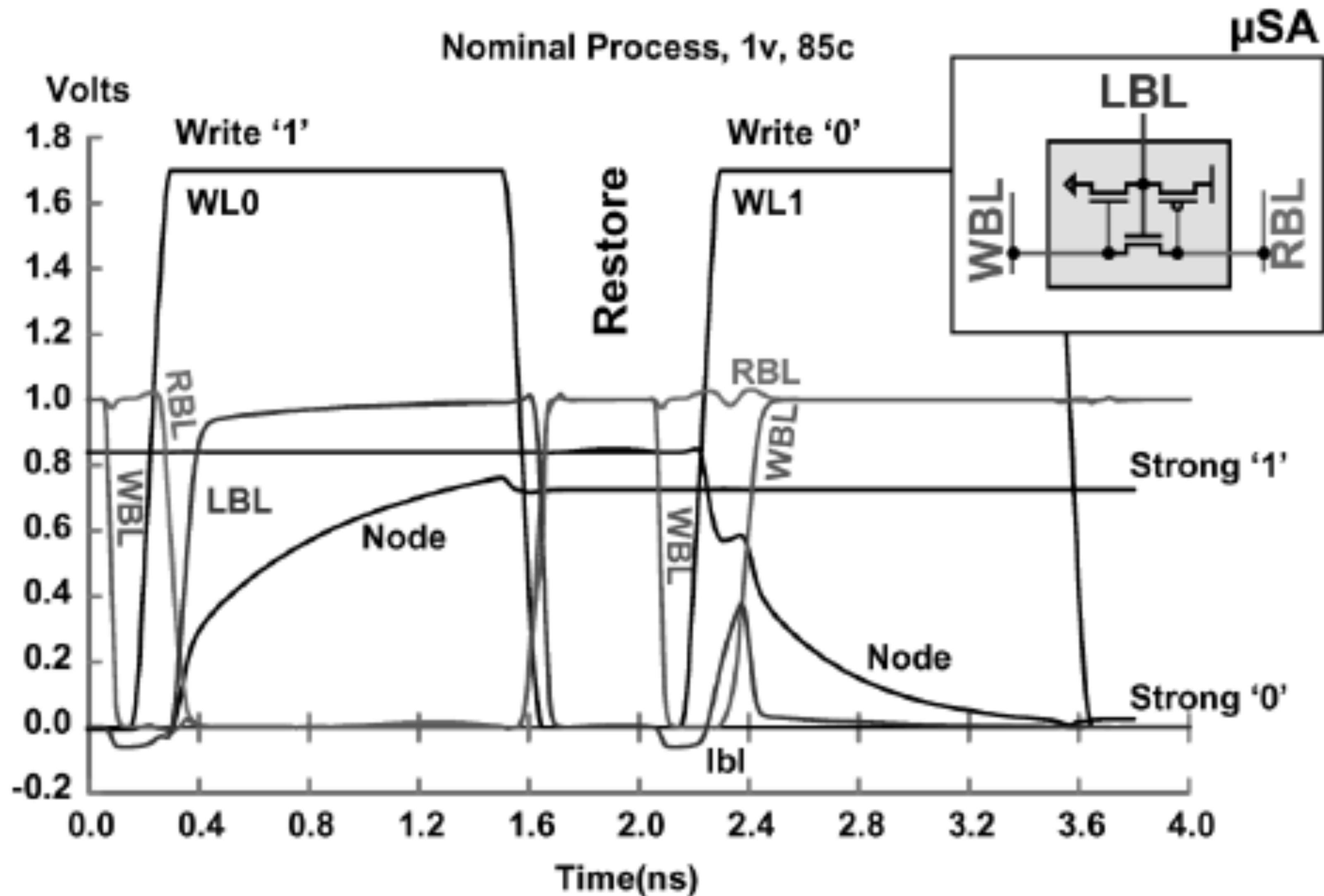
# Simulations - Write

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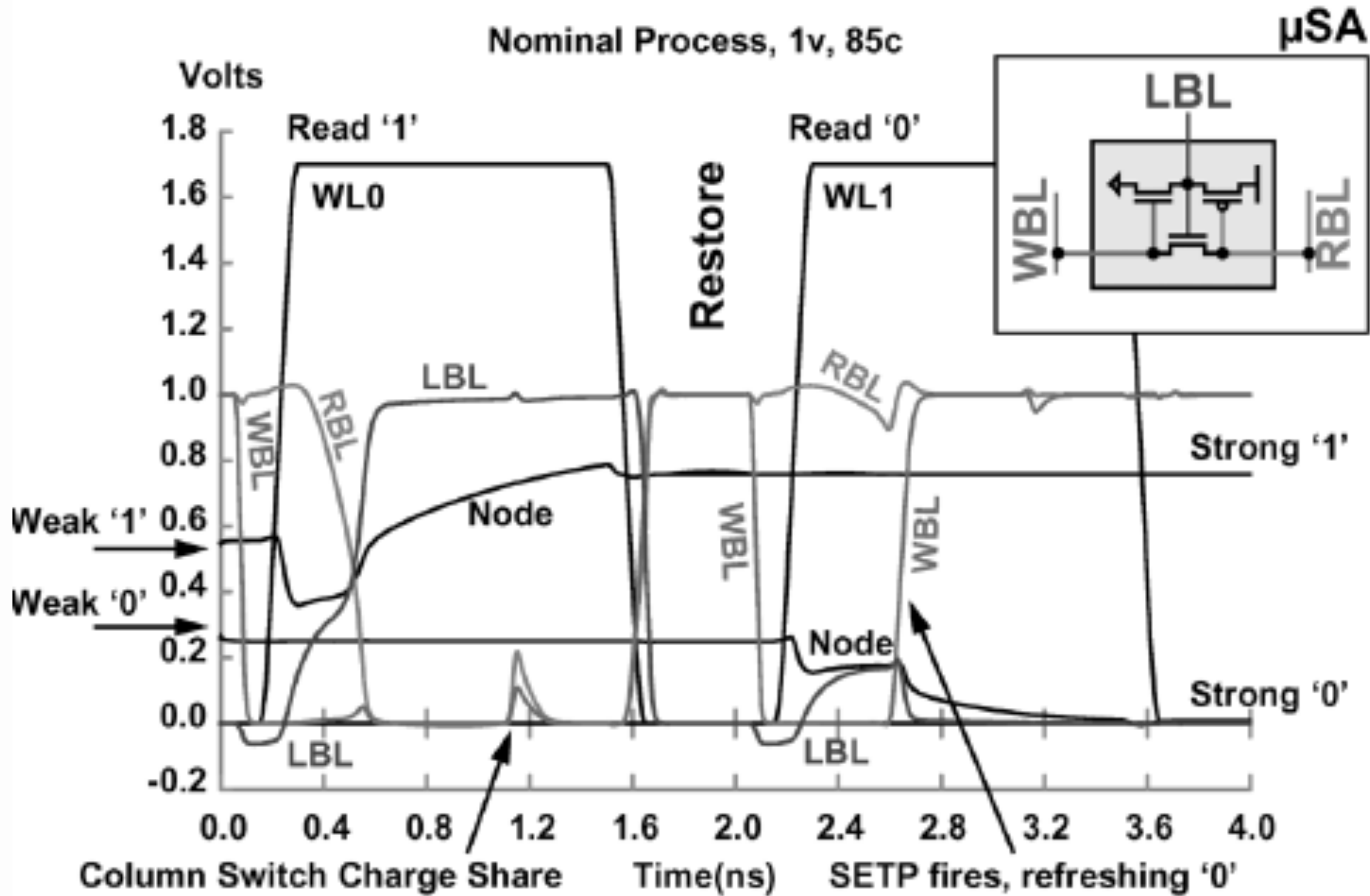
# Simulations - Read




(b)

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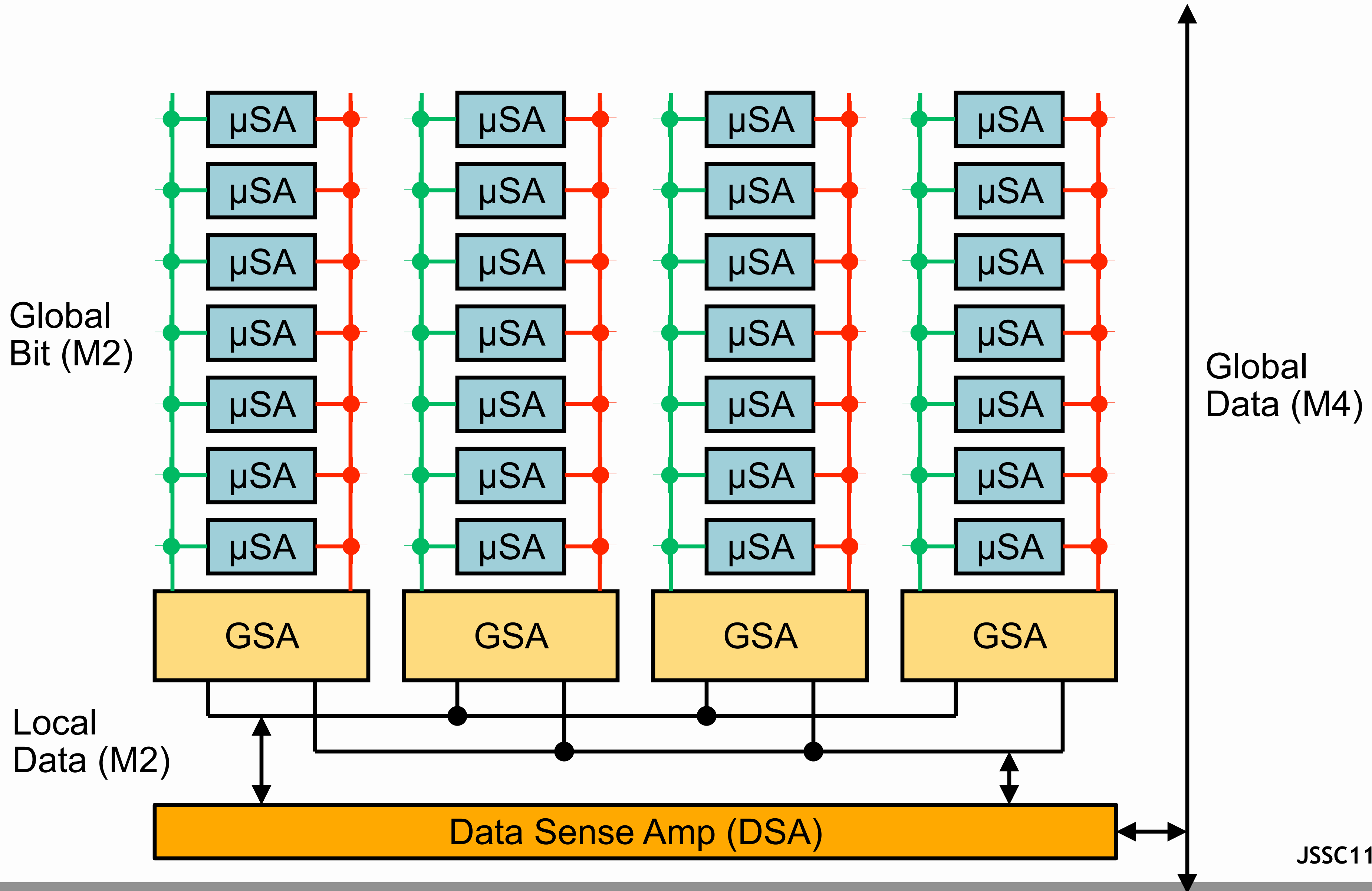
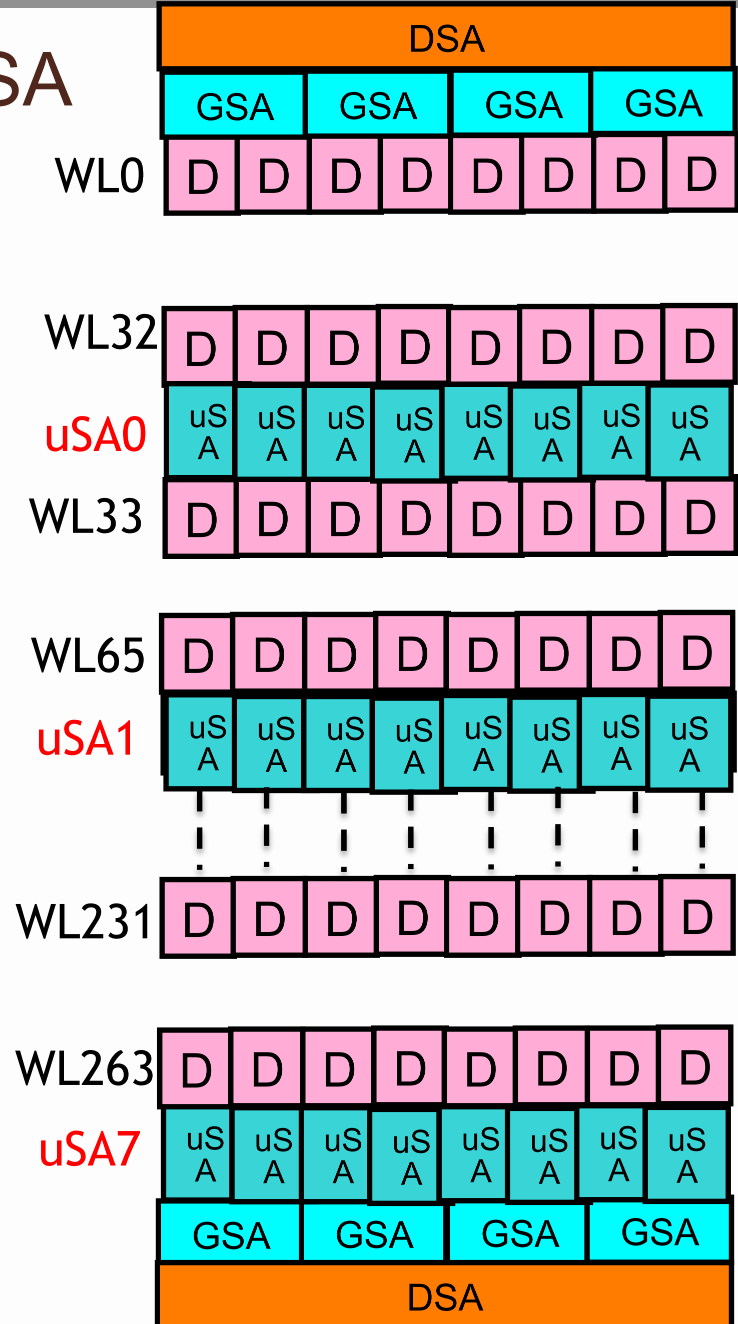


# Layout Floor plan of Array+SA

GSA Should fit into the bitcell width or n*bitcell width

Thus, distributed GSA on two sides of bitcell array



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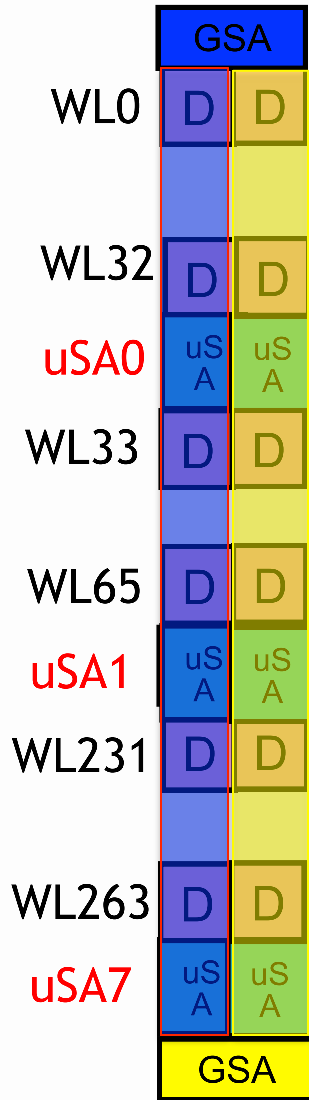
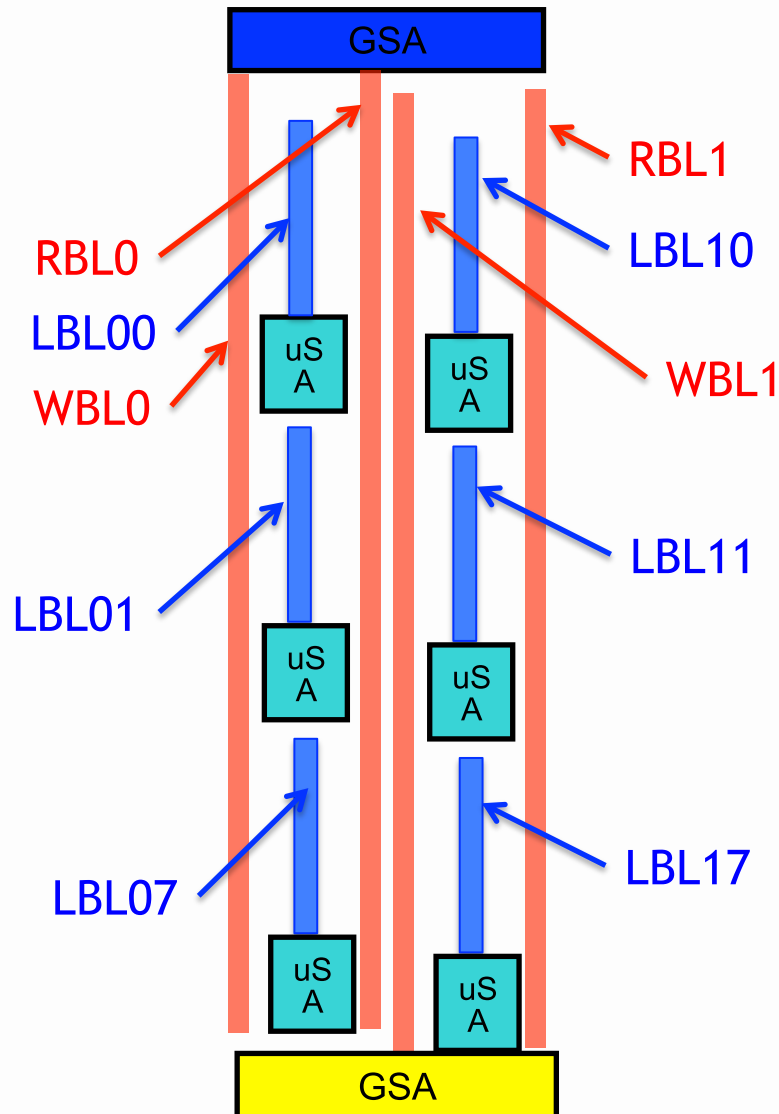
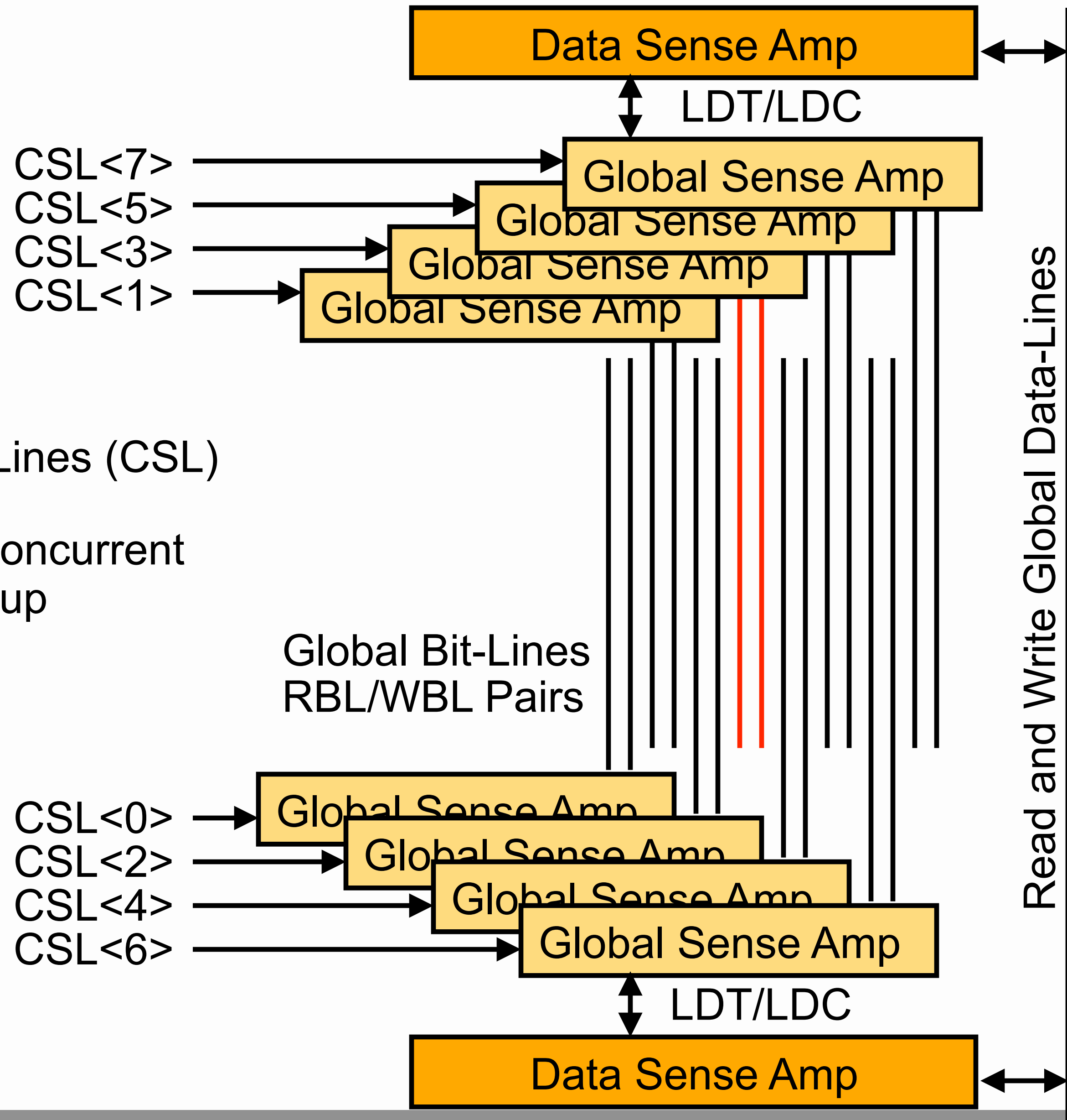


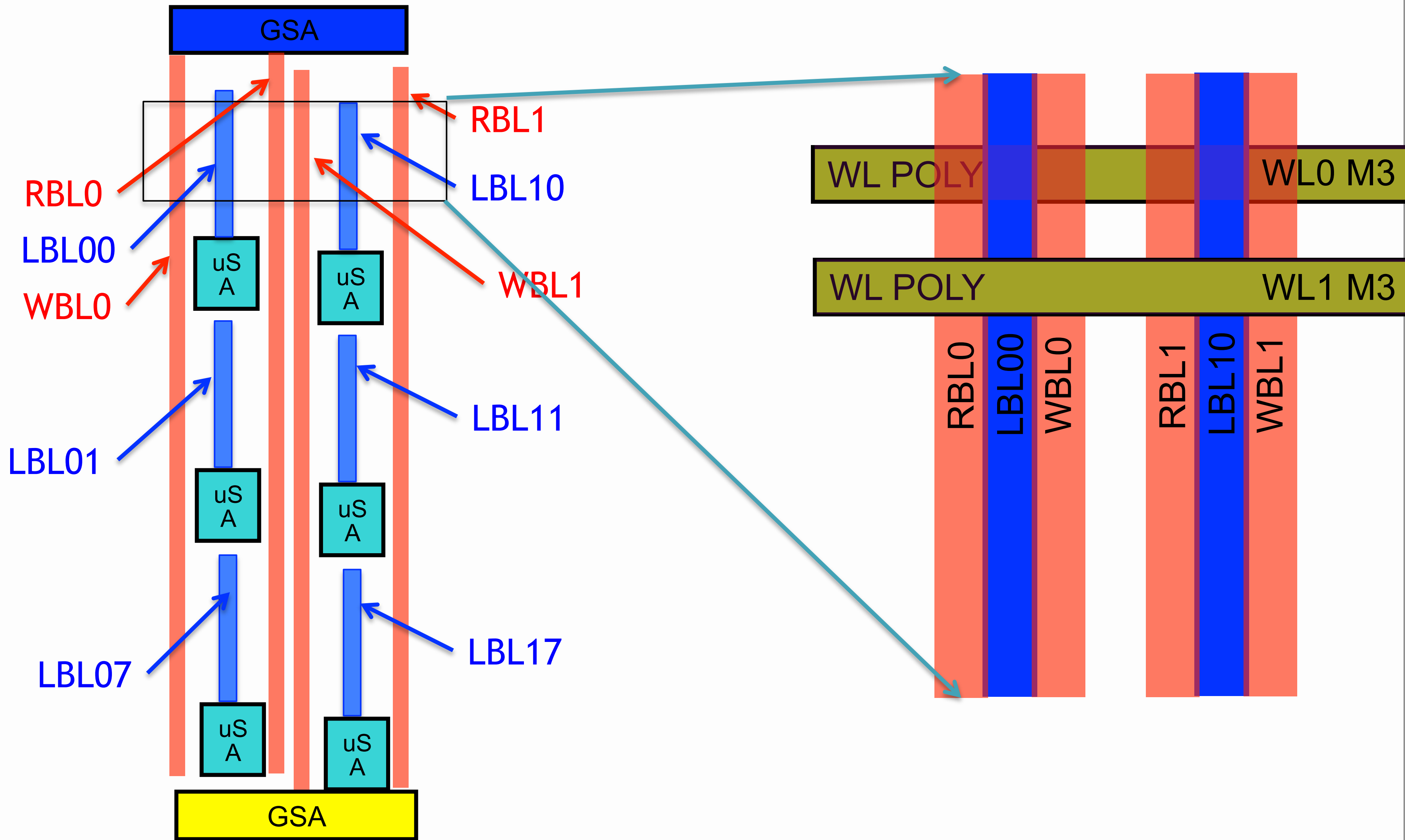



# Column Interleave

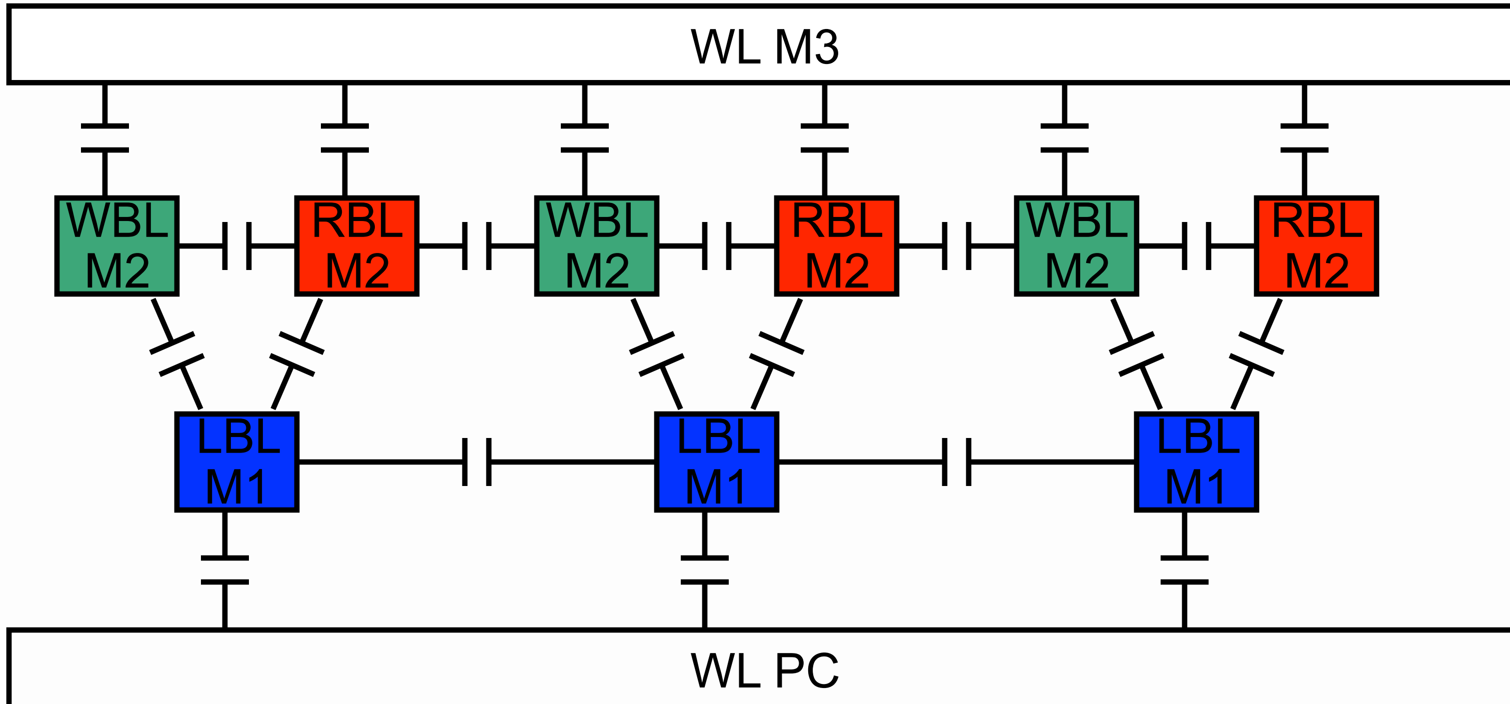



- 1 of 8 Column Select Lines (CSL)
- Fire Early for Write
- Fire Late to Support Concurrent Cache Directory Lookup

# LAYOUT of array

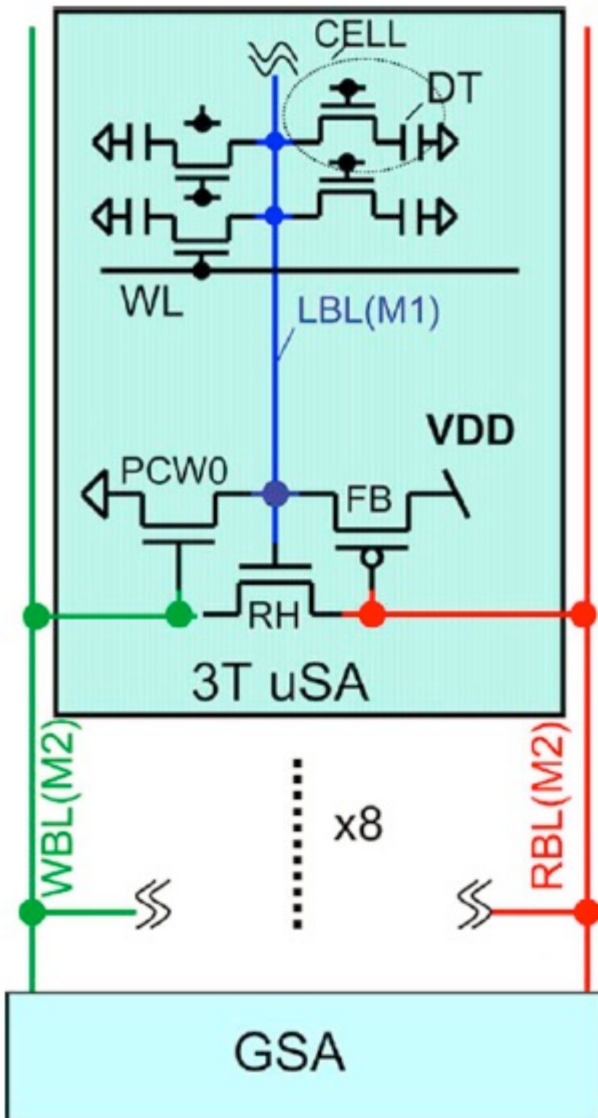


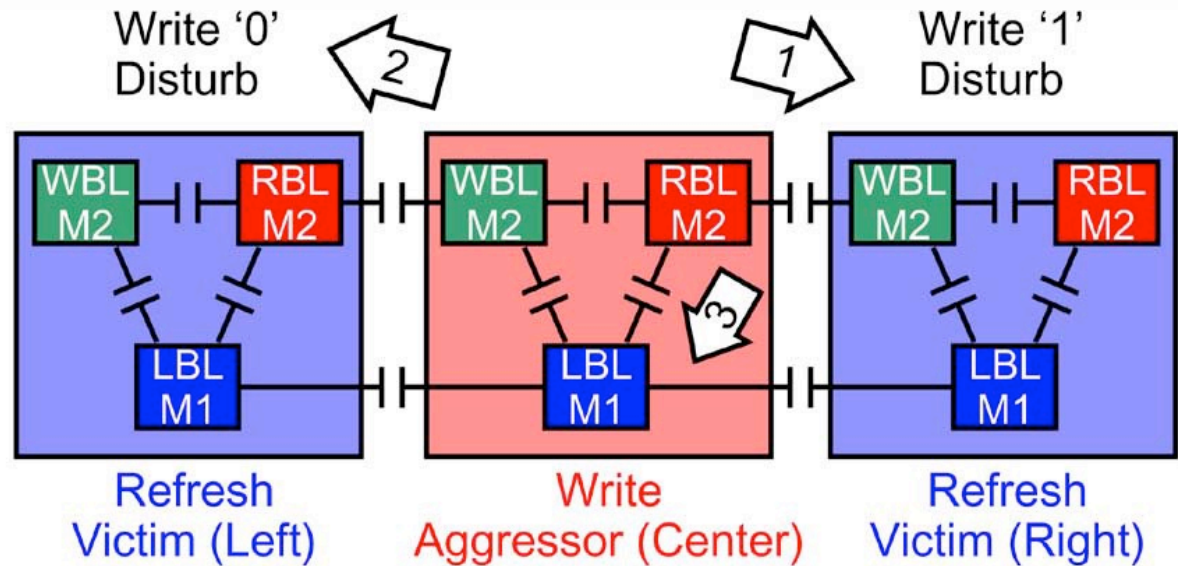
# Micro Sense Local Bit-line Cross Section




Single Ended Sense – Twist not effective
Line to Line Coupling must be managed

# Micro Sense Coupling Mechanisms




1. Write '1' Couples WBL below Ground Increasing RH leakage during Refresh '0'
2. Write '0' Couples RBL above VDD Delaying Feedback during Refresh '1'
3. Read '1' Couples Half-Selected LBL Below GND Increasing Array Device Sub-VT Leakage

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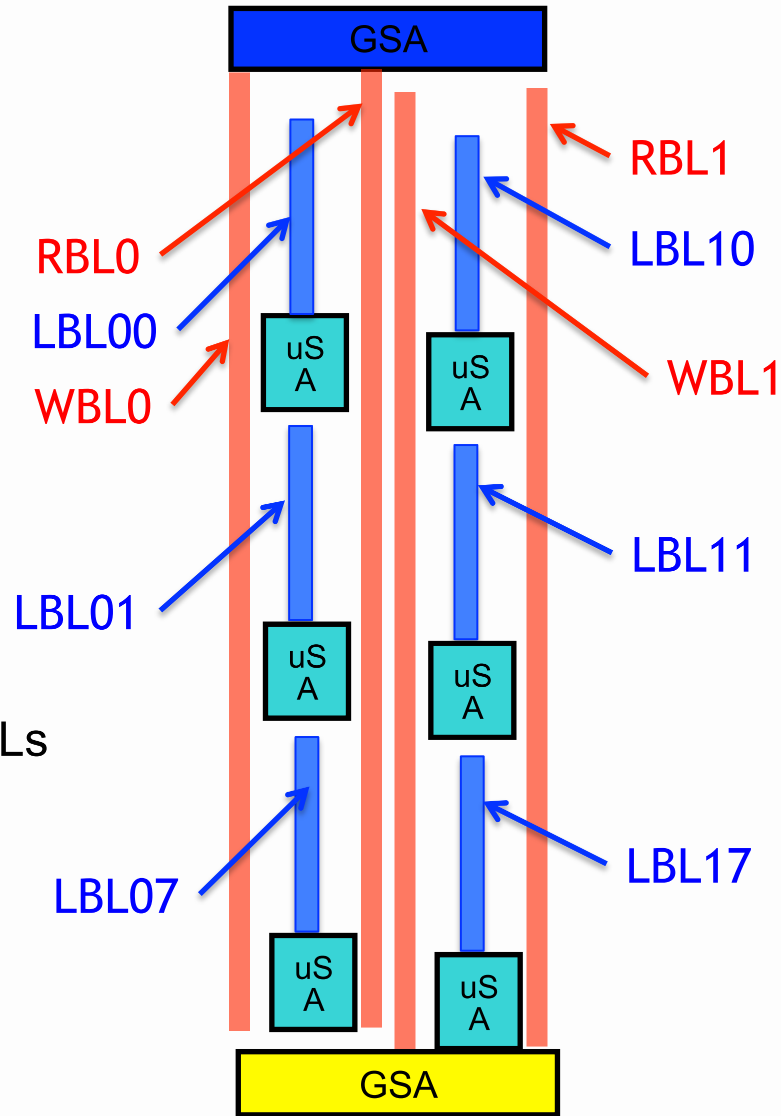
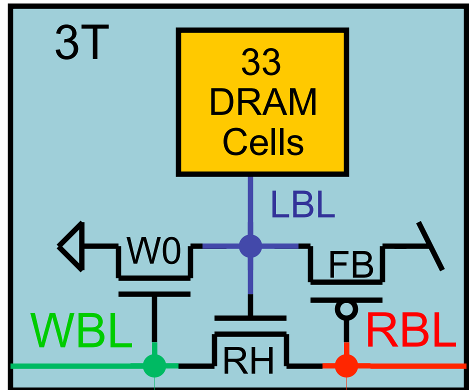
# Half Selected LBL




- Accessing one of WL0-32
- Cell connected is on LBL00
- LBL01-07 – Half Selected LBLs

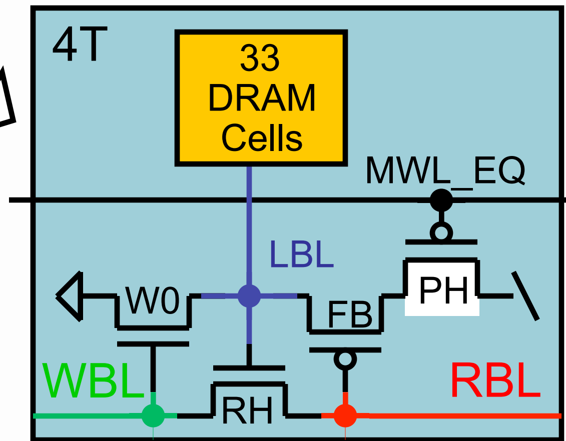
# Micro Sense Evolution

1. Write Zero (W0)
2. Read Head (RH)
3. Feed-Back (FB)



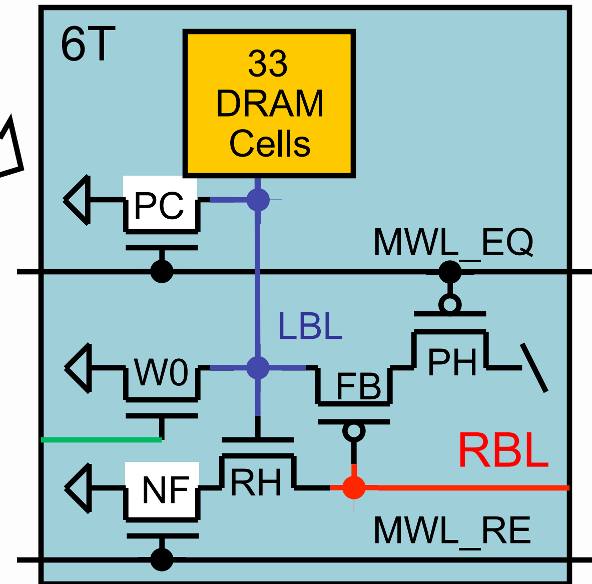

Barth, ISSCC'07

4. PFET Header (PH)
   - LBL Power Gate
   - LBL Leakage




Klim, VLSI'07

5. Pre-Charge (PC)
   - WBL Power (Write '0' Only)
6. NFET Footer (NF)
   - RBL Leakage
   - Decompose Pre-Charge and Read Enable (MWL_RE)

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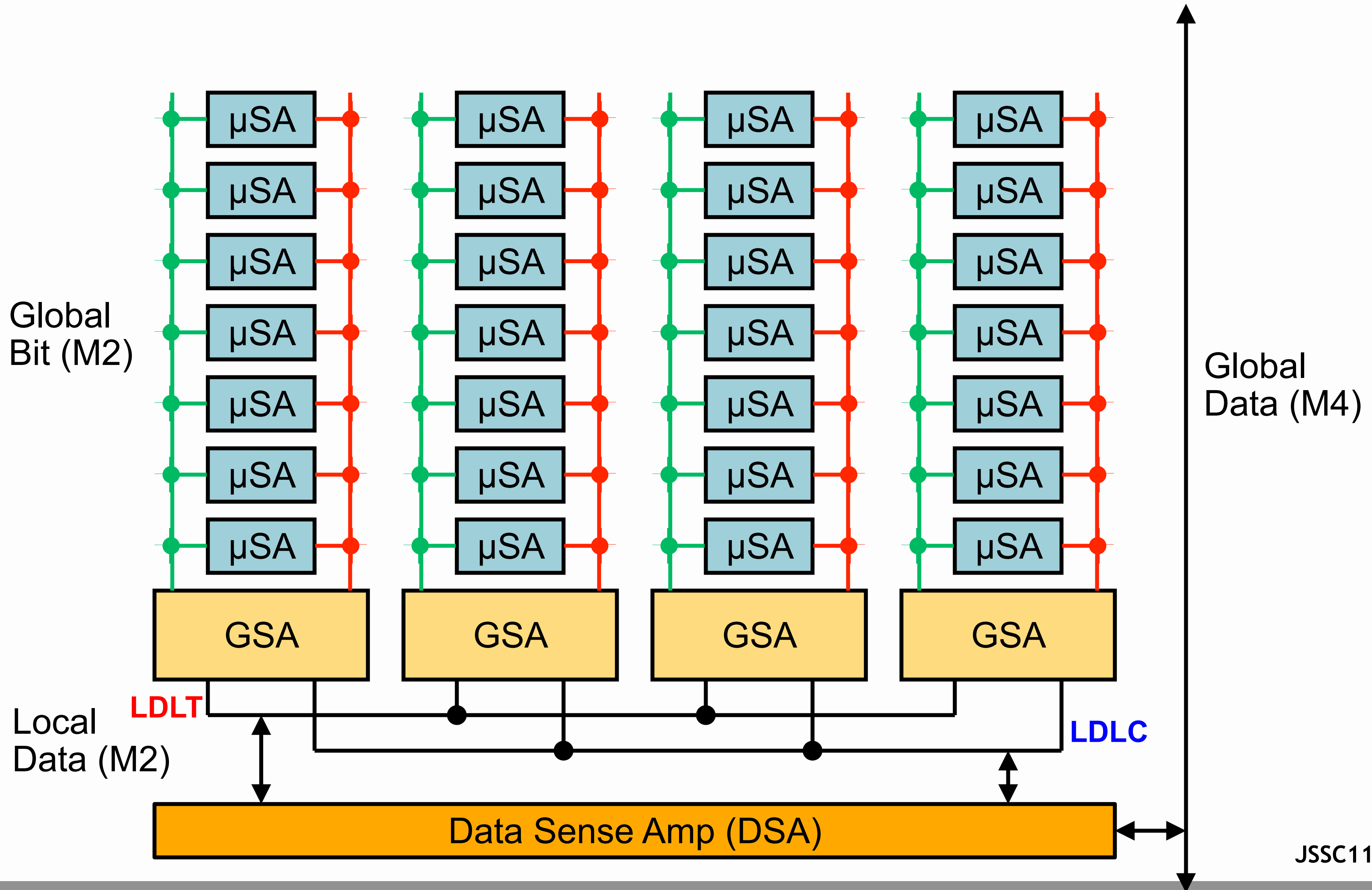
Power Reduction

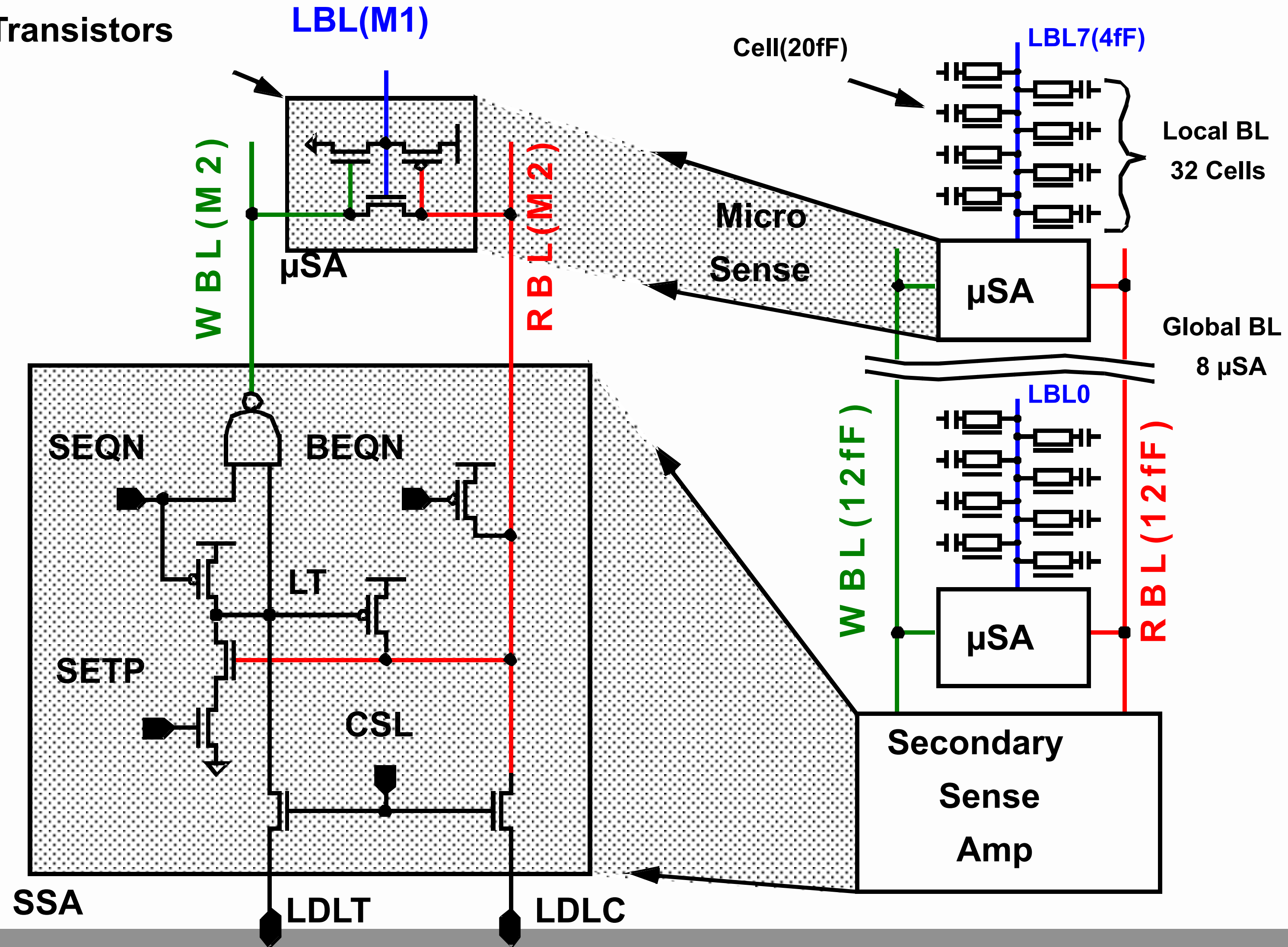
Power Reduction
Traded for Transistor Count

Increased Transistor Count

# Micro Sense Hierarchy - Three levels



# Micro Sense Architecture (μSA)

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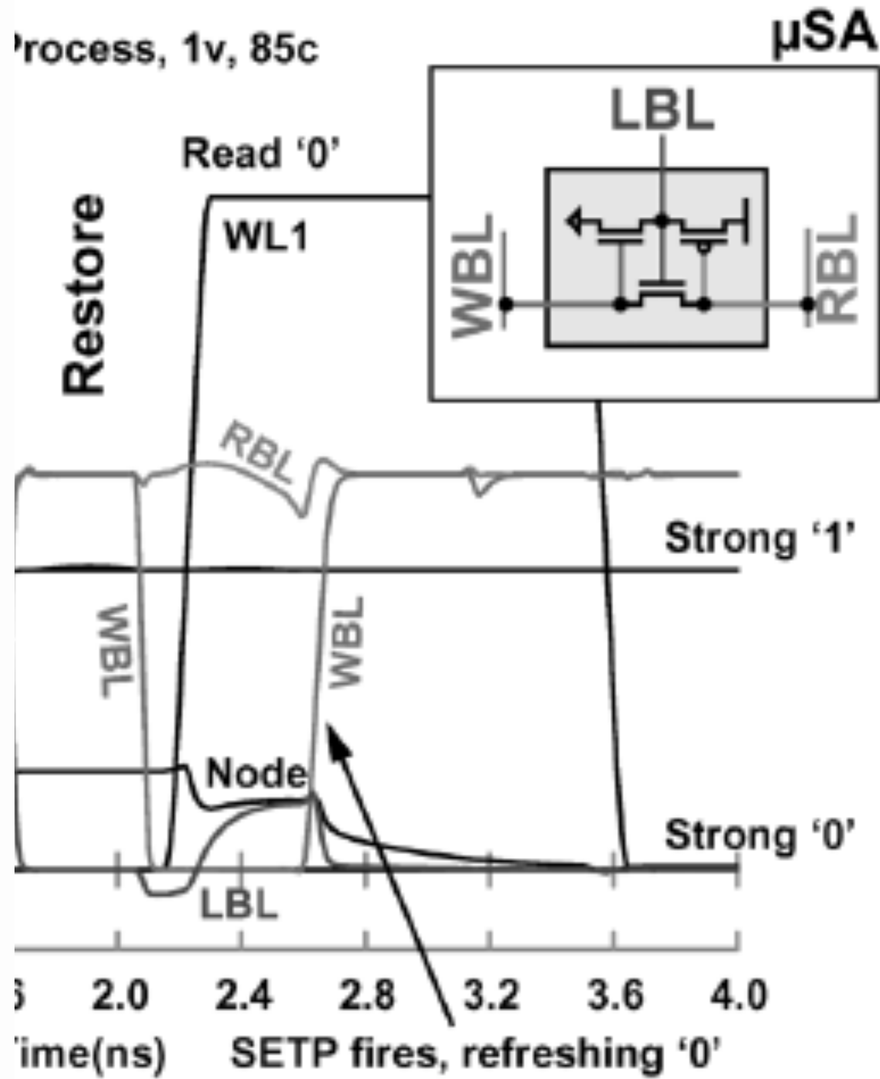
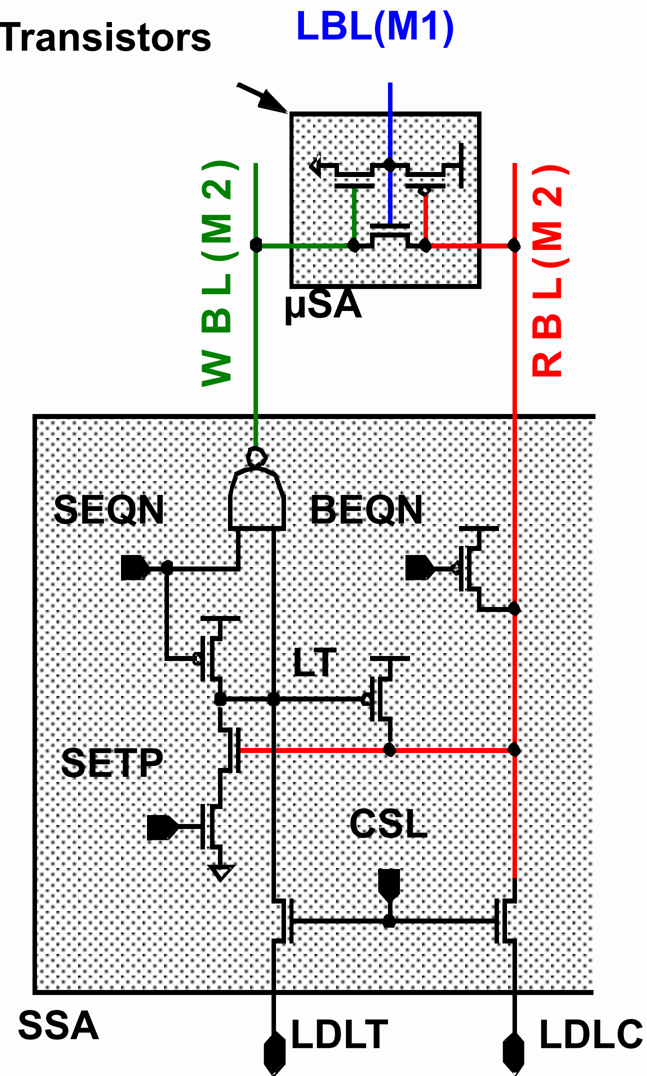
# Micro Sense Architecture (µSA)



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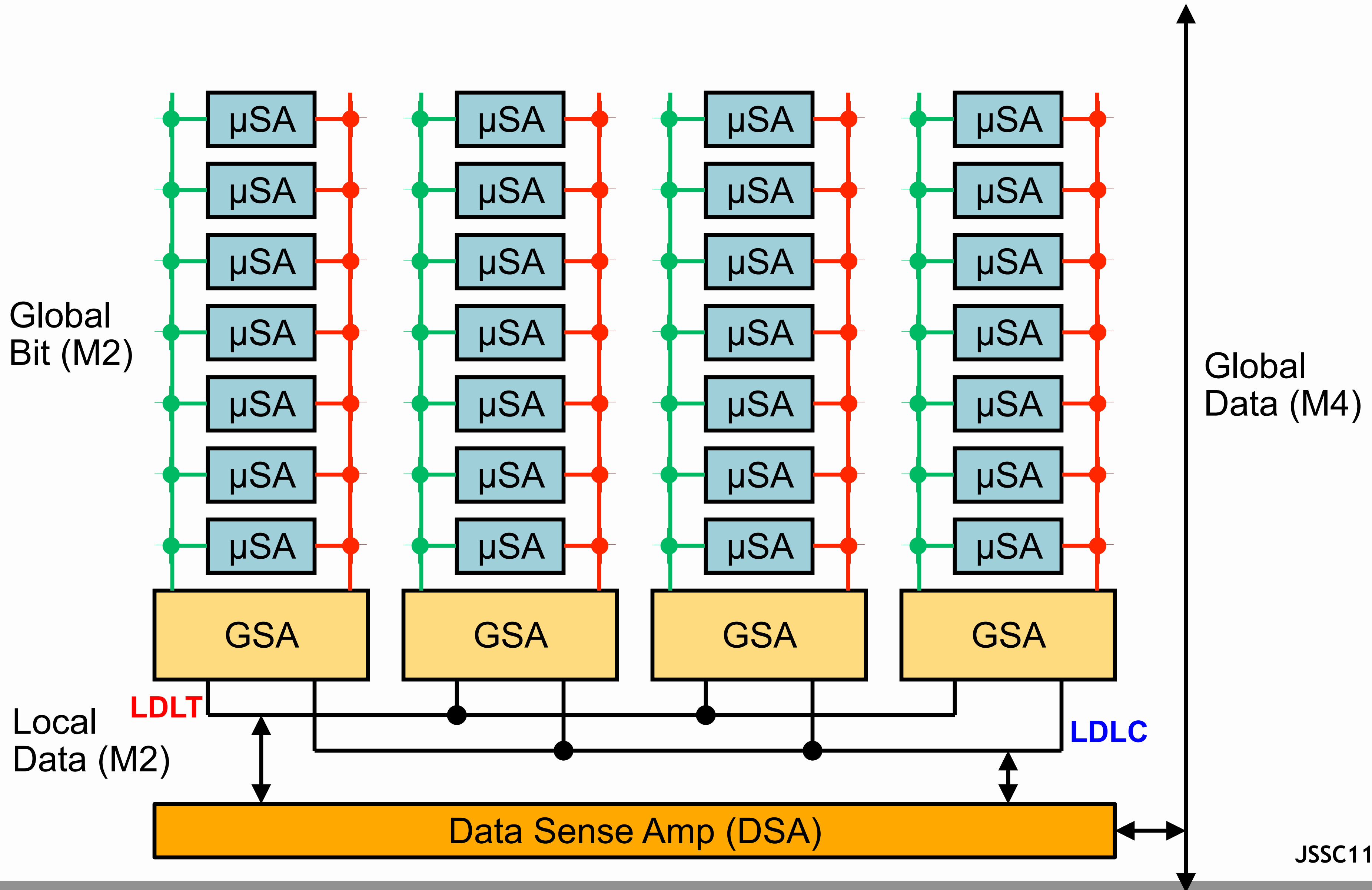
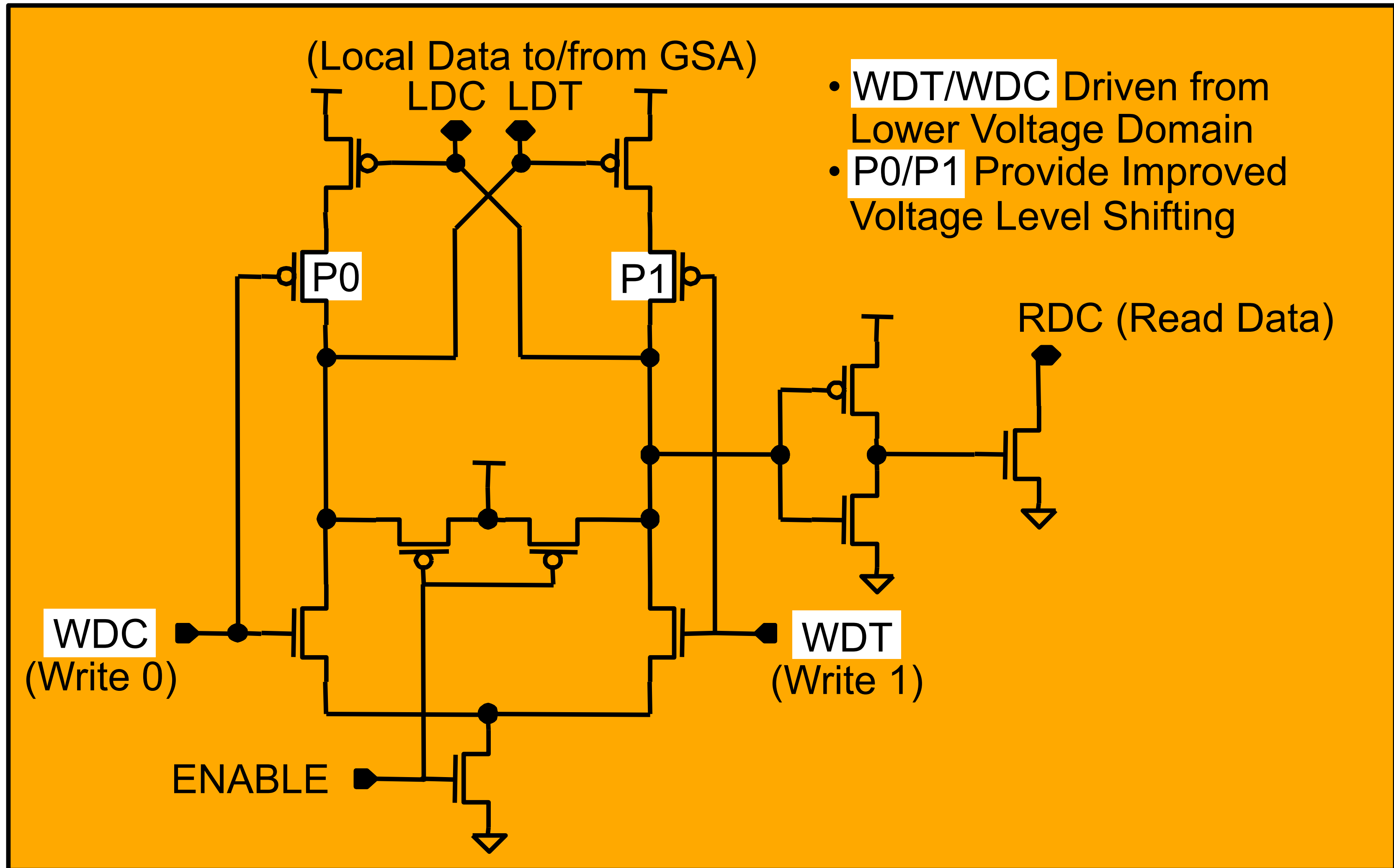
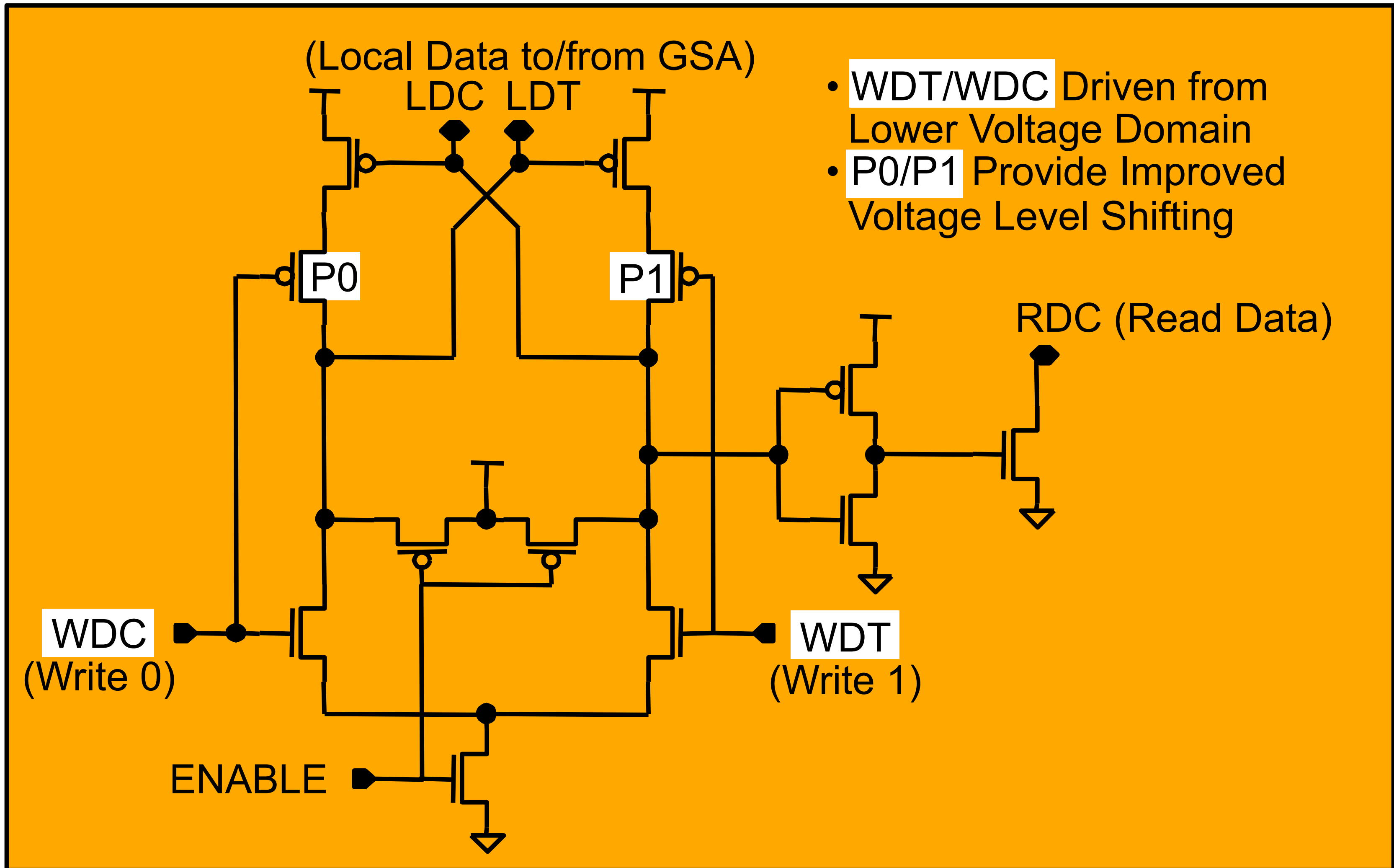


# Data Sense Amp (DSA)

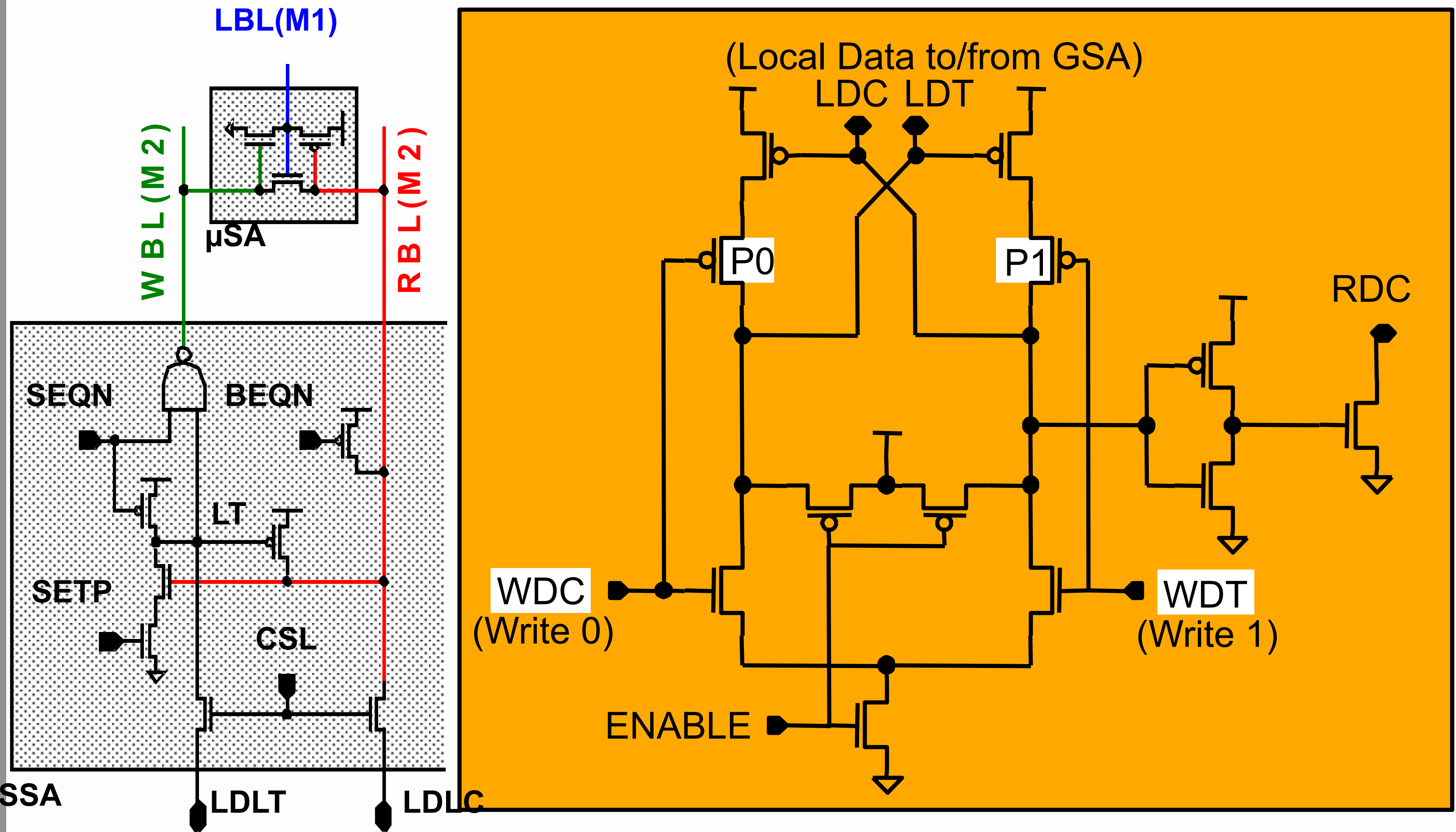


# Data Sense Amp (DSA) – Write




- WDT/WDC Driven from Lower Voltage Domain
- P0/P1 Provide Improved Voltage Level Shifting

# Data Sense Amp (DSA) – Read

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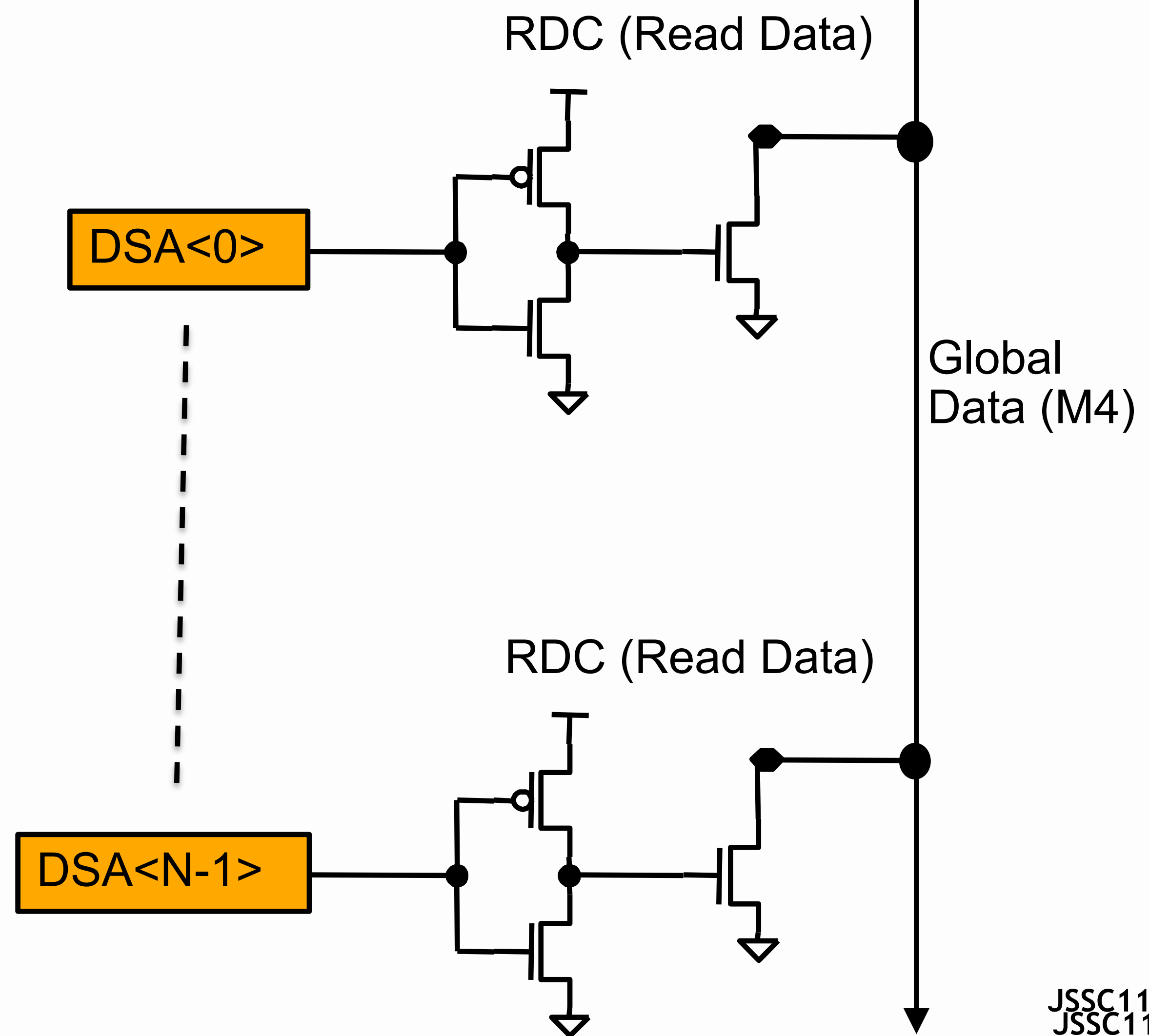
# Combining DSA's- Dynamic NOR Gate

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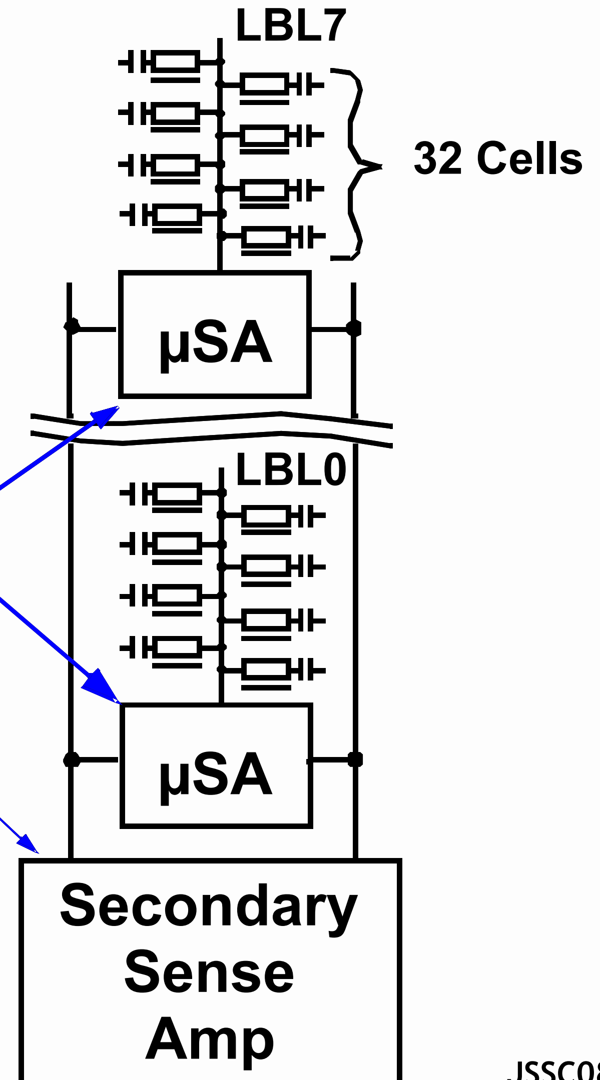
# Micro Sense Advantage

Fast Performance of Short Bit-Line

Area Overhead of 4x Longer Bit-Line

| Bits/BL | 256 | 128 | 32 |
|---|---|---|---|
| Sense Amp | 10% | 20% | 19% |
| Reference Cells | 2.3% | 4% | - |
| Twist Region | 2% | 2.6% | - |
| Second Sense Amp | - | - | 8% |
| Total | 14.3% | 26.6% | 27% |

Same Overhead

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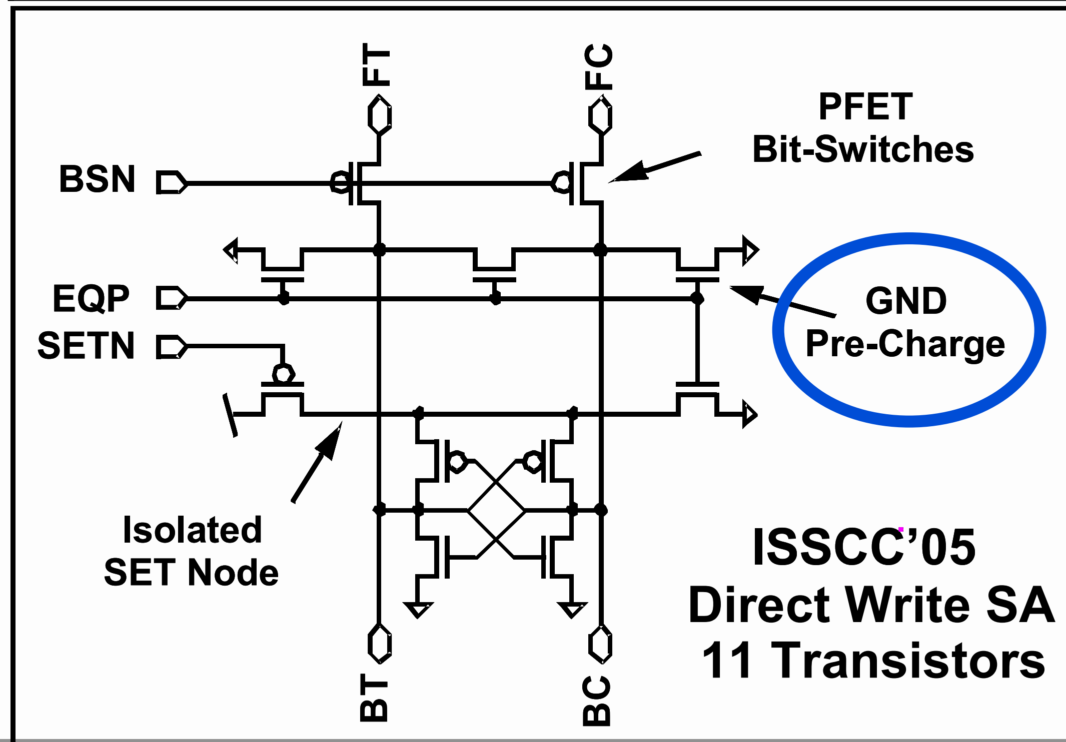
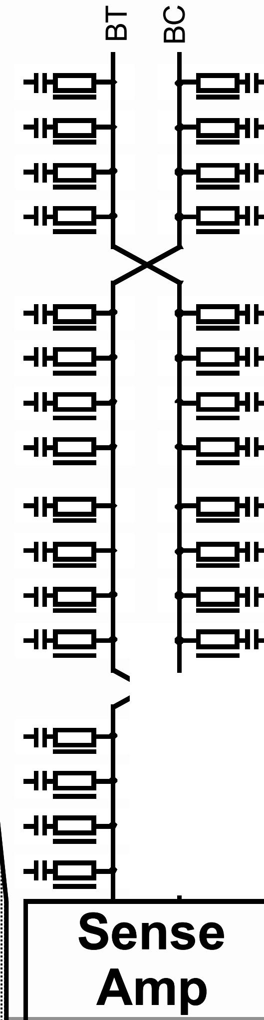
# Bit-Line area overhead

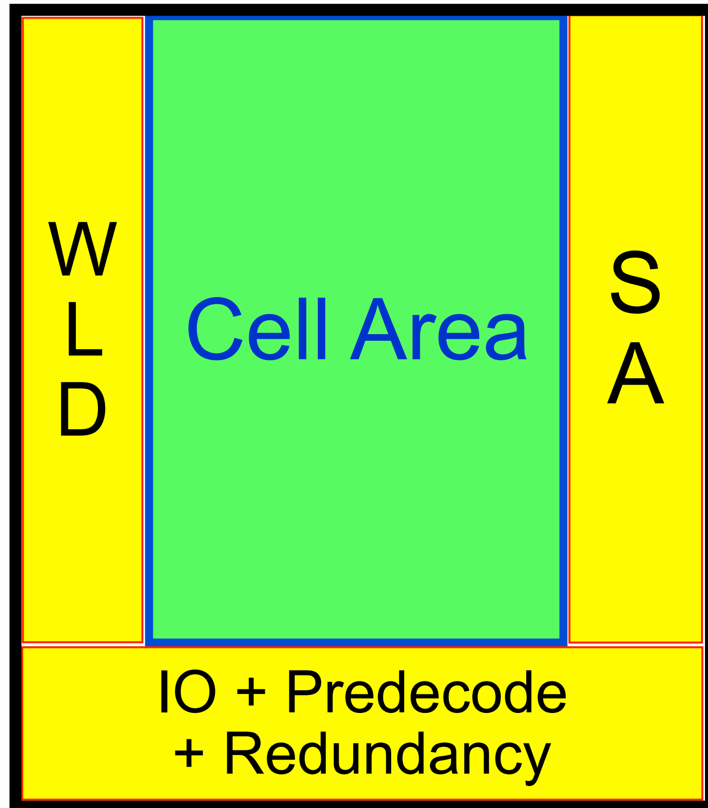
| Bits/BL | 256 | 128 | 32 |
|---|---|---|---|
| Sense Amp | 10% | 20% | > 80% |
| Reference Cells | 2.3% | 4% | |
| Twist Region | 2% | 2.6% | |

Unacceptable



# Array utilization

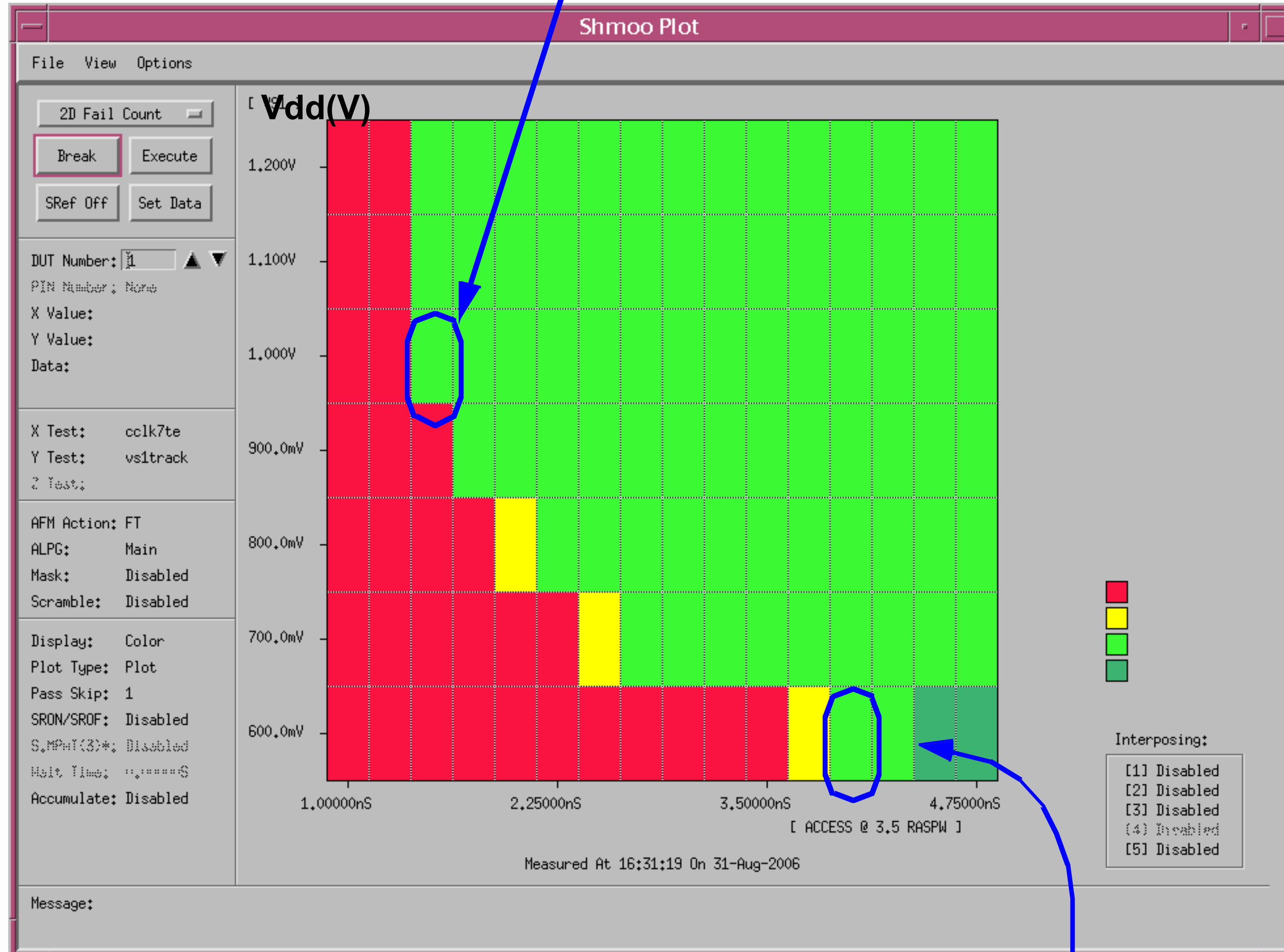



Utilization =

Mbits/mm²

# Access Shmoo

1.5ns Access @1V 85C




4ns Access @600mV

# Redundancy

Notebook

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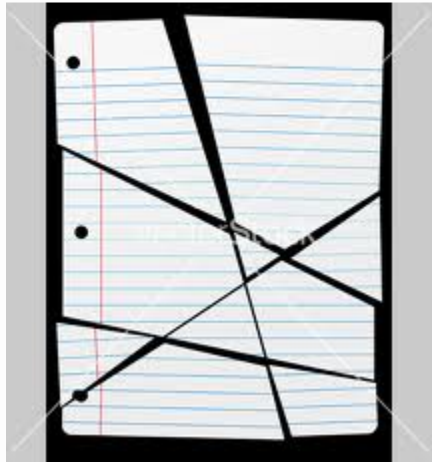
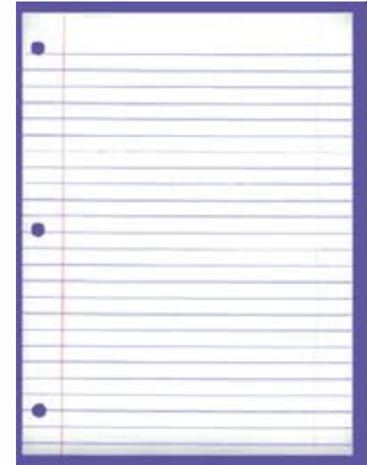


Extra Page R05



eFuse based repair table

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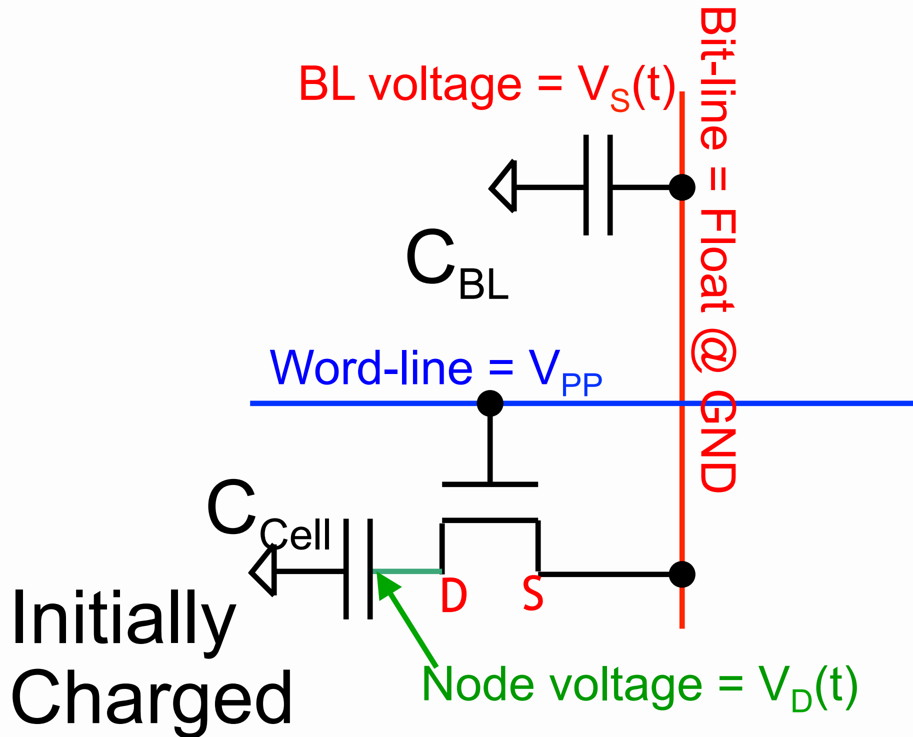
| 110 | 1 - MAY 1999 EXP 30 CONTD |
| 111 | 1-MAY 1999 EXP 31 |
| 112 | 1- MAY 1999 EXP 31 CONTD. |
| | |

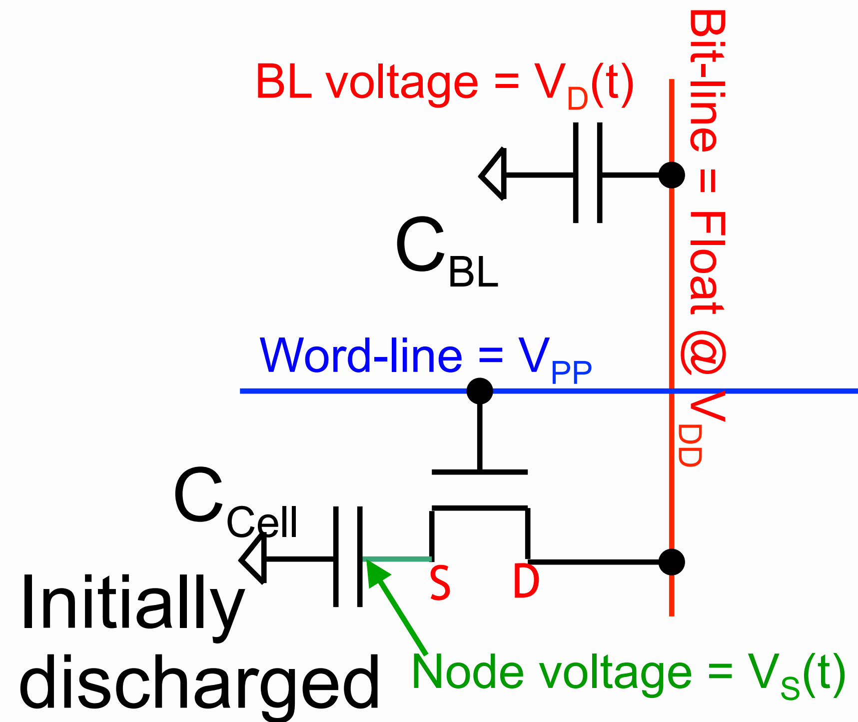
(see page R05)

# Topics

- Introduction to memory
- DRAM basics and bitcell array
- eDRAM Write Analysis
- eDRAM Sense-Amplifier Specification
- eDRAM operational details (case study)
- eDRAM Read Analysis
- Noise concerns
- Wordline driver (WLDRV) and level translators (LT)
- Challenges in eDRAM

# Read Time Calculation




BL – Pre-discharged
Read-1

BL – Pre-charged
Read-0

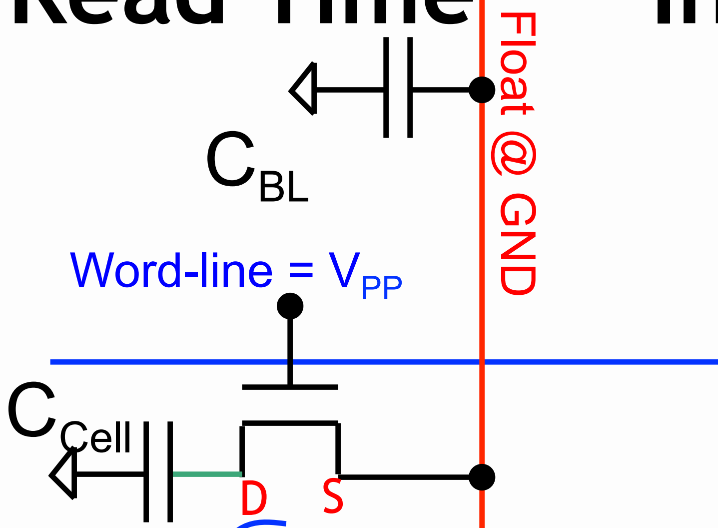
Read time : Let us define it as time required for BL to reach $V_{DD}/2$

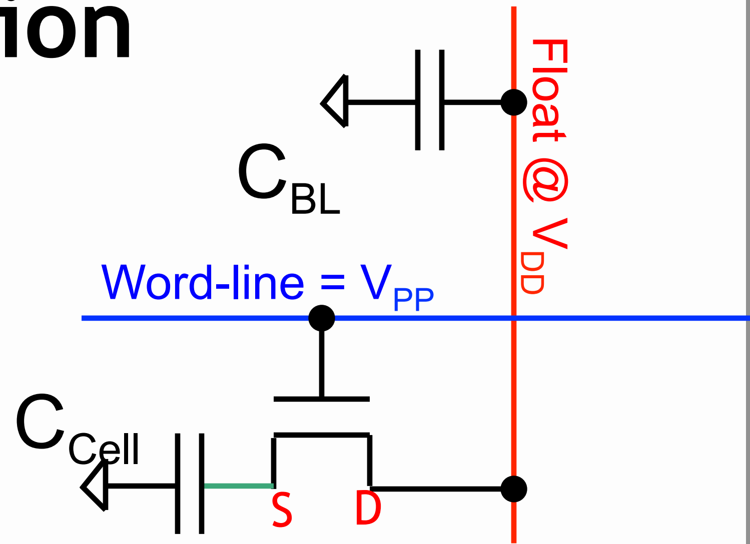
# Read Time

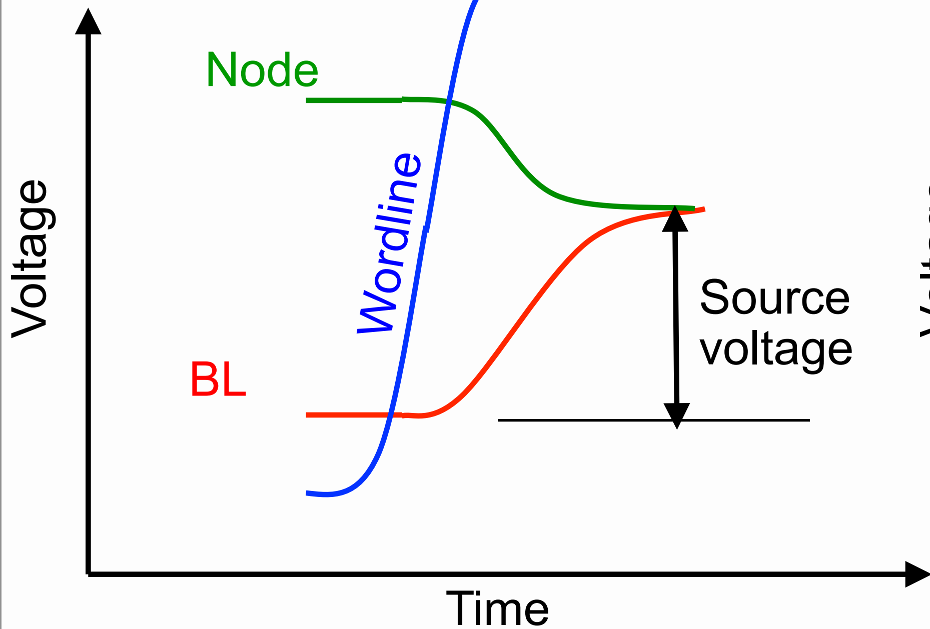
| | BL pre-discharged | BL pre-charged |
|---|---|---|
| Source | BL | Node |
| Drain | Node | BL |
| Initial Charge | $C_{Cell} V_{DD}$ | $C_{BL} V_{DD}$ |
| Charge | $C_{Cell} V_D + C_{BL} V_S = C_{Cell} V_{DD}$ | $C_{Cell} V_S + C_{BL} V_D = C_{BL} V_{DD}$ |
| Charging Equation | $I_{DS}[\frac{1}{C_{Cell}} + \frac{1}{C_{BL}}] = -\frac{dV_{DS}}{dt}$ | |
| Current | $I_{DS} = \mu_n C_{OX} \frac{W}{L} V_{DS}(V_{PP} - V_{Tn} - V_S - V_{DS}/2)$ | |
| $V_S$ | $\alpha(V_{DD} - V_{DS})$ | $(1 - \alpha)(V_{DD} - V_{DS})$ |
| $\alpha$ | $\frac{C_{Cell}}{C_{Cell} + C_{BL}}$ | |
| $I_{DS}$ | $KV_{DS}(\Delta_1 + (\alpha - 0.5)V_{DS})$ | $KV_{DS}(\Delta_2 - (\alpha - 0.5)V_{DS})$ |
| $K$ | $\frac{C_{EFF}}{\mu_n C_{OX}(W/L)}$; $C_{EFF} = \frac{C_{Cell} C_{BL}}{C_{Cell} + C_{BL}}$ | |
| $\Delta$ | $\Delta_1 = V_{PP} - V_{Tn} - \alpha V_{DD}$ | $\Delta_2 = V_{PP} - V_{Tn} - (1 - \alpha)V_{DD}$ |

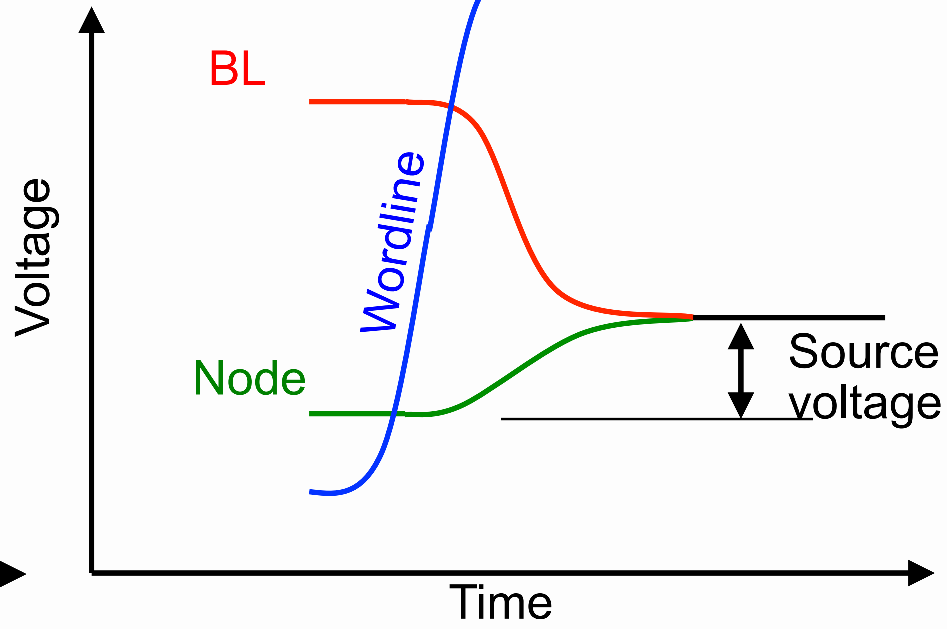
| | **BL pre-discharged** | **BL pre-charged** |
|---|---|---|
| Read Threshold | $V_S = V_{DD}/2$ | $V_D = V_{DD}/2$ |
| $V_{DS-TH}$ ($V_{FINAL}$) | $\frac{V_{DD}}{2}(1 - \frac{C_{BL}}{C_{Cell}})$ | |
| $T_{WRITE}$ | $-K \int_{V_{DD}}^{V_{FINAL}} \frac{dV_{DS}}{V_{DS}(\Delta_1+(\alpha-0.5)V_{DS})}$ | $-K \int_{V_{DD}}^{V_{FINAL}} \frac{dV_{DS}}{V_{DS}(\Delta_2-(\alpha-0.5)V_{DS})}$ |
| $T_{WRITE}$ | $\frac{K}{\Delta_1} ln(\frac{V_{DD}(\Delta_1+(\alpha-0.5)V_{FINAL})}{V_{FINAL}(\Delta_1+(\alpha-0.5)V_{DD})})$ | $\frac{K}{\Delta_2} ln(\frac{V_{DD}(\Delta_2+(0.5-\alpha)V_{FINAL})}{V_{FINAL}(\Delta_2+(0.5-\alpha)V_{DD})})$ |

# Read Time Intuition



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- ❑ eDRAM operational details (case study)
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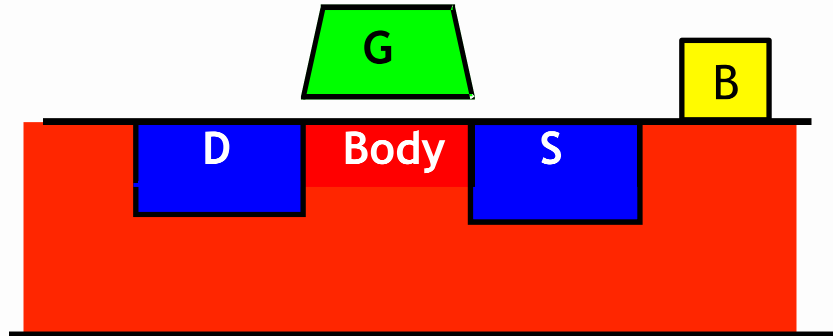
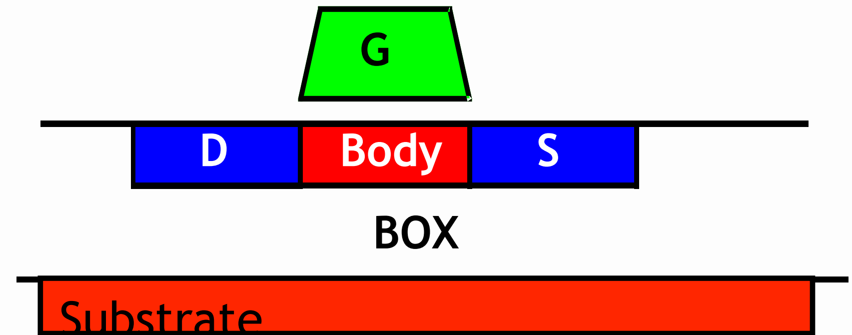
- ❑ Challenges in eDRAM

# Bulk vs SOI Technology




Body contact can be used to fix the body potential in bulk technology
SOI Technology

- Floating body is a problem
- History effect
- SOI provides better sub-threshold slope
- Higher performance with lower leakage

# Floating Body Effects

Body potential modulated by coupling and leakage

Better source follower vs. bulk during write back (body coupling)

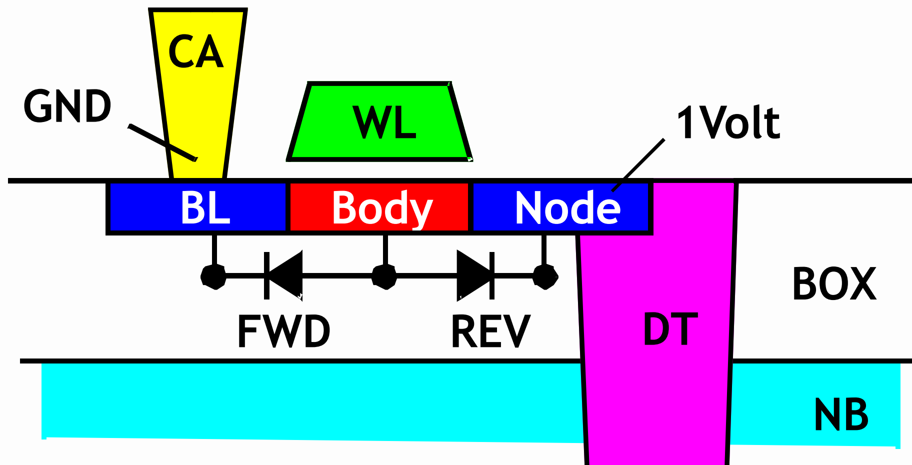
- Improved write ‘1’ cell voltage

Degraded $I_{off}$/ Retention if body floats high (body leakage)

- GND pre-charge keeps body low
- Eliminate long periods with BL high (limit page mode)

$ILeak_{FWD} > ILeak_{REV}$

When BL = GND
Body ~ GND

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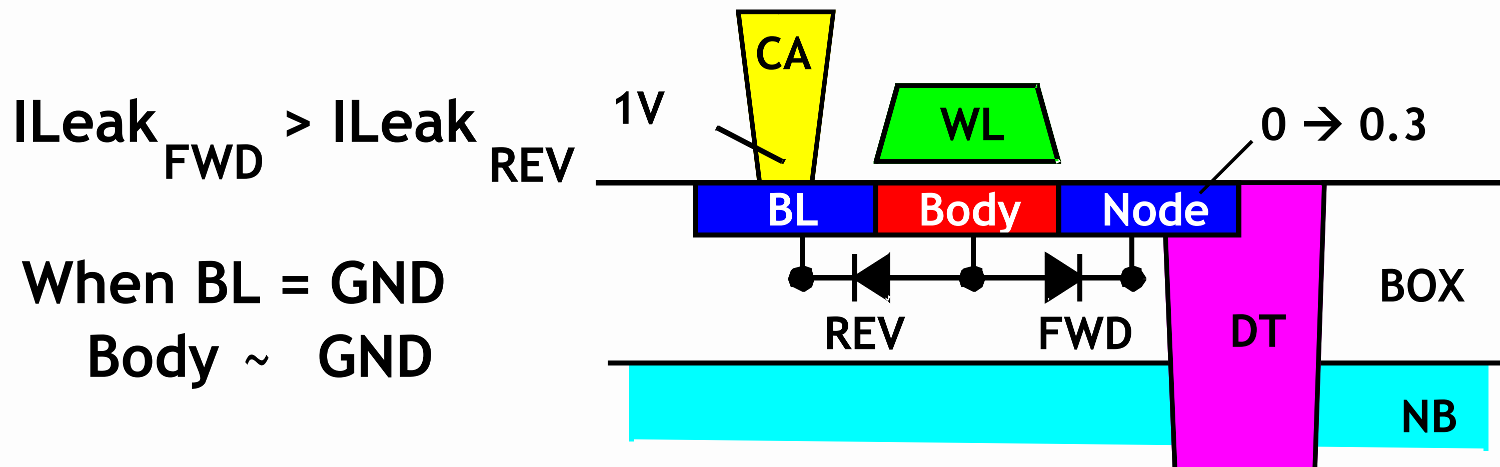


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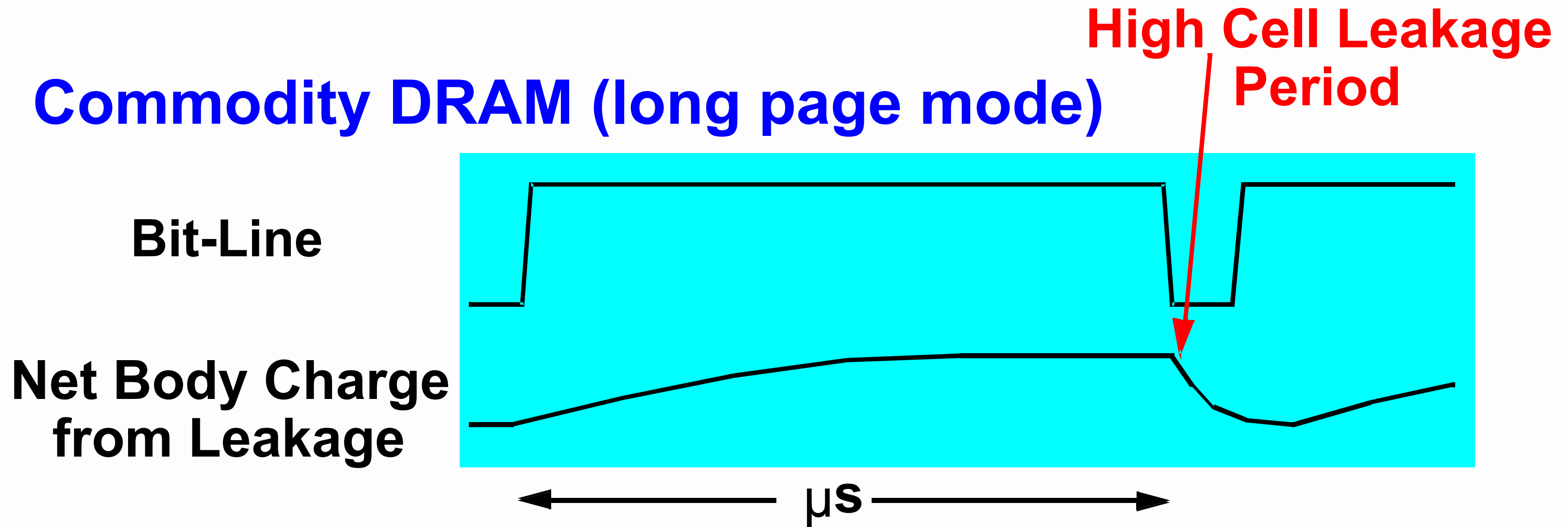
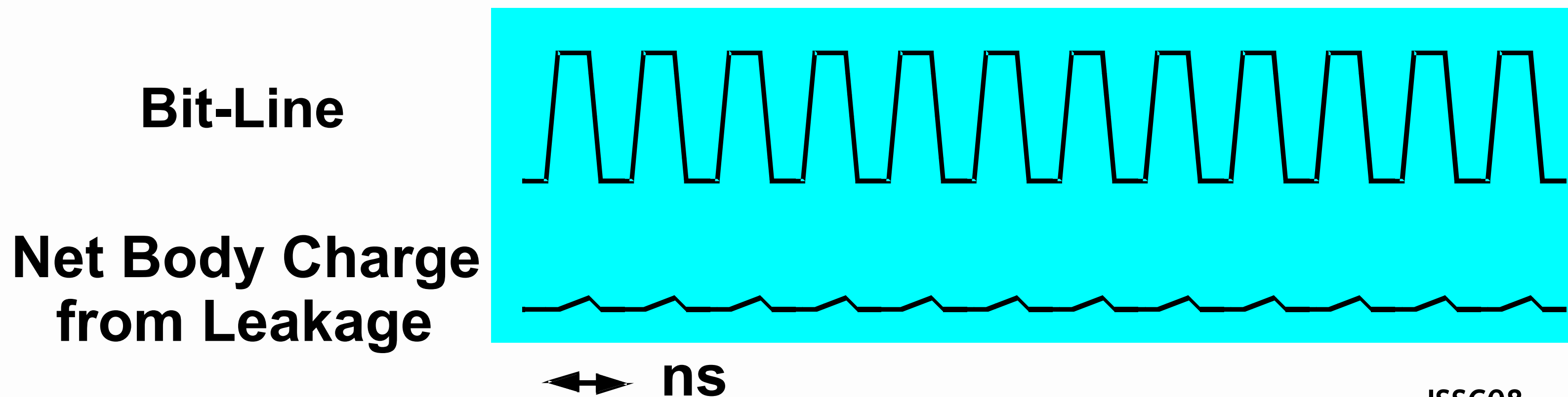
# Array Body Charging

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