DRAM Operation Details (Case Study)

A 500 MHz Random Cycle, 1.5 ns Latency, SOI Embedded DRAM Macro Featuring a Three-Transistor Micro Sense Amplifier (John Barth/IBM)
• Hierarchical Direct Sense
• Short Local Bit-Line (LBL)
  - 33 Cells per LBL
• 8 Micro Sense Amps (µSA) per Global Sense Amp (GSA)
• Write Bit-Line (WBL)
  Uni-Directional
• Read Bit-Line (RBL)
  Bi-Directional
Sense Hierarchy - Motivation

Long interconnect – Needs Buffering
3T uSA operation

**Pre-charge**
WL is low. WBL and RBL both pre-charged to HIGH. Next GSA drives WBL low. **LBL floats to GND level**

**Read “0”**
LBL remains LOW. RBL is HIGH. Sensed as a “0”

**Read “1”**
LBL is HIGH. Turns on RH, pulls RBL LOW. + feedback as pFET FB turns ON. Sensed as a “1”

**Write “1”**
GSA pulls RBL to GND. FB pFET turns ON
Happens while WL rises (direct write)

**Write “0”**
WBL is HIGH, PCW0 ON. Clamps LBL to GND
As WL activates.
Simulations - Write

Nominal Process, 1v, 85°C

Volts
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
-0.2

Time(ns)
0.0
0.4
0.8
1.2
1.6
2.0
2.4
2.8
3.2
3.6
4.0

Write ‘1’
Write ‘0’

Restore

WBL
RBL
LBL
Node

Strong ‘1’
Strong ‘0’

μSA

JSSC08
Simulations - Read
Micro Sense Hierarchy - Three levels

Global Bit (M2)

Local Data (M2)

Global Data (M4)

Data Sense Amp (DSA)

GSA

µSA

µSA

µSA

µSA

µSA

µSA

µSA

µSA

JSSC11
GSA Should fit into the bitcell width or \( n \times \text{bitcell width} \)

Thus, distributed GSA on two sides of bitcell array
• 1 of 8 Column Select Lines (CSL)
• Fire Early for Write
• Fire Late to Support Concurrent Cache Directory Lookup
LAYOUT of array

- GSA
- WL POLY
- WBL0
- RBL0
- LBL00
- WL0 M3

- GSA
- WL POLY
- WBL1
- RBL1
- LBL10
- WL1 M3

- RBL0
- LBL00
- LBL10

- LBL01
- LBL11

- LBL07
- LBL17
Micro Sense Local Bit-line Cross Section

Single Ended Sense – Twist not effective
Line to Line Coupling must be managed
Micro Sense Coupling Mechanisms

1. Write ‘1’ Couples WBL below Ground Increasing RH leakage during Refresh ‘0’
2. Write ‘0’ Couples RBL above VDD Delaying Feedback during Refresh ‘1’
3. Read ‘1’ Couples Half-Selected LBL Below GND Increasing Array Device Sub-VT Leakage
- Accessing one of WL0-32
- Cell connected is on LBL00
- LBL01-07 – Half Selected LBLs
**Micro Sense Evolution**

1. Write Zero (W0)
2. Read Head (RH)
3. Feed-Back (FB)

4. PFET Header (PH)
   - LBL Power Gate
   - LBL Leakage

5. Pre-Charge (PC)
   - WBL Power (Write ‘0’ Only)

6. NFET Footer (NF)
   - RBL Leakage
   - Decompose Pre-Charge and Read Enable (MWL_RE)

Power Reduction Traded for Transistor Count

Barth, ISSCC’07

Klim, VLSI’07

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Micro Sense Hierarchy - Three levels

Global Bit (M2)

Global Data (M4)

Local Data (M2)

Data Sense Amp (DSA)

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Micro Sense Architecture (μSA)

- 3 Transistors
- LBL(M1)
- Cell(20fF)
- LBL7(4fF)
- Local BL 32 Cells
- Global BL 8 μSA
- 32 Cells
- Cell(20fF)
- μSA
- LBL0
- μSA
- LBL7(4fF)
- μSA
- LBL0
- 3 Transistors
- LBL(M2)
- W BL (M 2)
- μSA
- μSA
- LBL(M2)
- R BL (M 2)
- Micro Sense
- μSA
- Secondary Sense Amp
- μSA
- R BL (12fF)
- W BL (12fF)
- μSA
- μSA
- μSA
- μSA
- BEQN
- SEQN
- LT
- SETP
- CSL
- SSA
- LDLT
- LDLC
- JSSC08
Micro Sense Architecture (μSA)

Process, 1v, 85c

3 Transistors

LBL(M1)

μSA

Load

SETP

SEQN

BEQN

LT

CSL

SSA

LDLT

LDLC

3 Transistors

LBL(M1)

μSA

Load

SETP

SEQN

BEQN

LT

CSL

SSA

LDLT

LDLC
Micro Sense Hierarchy - Three levels

Data Sense Amp (DSA)

Local Data (M2)

Global Bit (M2)

Global Data (M4)

LDLT

LDLC

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Data Sense Amp (DSA)

- WDT/WDC Driven from Lower Voltage Domain
- P0/P1 Provide Improved Voltage Level Shifting

(Local Data to/from GSA) LDC LDT

RDC (Read Data)

WDC (Write 0)

WDT (Write 1)

ENABLE
Data Sense Amp (DSA) – Write

(Local Data to/from GSA)

- WDT/WDC Driven from Lower Voltage Domain
- P0/P1 Provide Improved Voltage Level Shifting

RDC (Read Data)

WDC (Write 0)

WDT (Write 1)

ENABLE
Data Sense Amp (DSA) – Read

(Local Data to/from GSA) LDC LDT

(Write 0) WDC

(Write 1) WDT

ENABLE

BL(M1)

µSA

SEQN

BEQN

LT

CSL

SSA

LDLC

LDLT

WBL (M2)

RBL (M2)

W

B

L
Combining DSA’s- Dynamic NOR Gate

RDC (Read Data)

Global Data (M4)

DSA<0>

DSA<N-1>

RDC (Read Data)
**Micro Sense Advantage**

Fast Performance of Short Bit-Line  
Area Overhead of 4x Longer Bit-Line

<table>
<thead>
<tr>
<th></th>
<th>256</th>
<th>128</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sense Amp</td>
<td>10%</td>
<td>20%</td>
<td>19%</td>
</tr>
<tr>
<td>Reference Cells</td>
<td>2.3%</td>
<td>4%</td>
<td>-</td>
</tr>
<tr>
<td>Twist Region</td>
<td>2%</td>
<td>2.6%</td>
<td>-</td>
</tr>
<tr>
<td>Second Sense Amp</td>
<td>-</td>
<td>-</td>
<td>8%</td>
</tr>
<tr>
<td>Total</td>
<td>14.3%</td>
<td>26.6%</td>
<td>27%</td>
</tr>
</tbody>
</table>

```
32 Cells
```

![Diagram of memory device with labels and connections]

**JSSC08**
Bit-Line area overhead

<table>
<thead>
<tr>
<th>Bits/BL</th>
<th>256</th>
<th>128</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sense Amp</td>
<td>10%</td>
<td>20%</td>
<td>&gt; 80%</td>
</tr>
<tr>
<td>Reference Cells</td>
<td>2.3%</td>
<td>4%</td>
<td>&gt; 80%</td>
</tr>
<tr>
<td>Twist Region</td>
<td>2%</td>
<td>2.6%</td>
<td>&gt; 80%</td>
</tr>
</tbody>
</table>

Unacceptable

ISSCC’05
Direct Write SA
11 Transistors

Unacceptable

GND Pre-Charge

Isolated SET Node
Array utilization

Utilization = \frac{\text{Cell Area}}{\text{IO + Predecode + Redundancy}} \text{ Mbits/mm}^2
Access Shmoo

1.5ns Access @1V 85C

4ns Access @600mV
Redundancy

Notebook

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Extra Page R05

eFuse based repair table

(see page R05)
Topics

- Introduction to memory
- DRAM basics and bitcell array
- eDRAM Write Analysis
- eDRAM Sense-Amplifier Specification
- eDRAM operational details (case study)
- eDRAM Read Analysis
- Noise concerns
- Wordline driver (WLDRV) and level translators (LT)
- Challenges in eDRAM
Read Time Calculation

Initially Charged

Initially discharged

BL – Pre-discharged
Read-1

BL – Pre-charge
Read-0

Read time: Let us define it as time required for BL to reach \( V_{DD}/2 \)
# Read Time

<table>
<thead>
<tr>
<th>Source</th>
<th>BL pre-discharged</th>
<th>BL pre-charged</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain</td>
<td>Node</td>
<td>BL</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Initial Charge</th>
<th>$C_{cell} V_{DD}$</th>
<th>$C_{BL} V_{DD}$</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Charge</th>
<th>$C_{cell} V_{D} + C_{BL} V_{S} = C_{cell} V_{DD}$</th>
<th>$C_{cell} V_{S} + C_{BL} V_{D} = C_{BL} V_{DD}$</th>
</tr>
</thead>
</table>

## Charging Equation

$$I_{DS} \left[ \frac{1}{C_{cell}} + \frac{1}{C_{BL}} \right] = -\frac{dV_{DS}}{dt}$$

### Current

$$I_{DS} = \mu_n C_{OX} \frac{W}{L} V_{DS}(V_{PP} - V_{Tn} - V_{S} - V_{DS}/2)$$

### $V_{S}$

- $\alpha(V_{DD} - V_{DS})$
- $(1 - \alpha)(V_{DD} - V_{DS})$

### $\alpha$

$$\frac{C_{cell}}{C_{cell} + C_{BL}}$$

### $I_{DS}$

- $K V_{DS} (\Delta_1 + (\alpha - 0.5) V_{DS})$
- $K V_{DS} (\Delta_2 - (\alpha - 0.5) V_{DS})$

### $K$

$$\frac{C_{EFF}}{\mu_n C_{OX} (W/L)}; \quad C_{EFF} = \frac{C_{cell} C_{BL}}{C_{cell} + C_{BL}}$$

### $\Delta$

- $\Delta_1 = V_{PP} - V_{Tn} - \alpha V_{DD}$
- $\Delta_2 = V_{PP} - V_{Tn} - (1 - \alpha) V_{DD}$

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Introduction of eDRAM
### Introduction of eDRAM

#### Slide 33

<table>
<thead>
<tr>
<th></th>
<th>BL pre-discharged</th>
<th>BL pre-charged</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Read Threshold</strong></td>
<td>( V_S = V_{DD}/2 )</td>
<td>( V_D = V_{DD}/2 )</td>
</tr>
<tr>
<td>( V_{DS-TH} (V_{FINAL}) )</td>
<td>( \frac{V_{DD}}{2} (1 - \frac{C_{BL}}{C_{Cell}}) )</td>
<td></td>
</tr>
<tr>
<td><strong>( T_{WRITE} )</strong></td>
<td>(-K \int_{V_{DD}}^{V_{FINAL}} \frac{dV_{DS}}{V_{DS}(\Delta_1 + (\alpha - 0.5)V_{DS})} )</td>
<td>(-K \int_{V_{DD}}^{V_{FINAL}} \frac{dV_{DS}}{V_{DS}(\Delta_2 - (\alpha - 0.5)V_{DS})} )</td>
</tr>
<tr>
<td>( T_{WRITE} )</td>
<td>( \frac{K}{\Delta_1} \ln \left( \frac{V_{DD}(\Delta_1 + (\alpha - 0.5)V_{FINAL})}{V_{FINAL}(\Delta_1 + (\alpha - 0.5)V_{DD})} \right) )</td>
<td>( \frac{K}{\Delta_2} \ln \left( \frac{V_{DD}(\Delta_2 + (0.5 - \alpha)V_{FINAL})}{V_{FINAL}(\Delta_2 + (0.5 - \alpha)V_{DD})} \right) )</td>
</tr>
</tbody>
</table>
Introduction of eDRAM

Read Time

\[ C_{BL} \]

Word-line = \( V_{PP} \)

Float @ GND

\[ C_{Cell} \]

D S

Node

Voltage

Time

Source voltage

Intuition

\[ C_{BL} \]

Word-line = \( V_{PP} \)

Float @ \( V_{DD} \)

\[ C_{Cell} \]

S D

Node

Voltage

BL

Voltage

Time

Source voltage
Topics

- Introduction to memory
- DRAM basics and bitcell array
- eDRAM Write Analysis
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- eDRAM Read Analysis
- SOI Technology
- Wordline driver (WLDRV) and level translators (LT)
- Challenges in eDRAM
Body contact can be used to fix the body potential in bulk technology.

SOI Technology:
- Floating body is a problem
- History effect
- SOI provides better sub-threshold slope
- Higher performance with lower leakage
Floating Body Effects

Body potential modulated by coupling and leakage

Better source follower vs. bulk during write back (body coupling)

Improved write ‘1’ cell voltage

Degraded $I_{\text{off}}$ / Retention if body floats high (body leakage)

GND pre-charge keeps body low

Eliminate long periods with BL high (limit page mode)

$I_{\text{Leak}}^{\text{FWD}} > I_{\text{Leak}}^{\text{REV}}$

When BL = GND

Body ~ GND

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Floating Body Effects

Body potential modulated by coupling and leakage
Better source follower vs. bulk during write back (body coupling)

Improved write ‘1’ cell voltage

Degraded $I_{off}$ / Retention if body floats high (body leakage)
GND pre-charge keeps body low

Eliminate long periods with BL high (limit page mode)

When BL = GND

Body ~ GND
Array Body Charging

Commodity DRAM (long page mode)

Bit-Line

Net Body Charge from Leakage

μs

embedded DRAM (limited page mode)

Bit-Line

Net Body Charge from Leakage

ns

High Cell Leakage Period