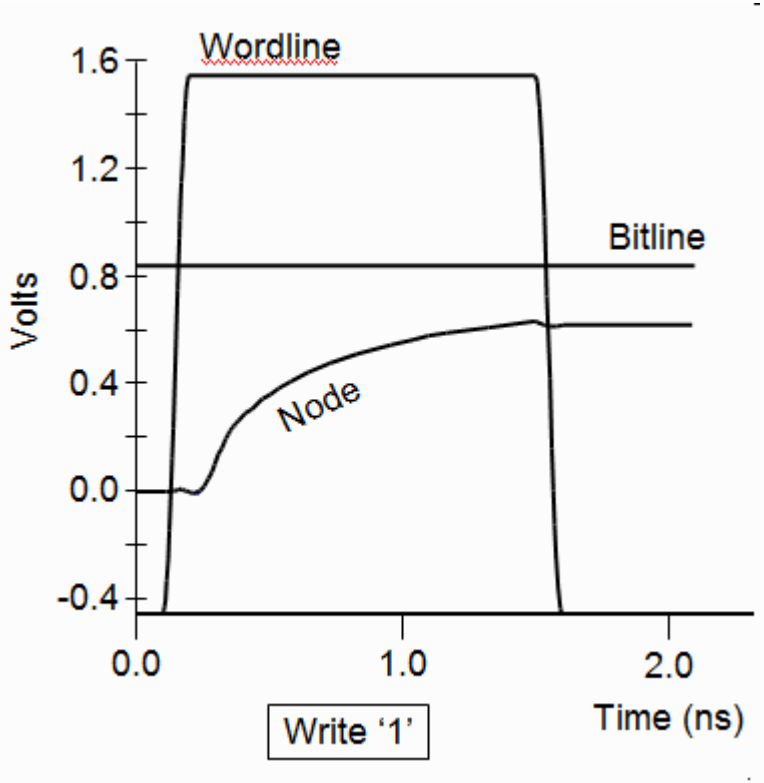
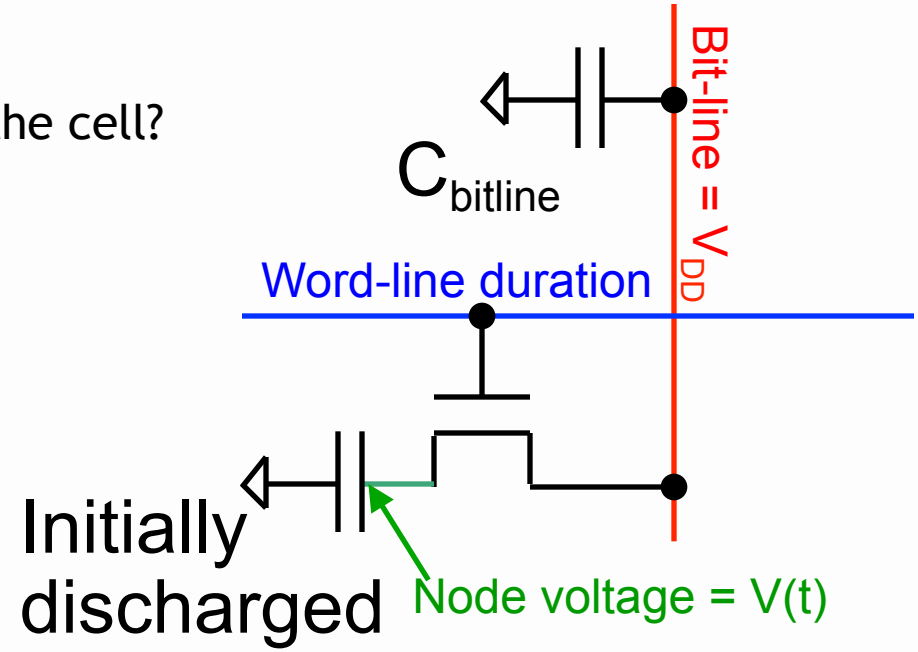
Topics

- ❑ Introduction to memory
- ❑ DRAM basics and bitcell array
- ❑ eDRAM Write Analysis
- ❑ eDRAM Sense-Amplifier Specification
- ❑ eDRAM operational details (case study)
- ❑ Noise concerns
- ❑ Wordline driver (WLDRV) and level translators (LT)
- ❑ Challenges in eDRAM
- ❑ Understanding Timing diagram – An example

Write-Margin

How much signal can we write into the cell?





Write-Margin

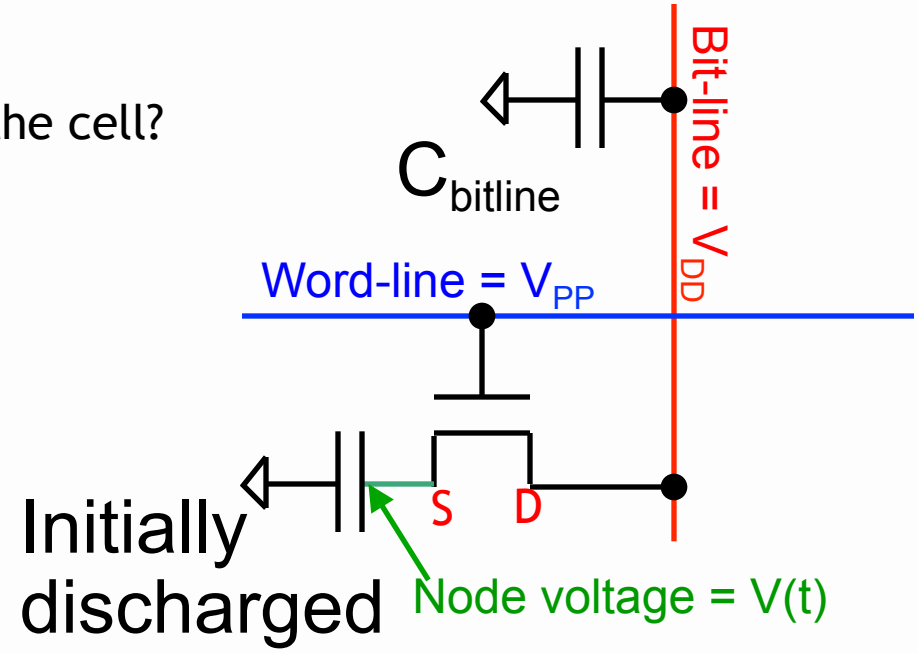
How much signal can we write into the cell?

Assume:

- Bit-line is charged to V_{DD}
- Word-line rises instantly to V_{PP}

$V_{GS} = V_{PP} - V(t)$

$V_{DS} = V_{DD} - V(t)$



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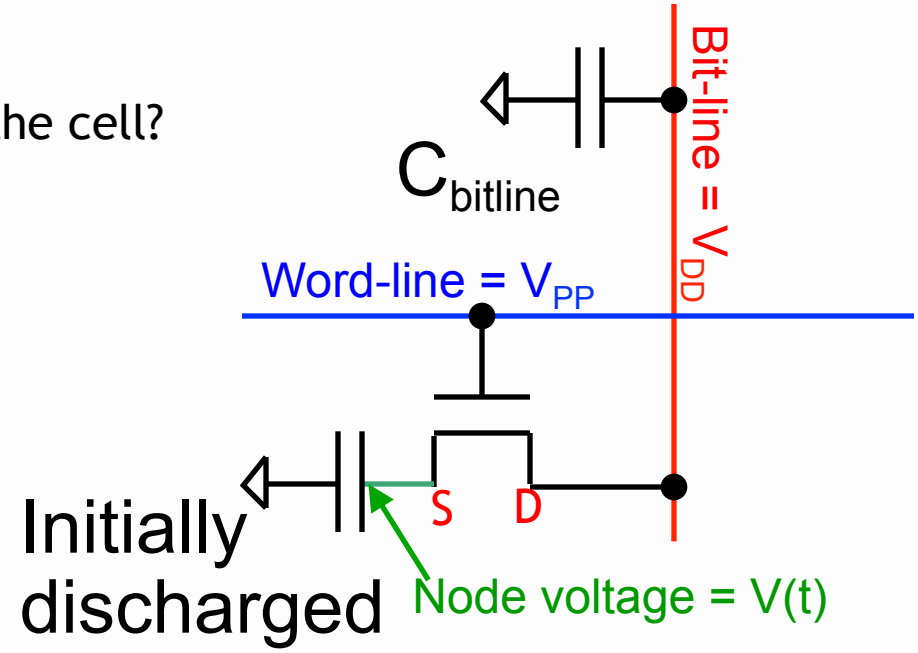


Assume:

- Bit-line is charged to V_{DD}
- Word-line rises instantly to V_{PP}

$V_{GS} = V_{PP} - V(t)$

$V_{DS} = V_{DD} - V(t)$

Access transistor is a thick oxide device => $V_{DSAT} >> V_{PP}$

$V_{DS} = V_{DD} - V(t) < V_{GS} - V_{Tn} = V_{PP} - V(t) - V_{Tn}$

$V_{PP} \geq V_{DD} + V_{Tn} + \Delta V_{Tn}$

Access device is in the linear region throughout

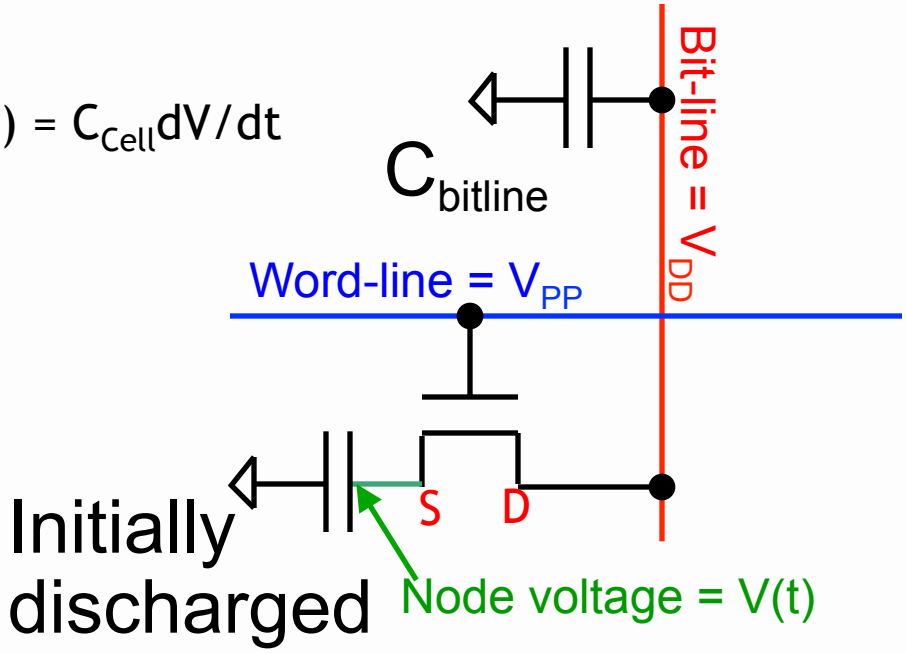
Write-Margin

$I_{DS} = \mu_n C_{OX} (W/L) V_{DS} (V_{GS} - V_{Tn} - V_{DS}/2) = C_{Cell} dV/dt$

$V_{GS} = V_{PP} - V(t)$

$V_{DS} = V_{DD} - V(t)$

Assume you wish to write a voltage V_f into the cell in a time T_{WRITE}



Solving you will get:

$T_{WRITE} = 2\ T_0\ \ln[(1-V_f/2\Delta)/(1-V_f/V_{DD})]$

Where

$T_0 = \{C_{cell}/[\mu_n C_{OX} (W/L)(2\Delta - V_{DD})]\}$

$\Delta = V_{PP} - V_{Tn} - V_{DD}/2$

$$I_{DS} = \mu_n C_{ox}\left(\frac{W}{L}\right) \cdot V_{DS}\left(V_{GS} - V_{Tn} - \frac{V_{DS}}{2}\right)$$

$$I_{DS} = C\frac{dV}{dt} \quad (C = C_{cell})$$

$$\Rightarrow K V_{DS}\left(V_{GS} - V_{Tn} - \frac{V_{DS}}{2}\right) = C\frac{dV}{dt}$$

$$K = \mu_n C_{ox}\left(\frac{W}{L}\right)$$

$$\therefore \left(\frac{K}{C}\right)\cdot(V_{DD} - V)\left(V_{PP} - V - V_{Tn} - \left(\frac{V_{DD} - V}{2}\right)\right) = \frac{dV}{dt}$$

$$\Rightarrow \left(\frac{K}{C}\right)(V_{DD} - V)\left(V_{PP} - V_{Tn} - \frac{V_{DD}}{2} - \frac{V}{2}\right) = \frac{dV}{dt}$$

$$\Rightarrow \frac{K}{C}dt = \frac{dV}{(V_{DD} - V)(\Delta - \frac{V}{2})}$$

Where $\Delta = (V_{PP} - V_{Tn} - V_{DD}/2)$

$$\Rightarrow \frac{K}{C}dt = \frac{2dV}{(2\Delta - V_{DD})} \times \left[\frac{1}{V_{DD} - V} - \frac{1}{2\Delta - V}\right]$$

$$\Rightarrow \frac{K}{C}\cdot\tau_{WRITE} = \frac{2}{2\Delta - V_{DD}} \cdot \ln\left[\frac{2\Delta - V}{V_{DD} - V}\right]\Bigg|_0^{V_f}$$

$$\Rightarrow \tau_{WRITE} = \frac{2C}{K(2\Delta - V_{DD})}\left[\ln\left[\left(\frac{2\Delta - V_f}{V_{DD} - V_f}\right)\left(\frac{V_{DD}}{2\Delta}\right)\right]\right]$$

$$\tau_{WRITE} = \frac{2C}{K(2\Delta - V_{DD})}\ln\left[\frac{1 - V_f/2\Delta}{1 - V_f/V_{DD}}\right]$$

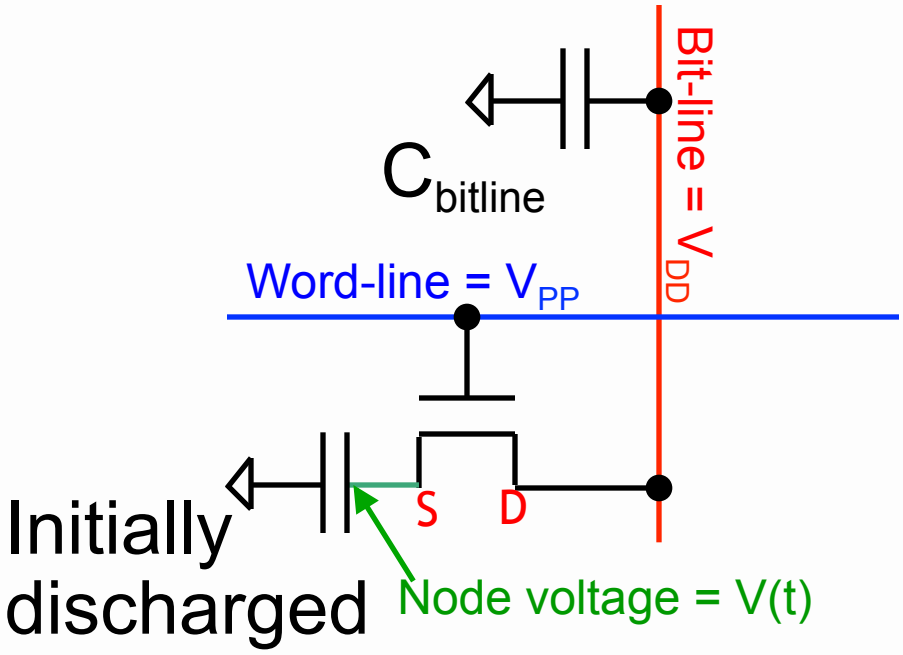
Write-Margin – Analysis

$T_{WRITE} = 2\ T_0\ \ln[(1-V_f/2\Delta)/(1-V_f/V_{DD})]$

Where

$T_0 = \{C_{cell}/[\mu_n C_{OX}\ (W/L)(2\Delta - V_{DD})]\}$

$\Delta = V_{PP} - V_{Tn} - V_{DS}/2$



1. What happens when VPP is increased?
2. What happens when V_f ➔ V_{DD}

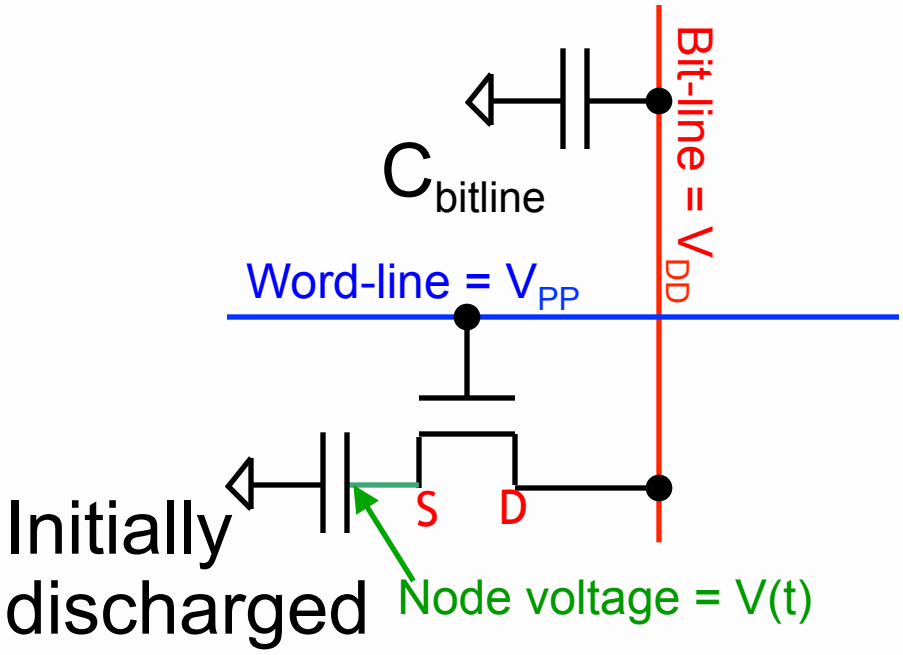
Write-Margin – Analysis

$T_{WRITE} = 2\ T_0\ \ln[(1-V_f/2\Delta)/(1-V_f/V_{DD})]$

Where

$T_0 = \{C_{cell}/[\mu_n C_{OX}\ (W/L)(2\Delta - V_{DD})]\}$

$\Delta = V_{PP} - V_{Tn} - V_{DD}/2$



1. What happens when VPP is increased?
   - Δ increases and T_0 decreases
   - $\ln[(1-V_f/2\Delta)/(1-V_f/V_{DD})]$ increases logarithmically
   - T_{WRITE} effectively decreases.
   - However WL power goes up as $(V_{PP} - V_{WL})^2$

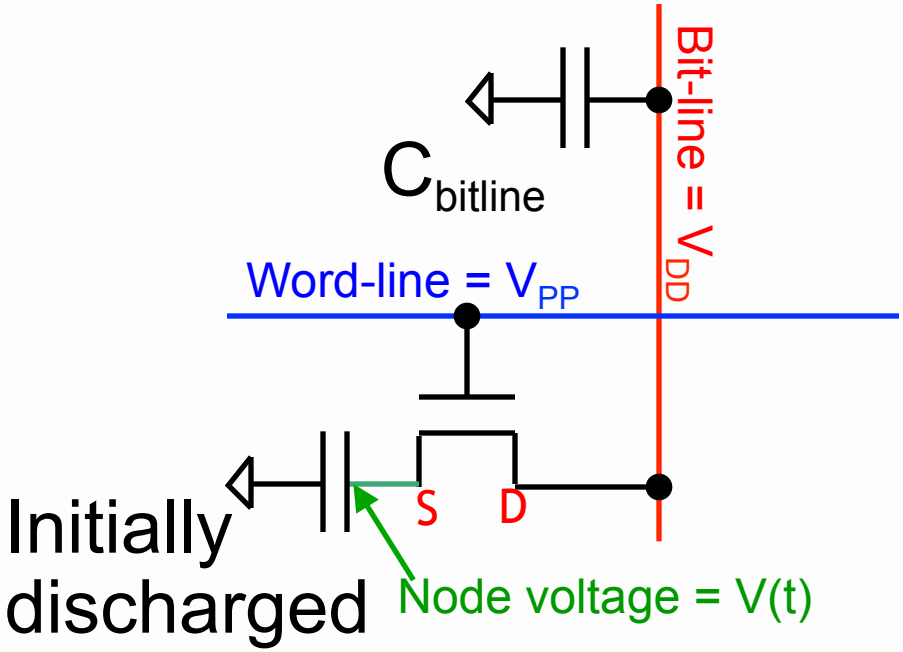
Write-Margin – Analysis

$T_{WRITE} = 2\ T_0\ \ln[(1-V_f/2\Delta)/(1-V_f/V_{DD})]$

Where

$T_0 = \{C_{cell}/[\mu_n C_{OX}\ (W/L)(2\Delta - V_{DD})]\}$

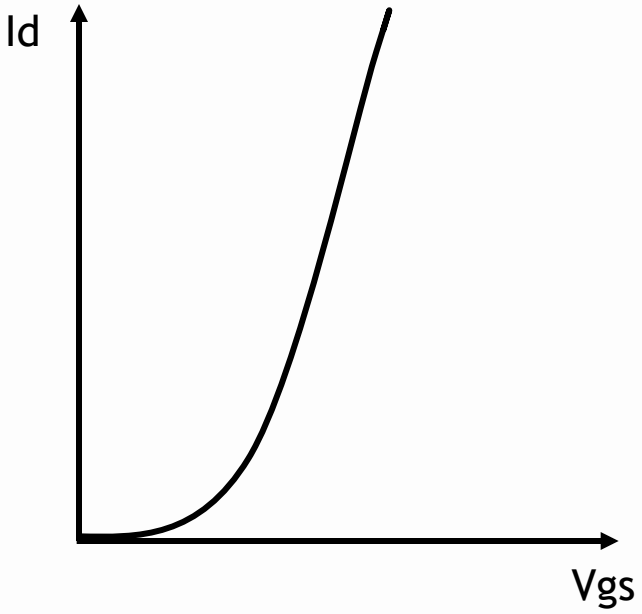
$\Delta = V_{PP} - V_{Tn} - V_{DS}/2$

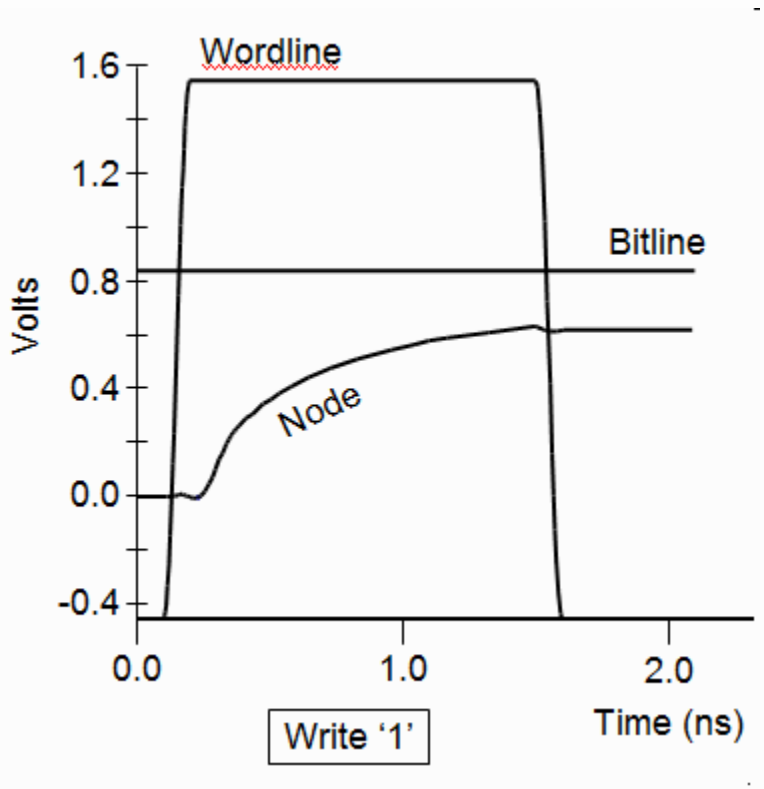


1. What happens when $V_f \rightarrow V_{DD}$
   - $(1-V_f/V_{DD})$ approaches 0
   - $\ln[(1-V_f/2\Delta)/(1-V_f/V_{DD})]$ shoots to ∞

You cannot write a FULL V_{DD} into the cell in finite time

Storing data ‘1’ in the cell

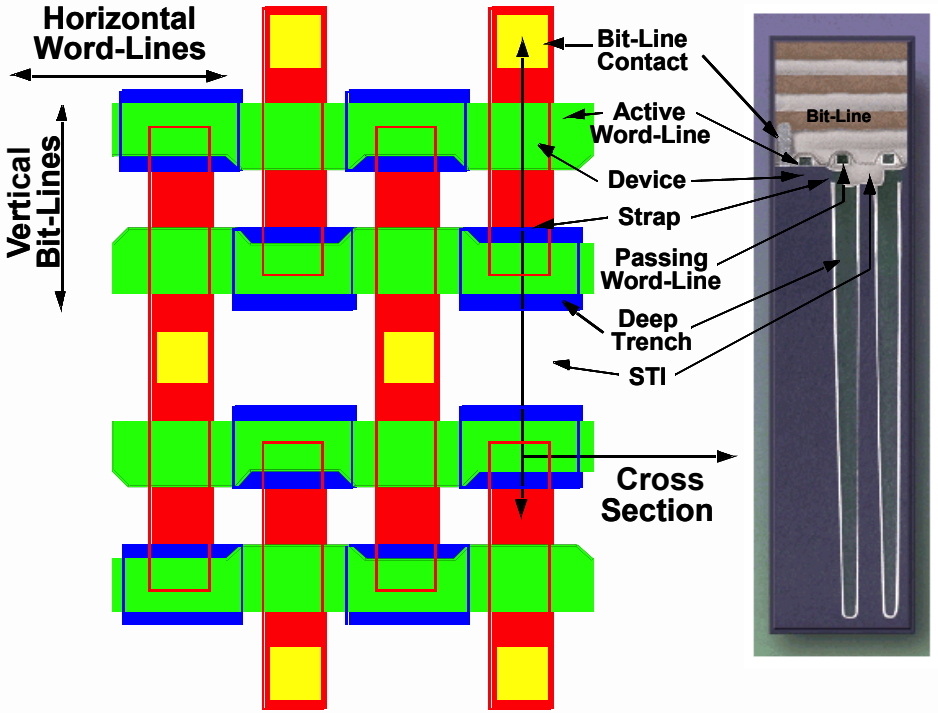


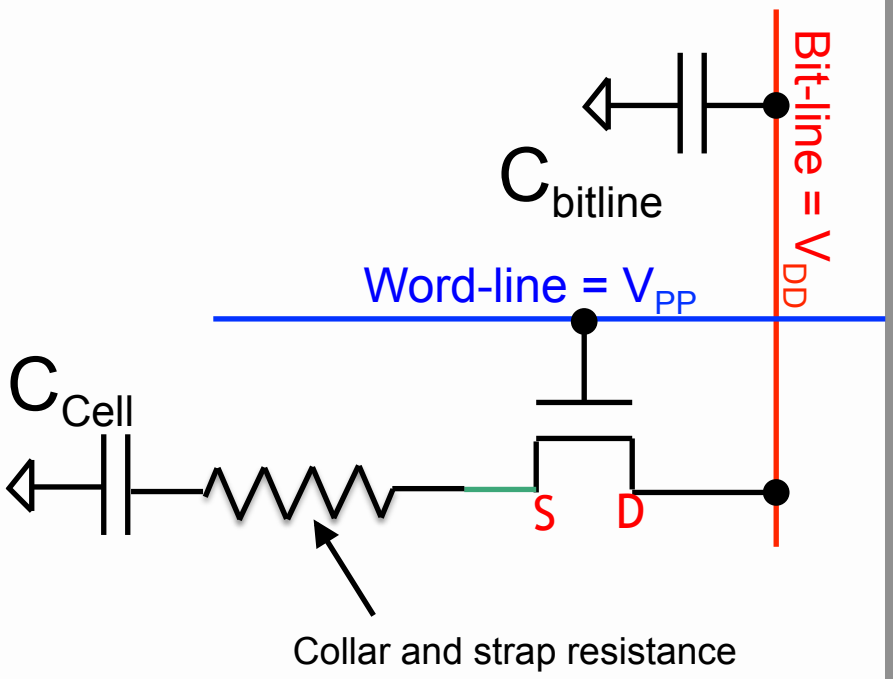


Vgs for pass transistor reduces as bitcell voltage rises, increasing Ron

Why there is a reduction in cell voltage after WL closes? Experiment

Reality





The node takes longer to charge than what we calculated analytically
Conclusions do not change:

- Increasing V_{PP} decreases the write time
- Cannot write a full V_{DD} in finite time

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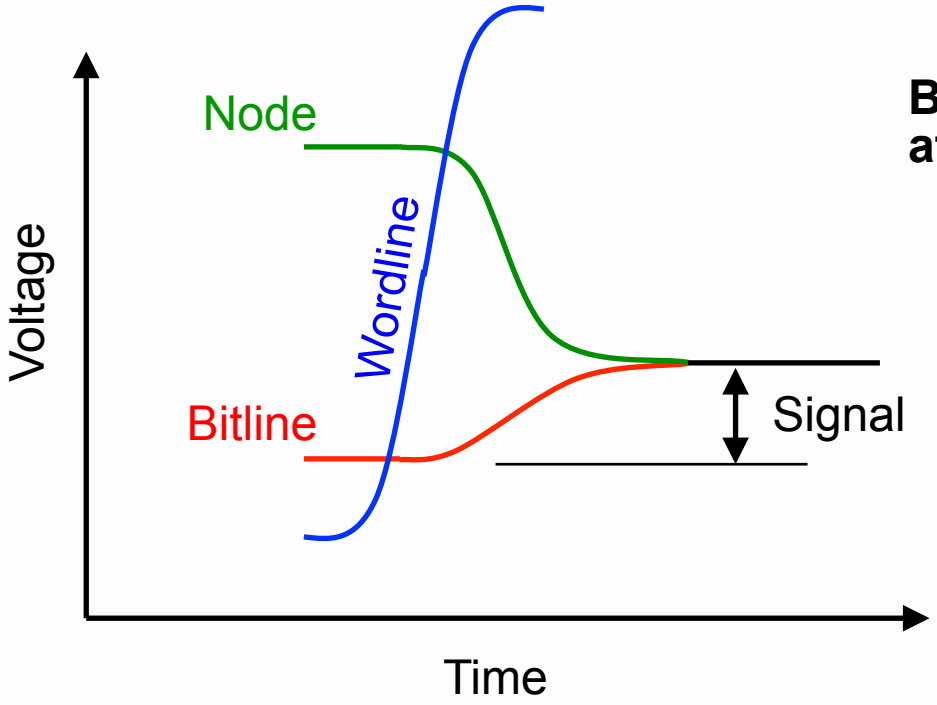
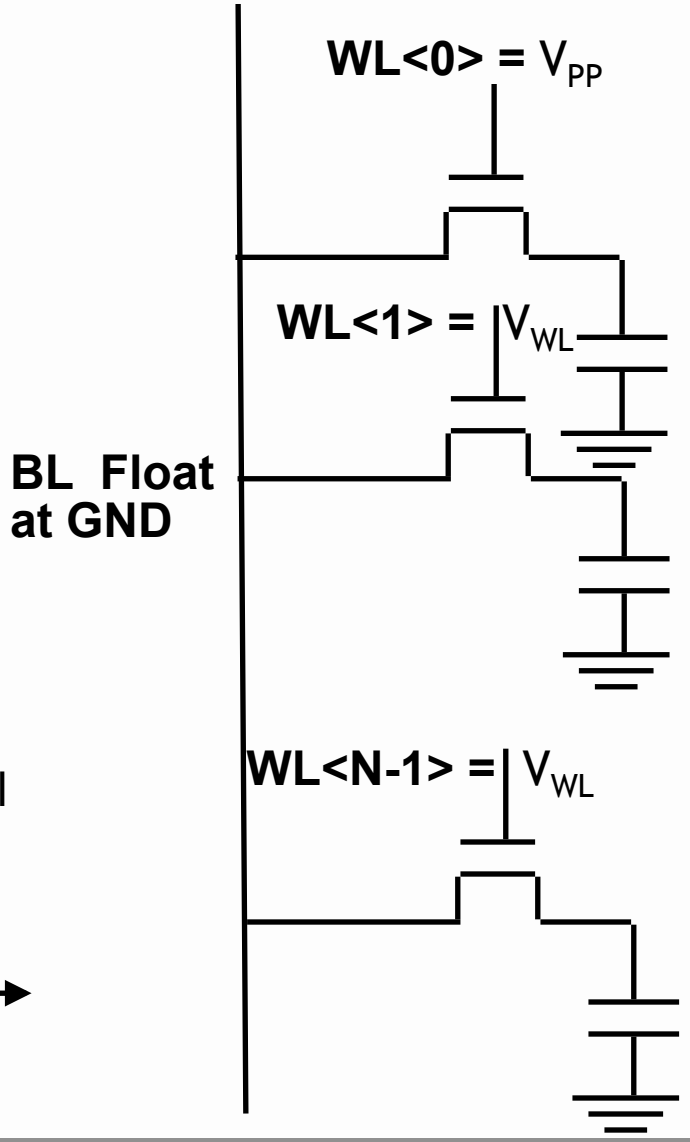
Signal: # WLs on a BL

Short BLs are Mandatory in DRAMs



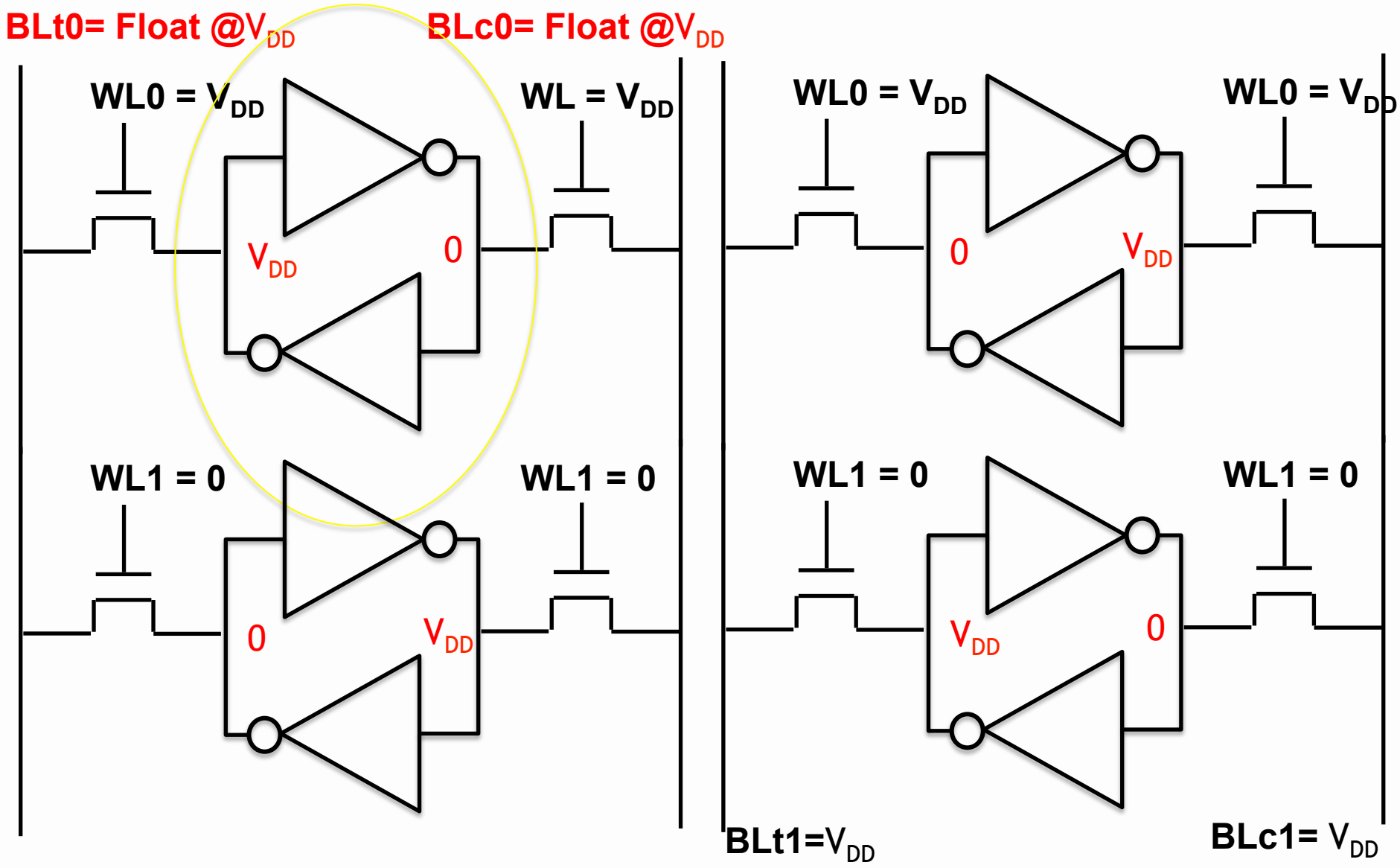


SRAM vs DRAM

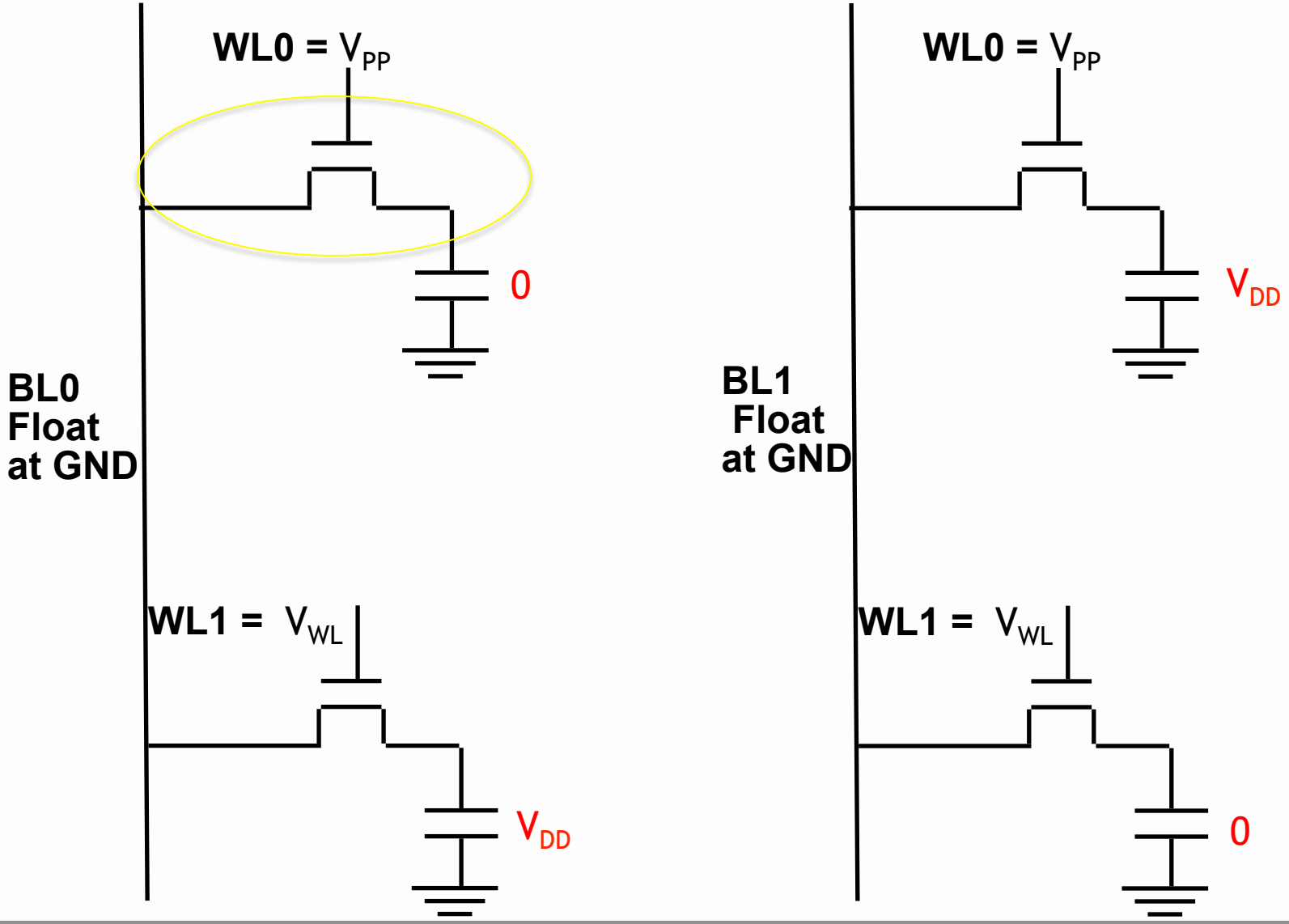
Assume a 1Mb memory with 512 WLs and 2048 BLs and 8 Columns. i.e. 256 DLs

	SRAM	DRAM
#WLs per BL	512	32
# BLs per DL	8	8
Sharing Sense Amps across columns	Yes	Possible?
Effective number of cells connected to a SA	4096	?
# Sense Amps	256	?

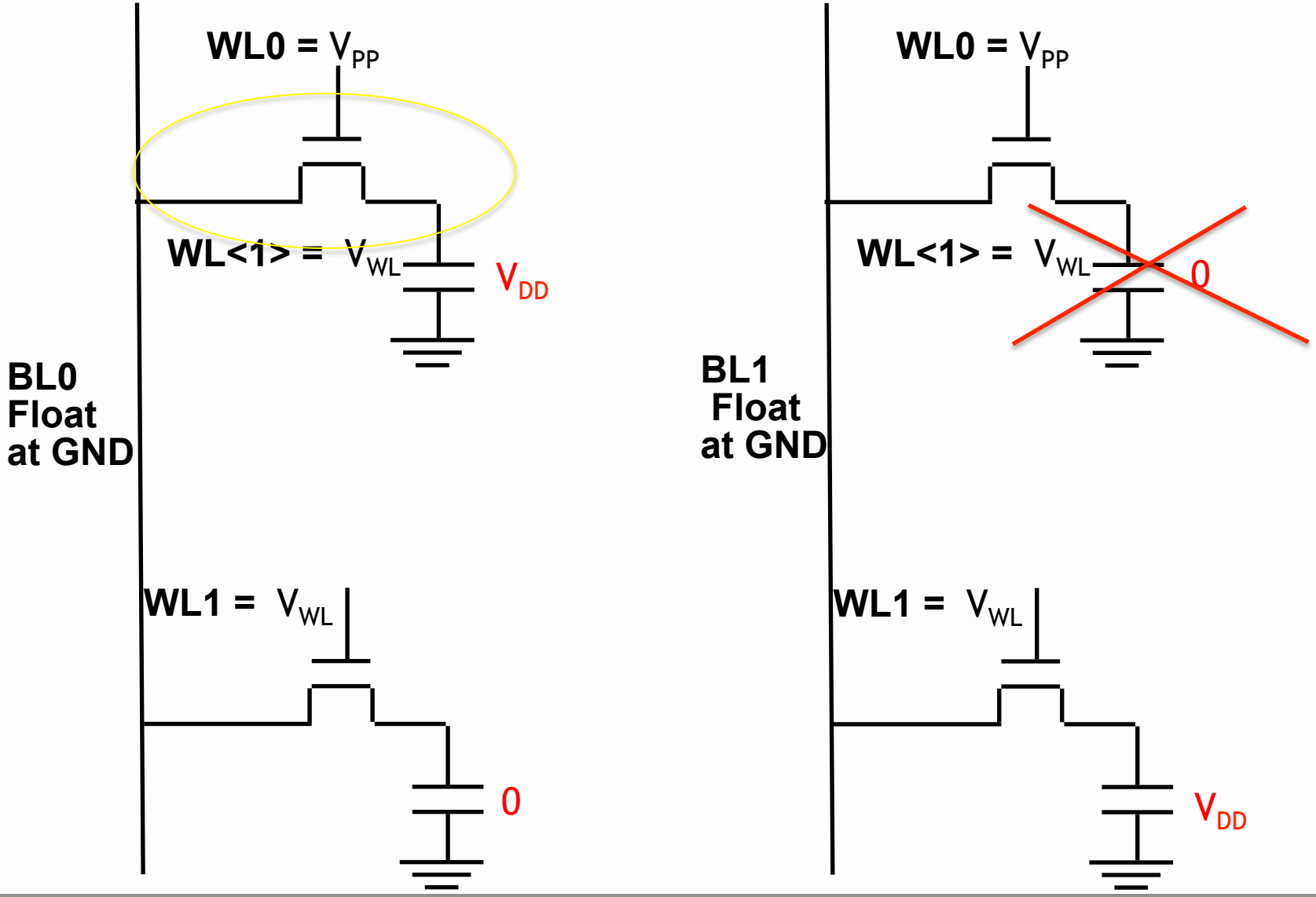
Half Select Condition - SRAM



Half Select Condition - eDRAM



Half Select Condition - eDRAM



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Extremely small SA

- **Number of transistors**
- **Sizes of transistors**

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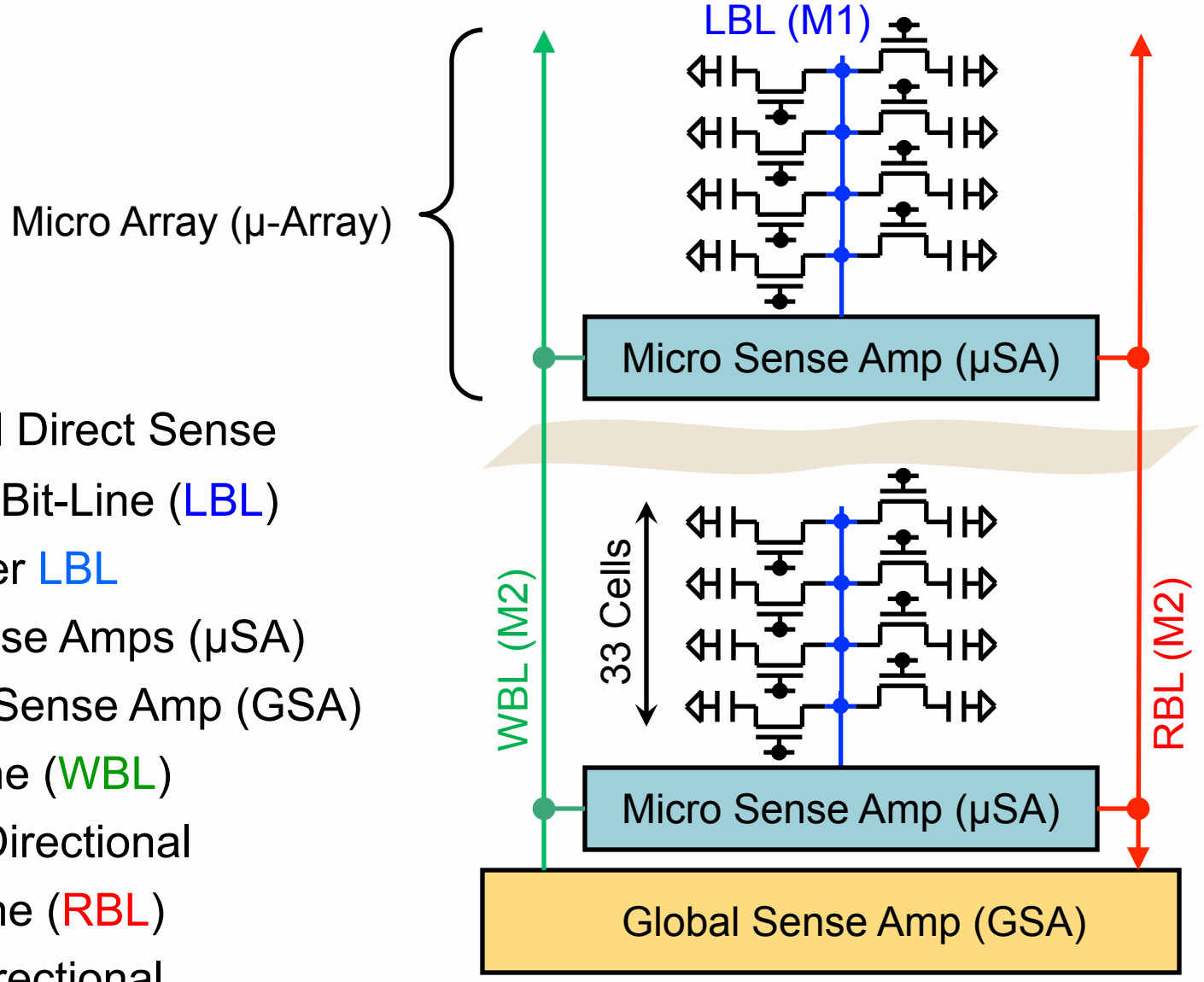
DRAM Operation Details (Case Study)

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 43, NO. 1, JANUARY 2008

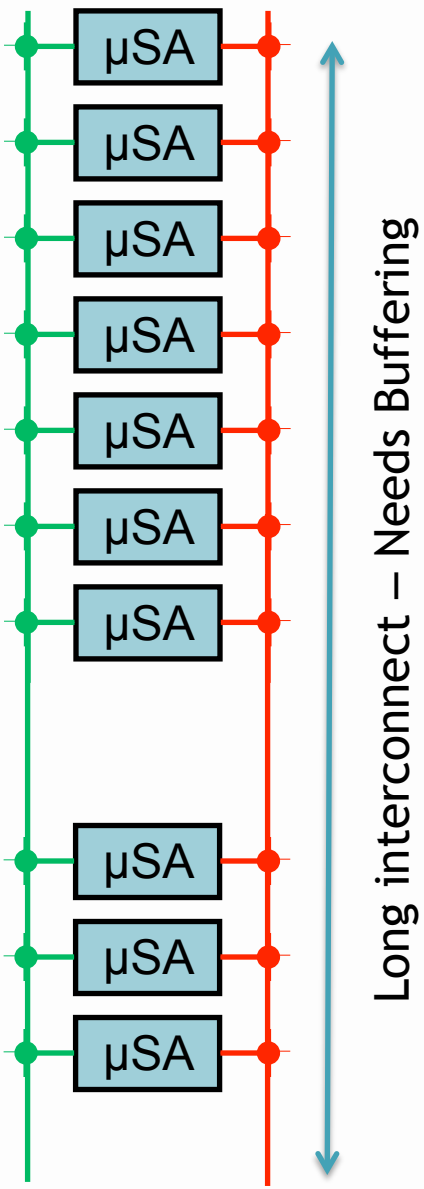
A 500 MHz Random Cycle, 1.5 ns Latency, SOI Embedded DRAM Macro Featuring a Three-Transistor Micro Sense Amplifier (John Barth/IBM)

Micro Sense Architecture

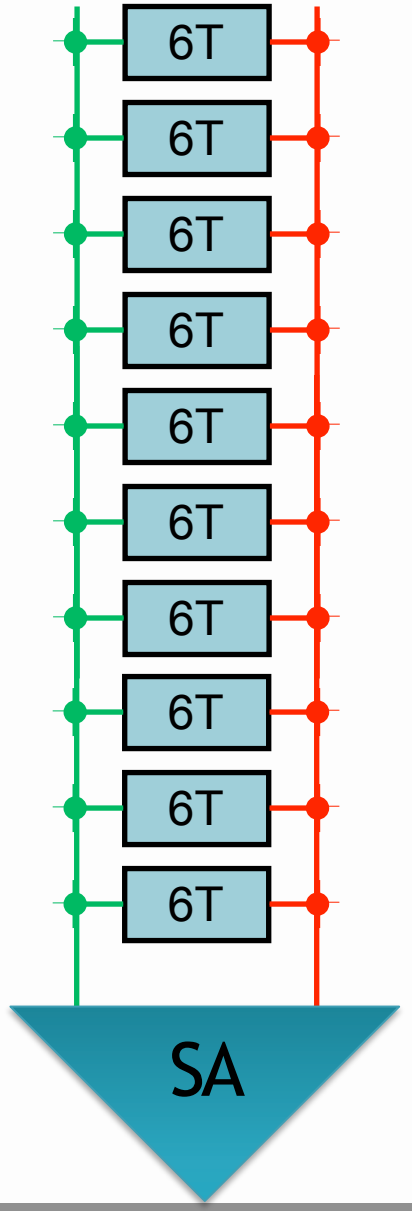


- Hierarchical Direct Sense
- Short Local Bit-Line (LBL)
  - 33 Cells per LBL
- 8 Micro Sense Amps (μSA)
  per Global Sense Amp (GSA)
- Write Bit-Line (WBL)
  Uni-Directional
- Read Bit-Line (RBL)
  Bi-Directional

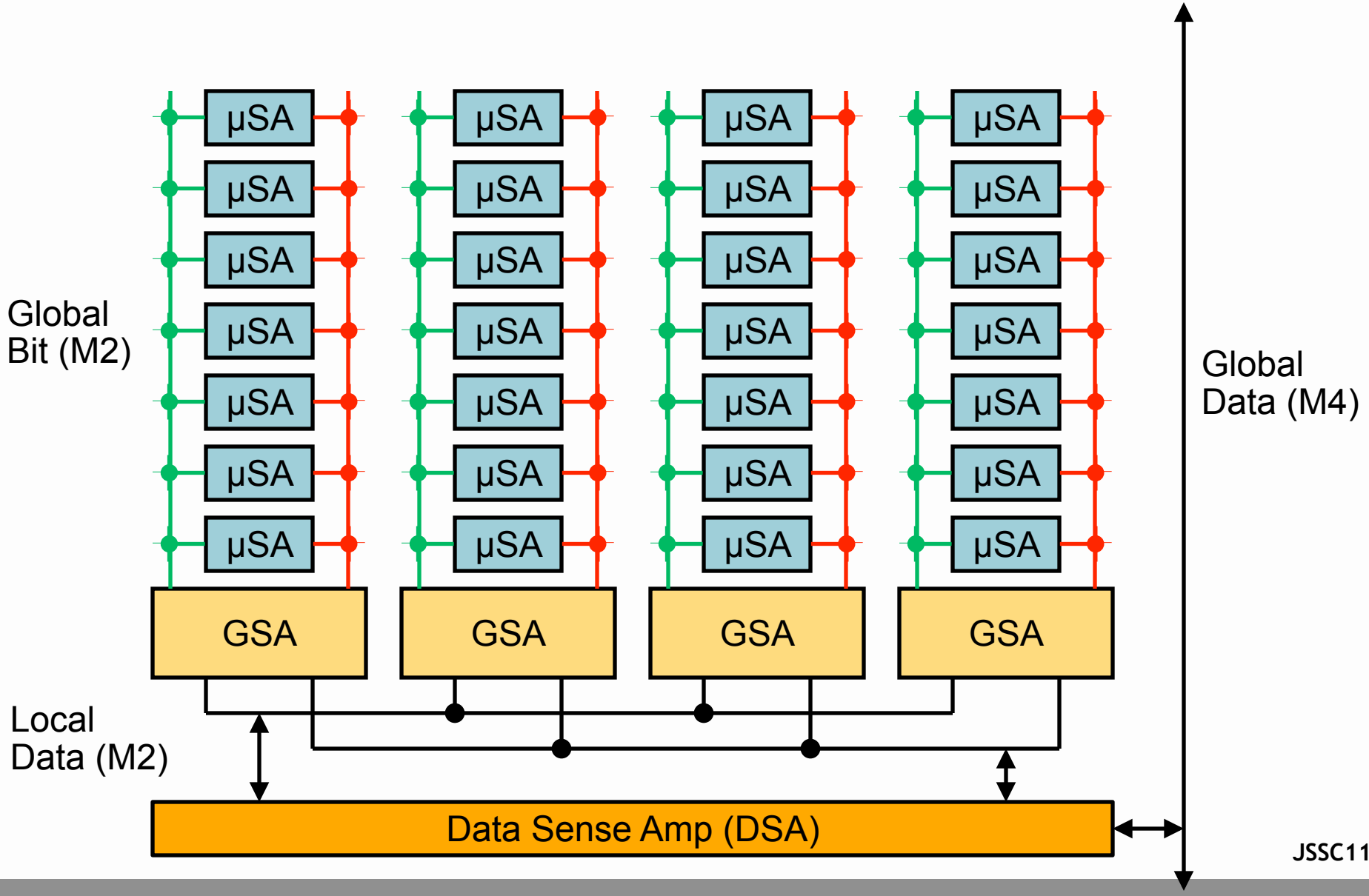
Sense Hierarchy - Motivation



Long interconnect – Needs Buffering



Micro Sense Hierarchy - Three levels



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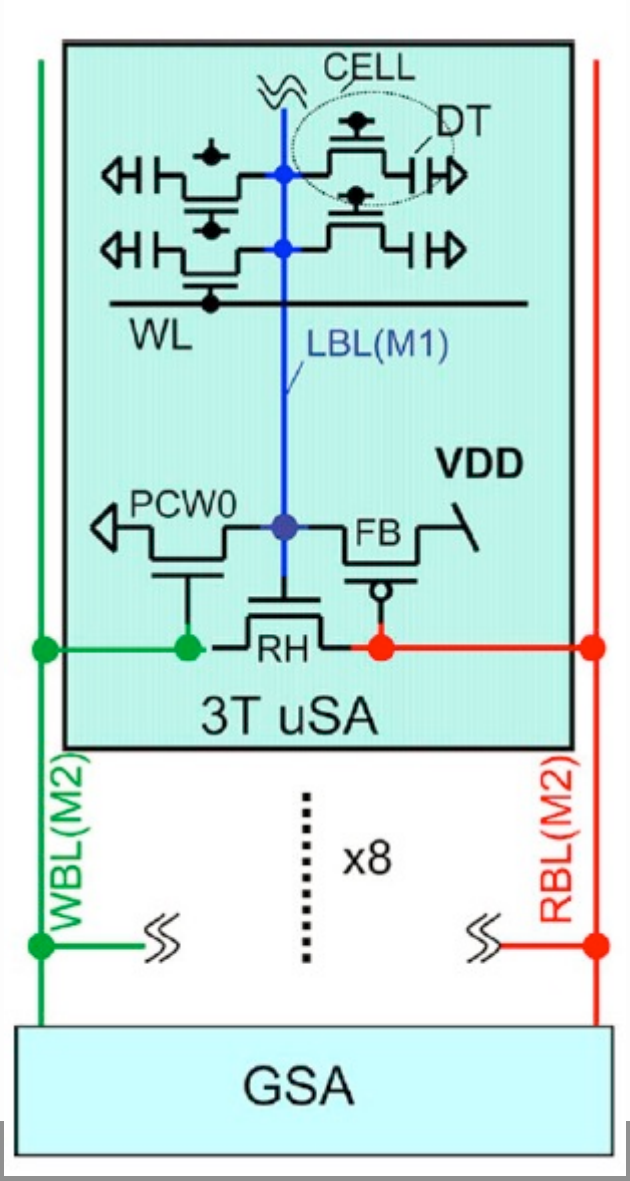
3T uSA operation



Pre-charge

WL is low. WBL and RBL both pre-charged to HIGH.
Next GSA drives WBL low. **LBL floats to GND level**

Read "0"

LBL remains LOW. RBL is HIGH. Sensed as a "0"

Read "1"

LBL is HIGH. Turns on RH, pulls RBL LOW.
+ feedback as pFET FB turns ON. Sensed as a "1"

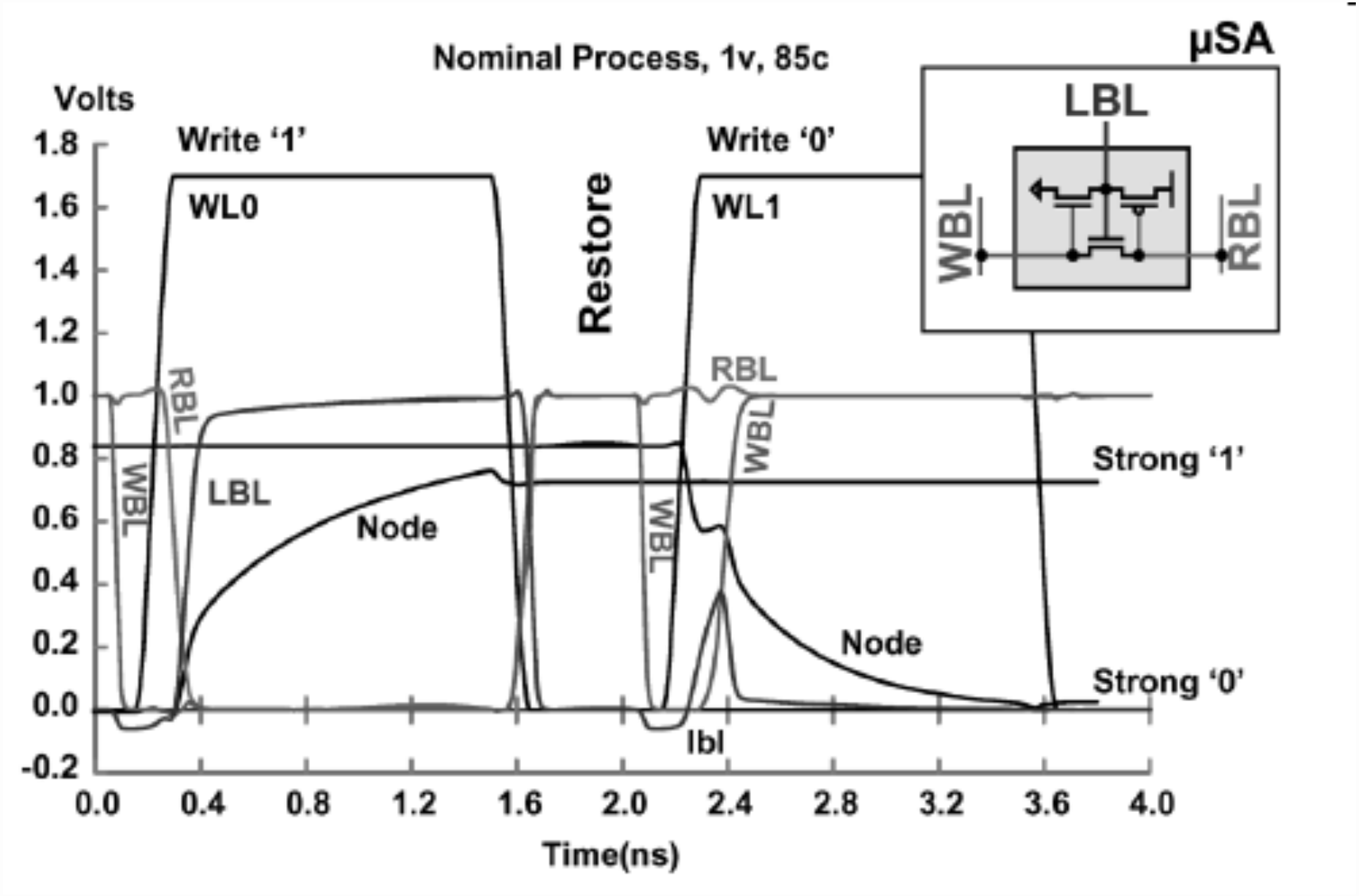
Write "1"

GSA pulls RBL to GND. FB pFET turns ON
Happens while WL rises (direct write)

Write "0"

WBL is HIGH, PCW0 ON. Clamps LBL to GND
As WL activates.

Simulations - Write



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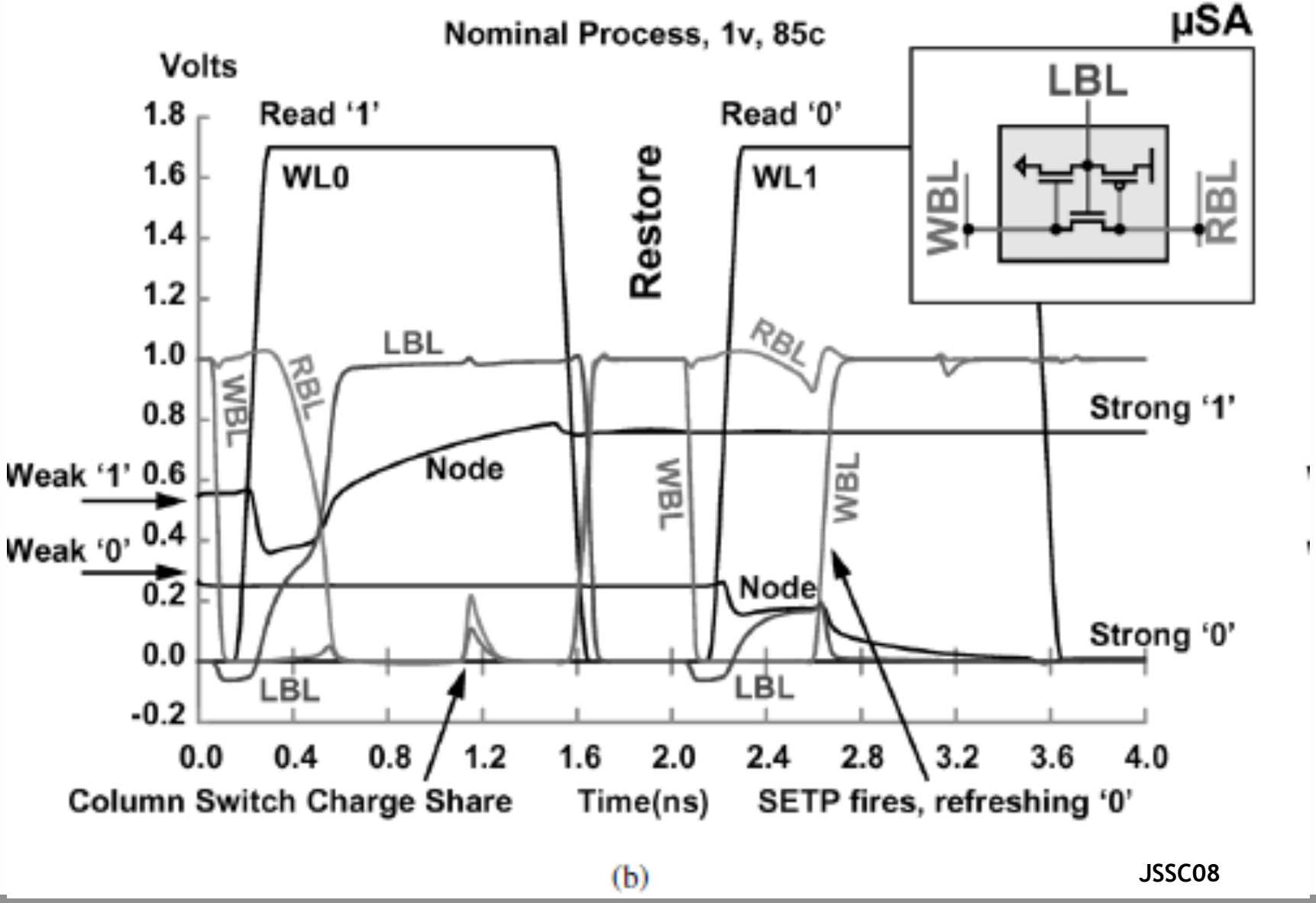
Simulations - Read



(b)

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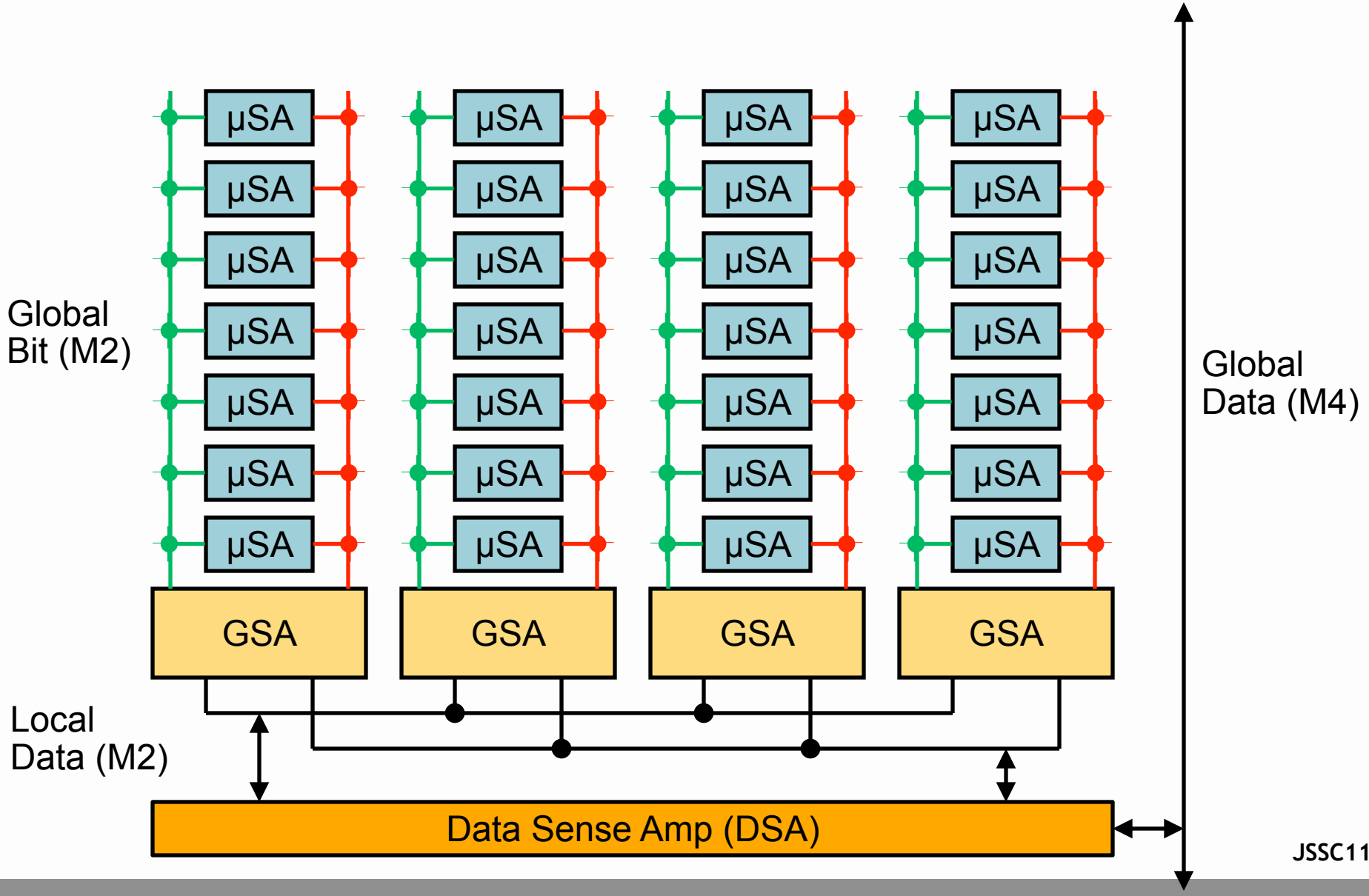
Micro Sense Hierarchy - Three levels



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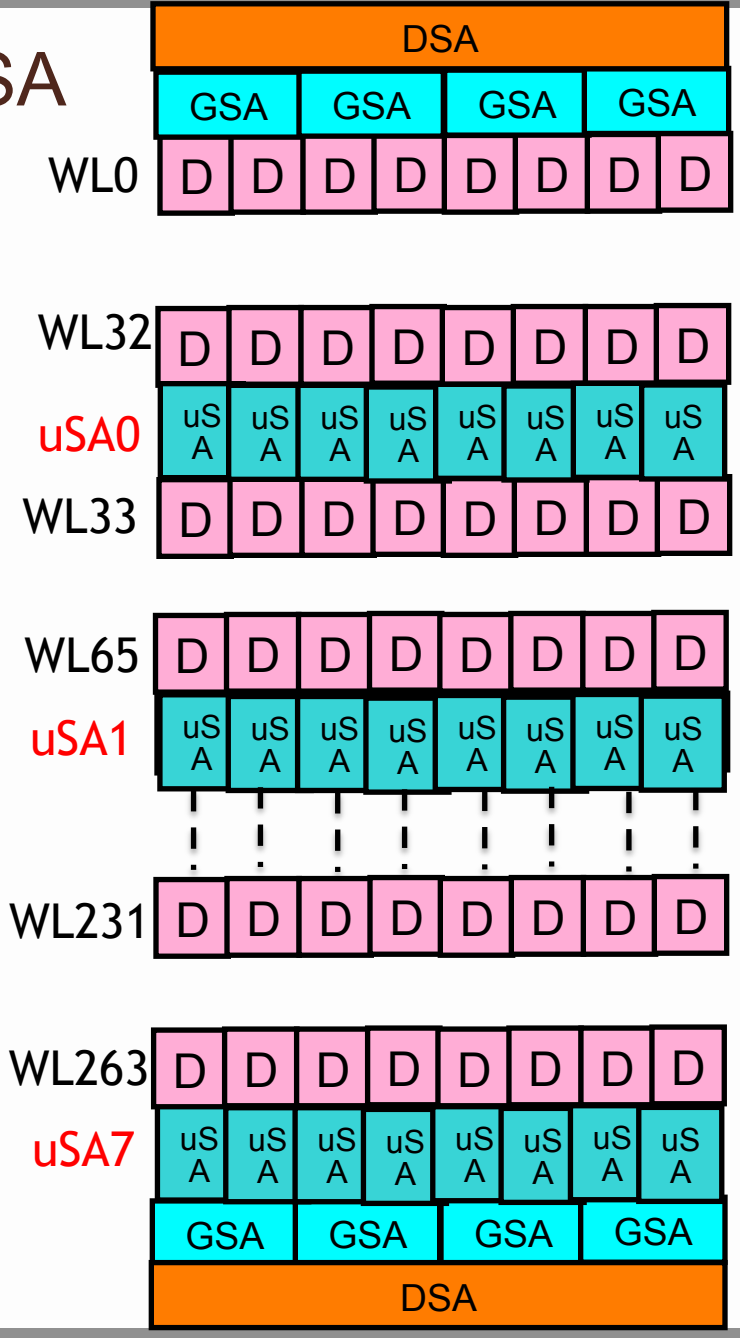
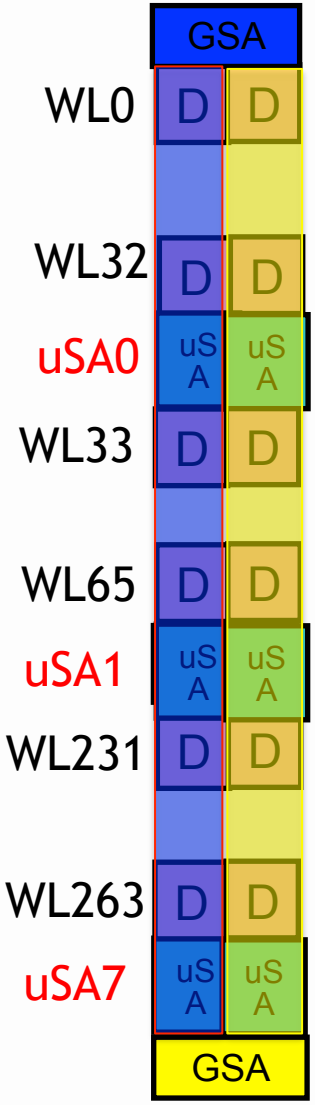
Layout Floor plan of Array+SA

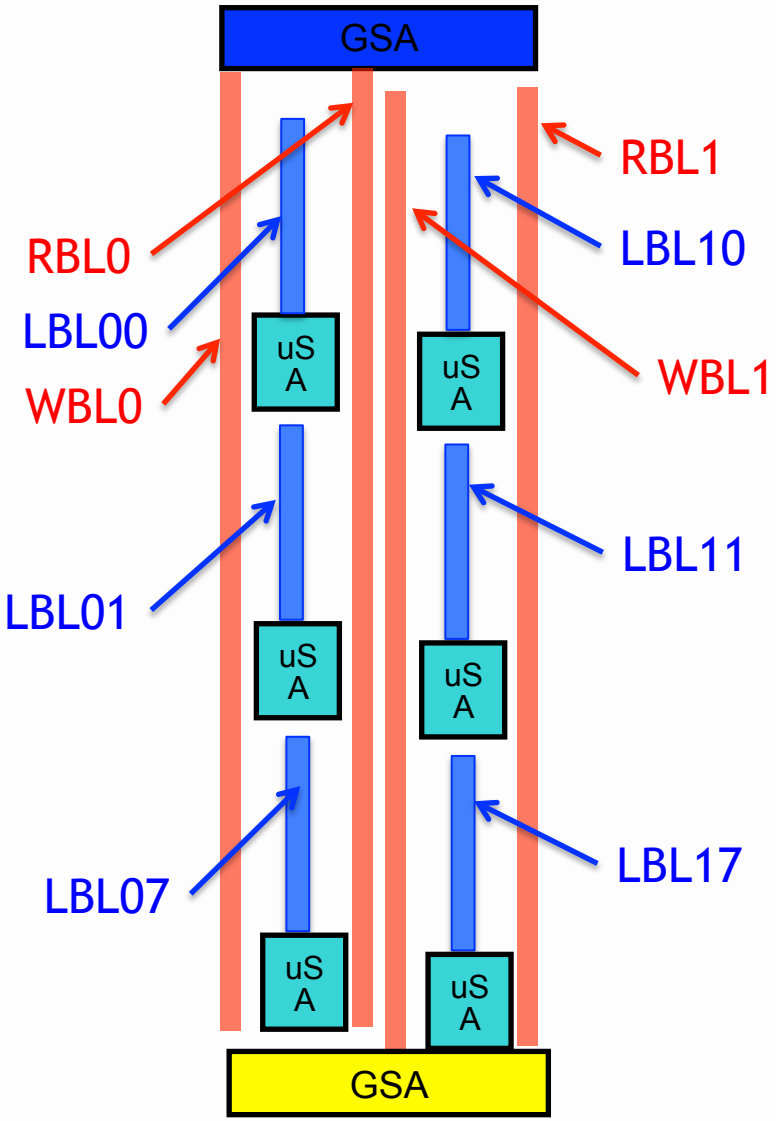
GSA Should fit into the bitcell width or n*bitcell width

Thus, distributed GSA on two sides of bitcell array

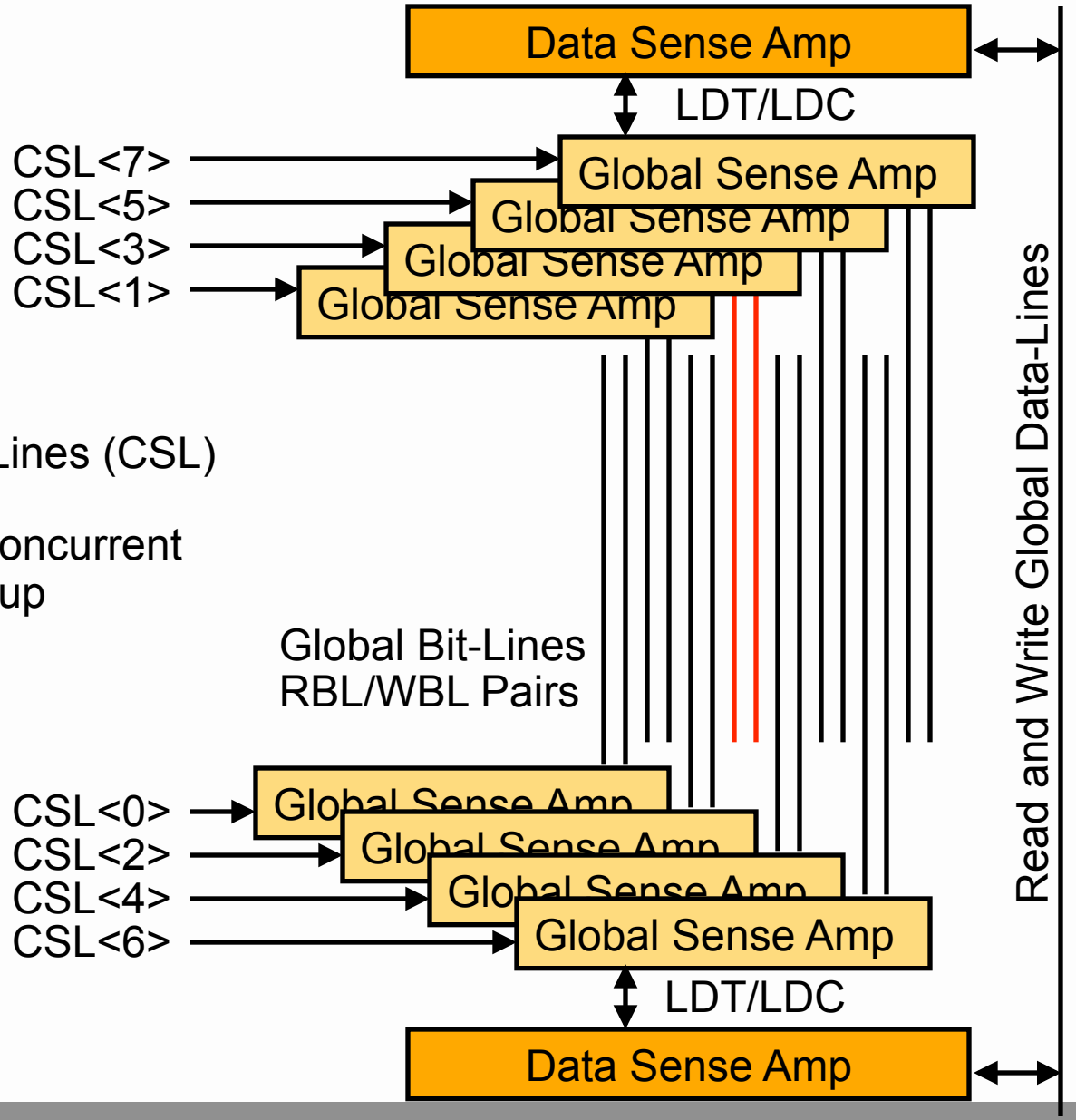


Layout Floor plan of Array+SA



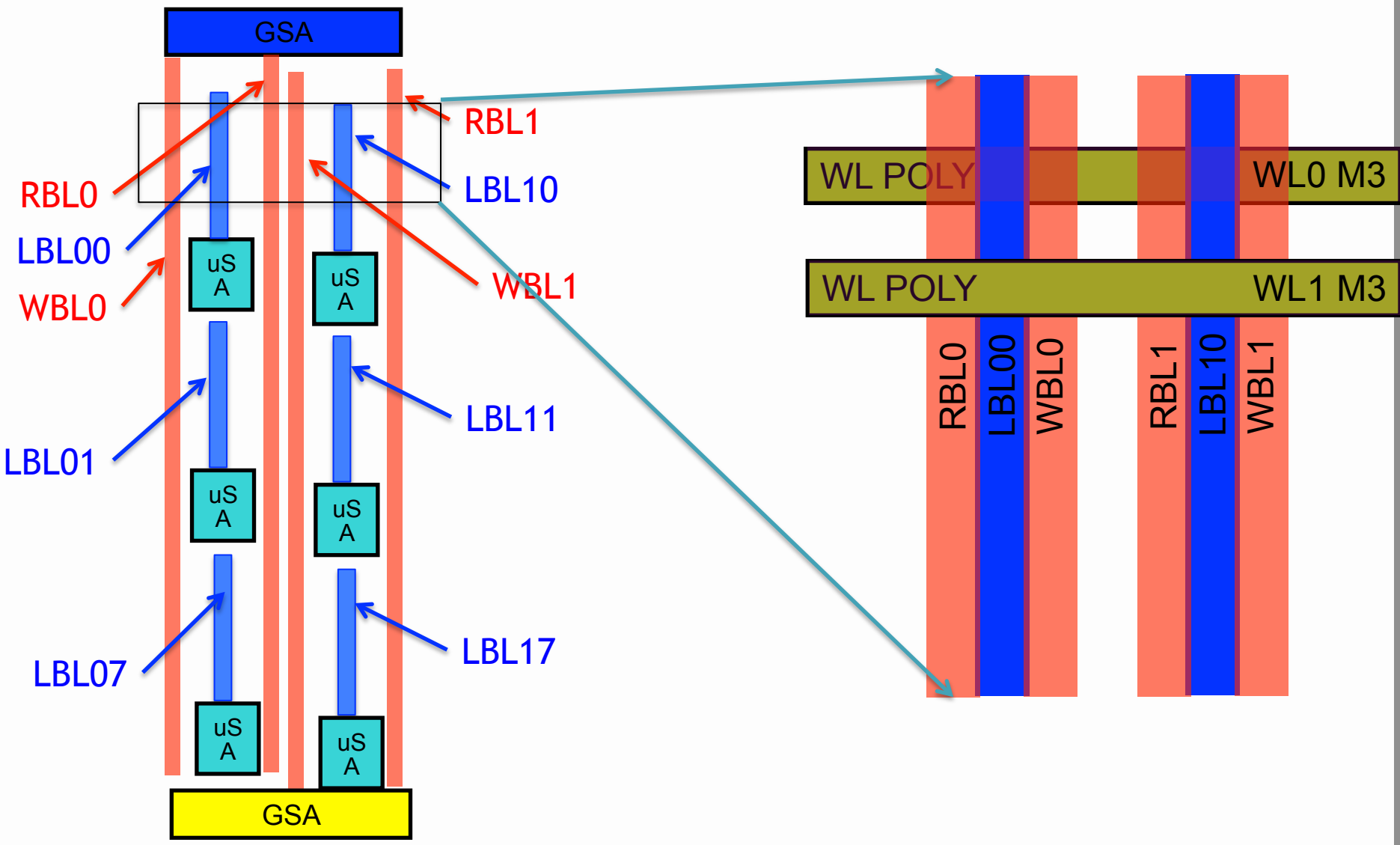


Column Interleave

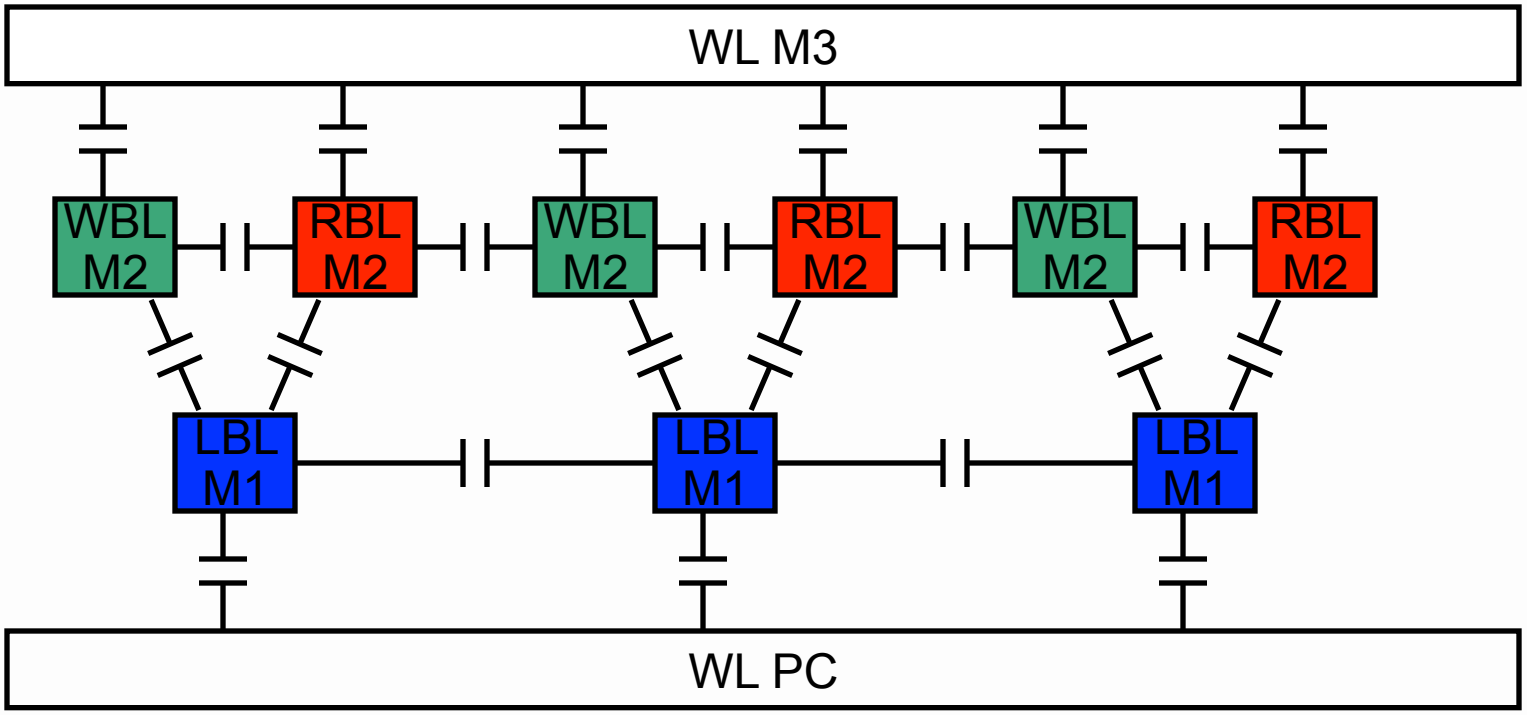


- 1 of 8 Column Select Lines (CSL)
- Fire Early for Write
- Fire Late to Support Concurrent Cache Directory Lookup

LAYOUT of array

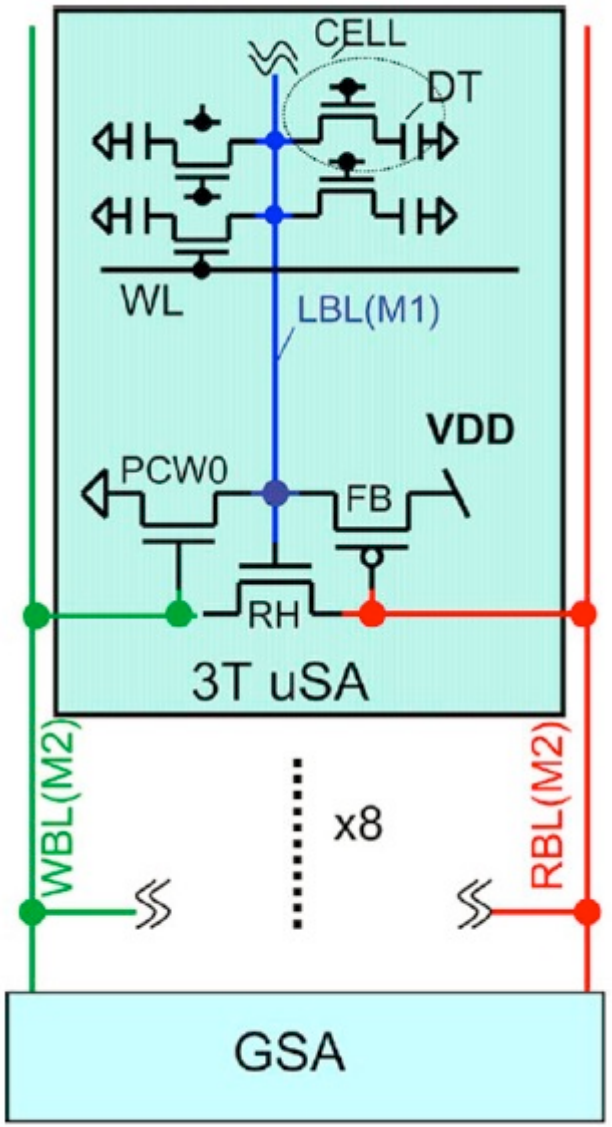


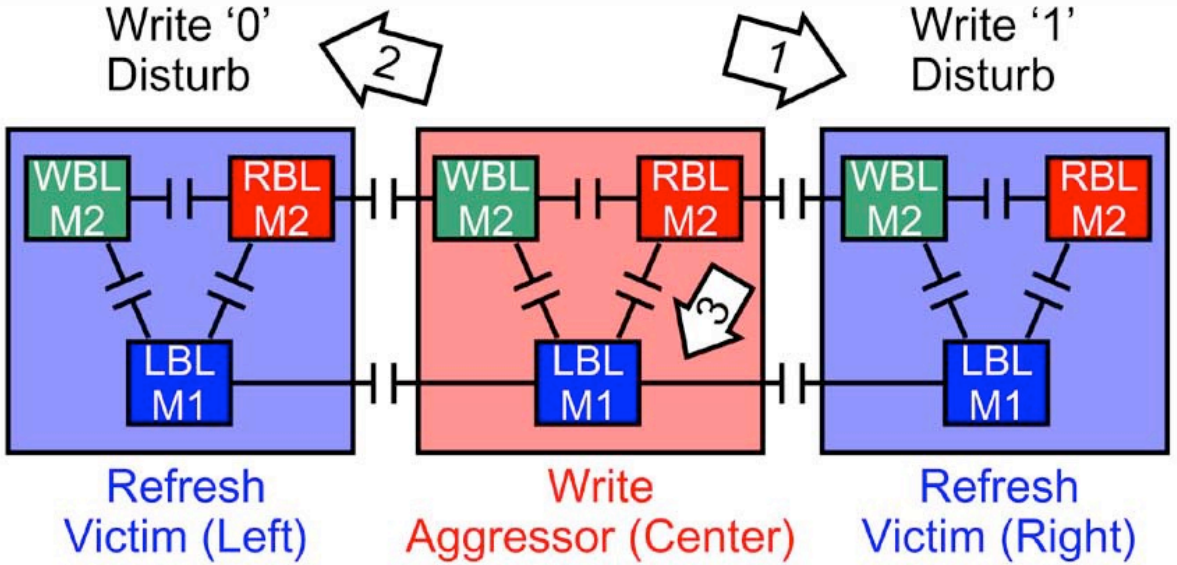
Micro Sense Local Bit-line Cross Section



Single Ended Sense – Twist not effective
Line to Line Coupling must be managed

Micro Sense Coupling Mechanisms





1. Write '1' Couples WBL below Ground
   Increasing RH leakage during Refresh '0'
2. Write '0' Couples RBL above VDD
   Delaying Feedback during Refresh '1'
3. Read '1' Couples Half-Selected LBL Below GND
   Increasing Array Device Sub-VT Leakage

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Half Selected LBL

- Accessing one of WL0-32
- Cell connected is on LBL00
- LBL01-07 – Half Selected LBLs