Variation Characterization

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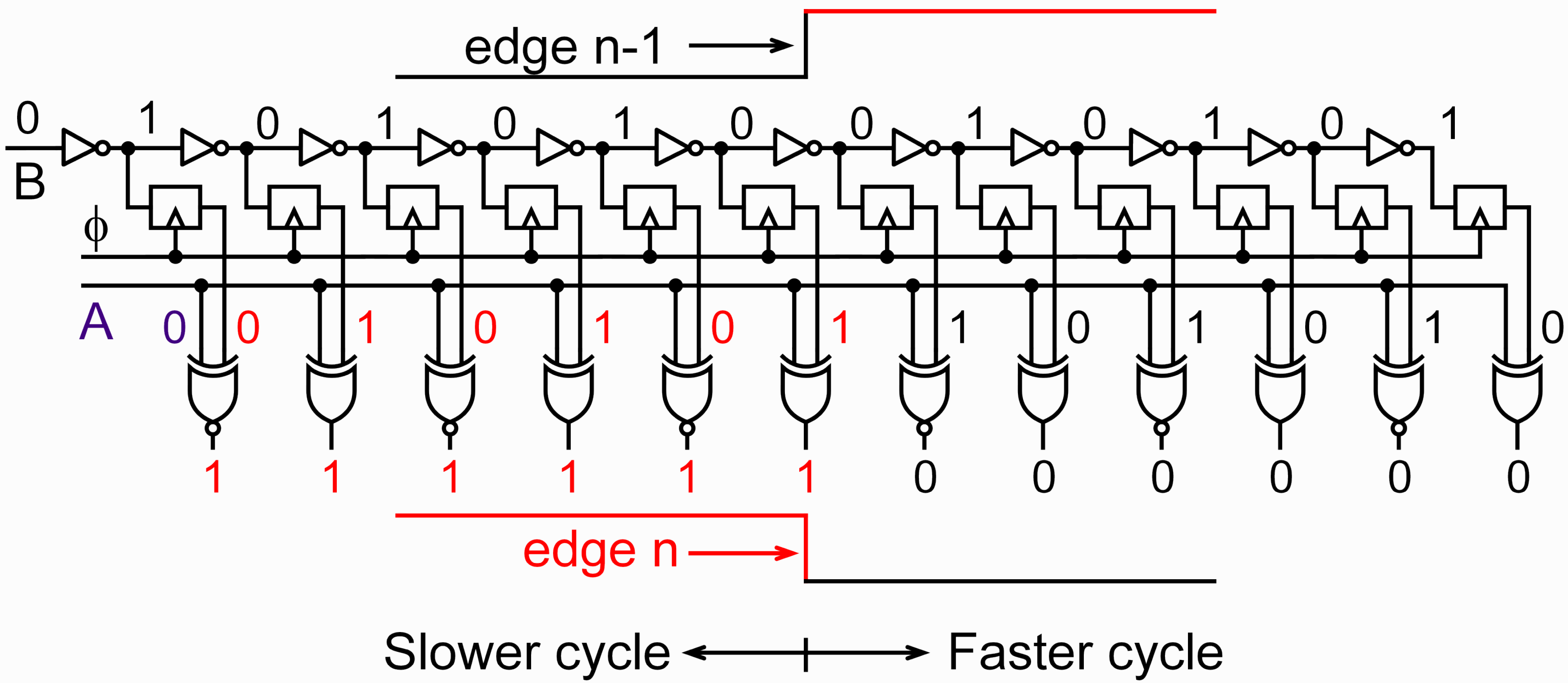
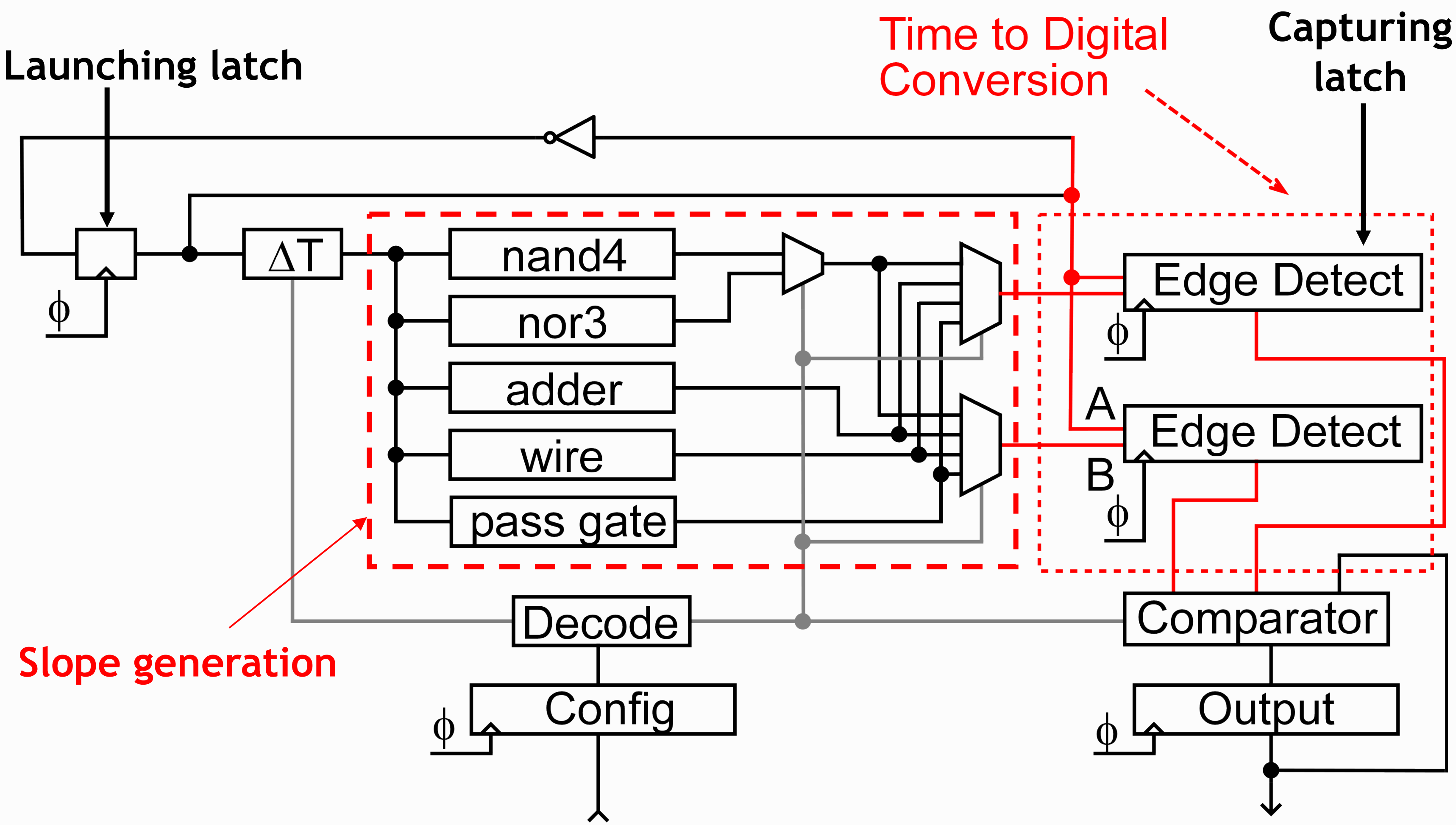
Time-to-Digital Conversion Using an Edge Detector



Delay based Sensing - Critical Path Monitor (CPM)



A. Drake et. al. ISSCC 2007

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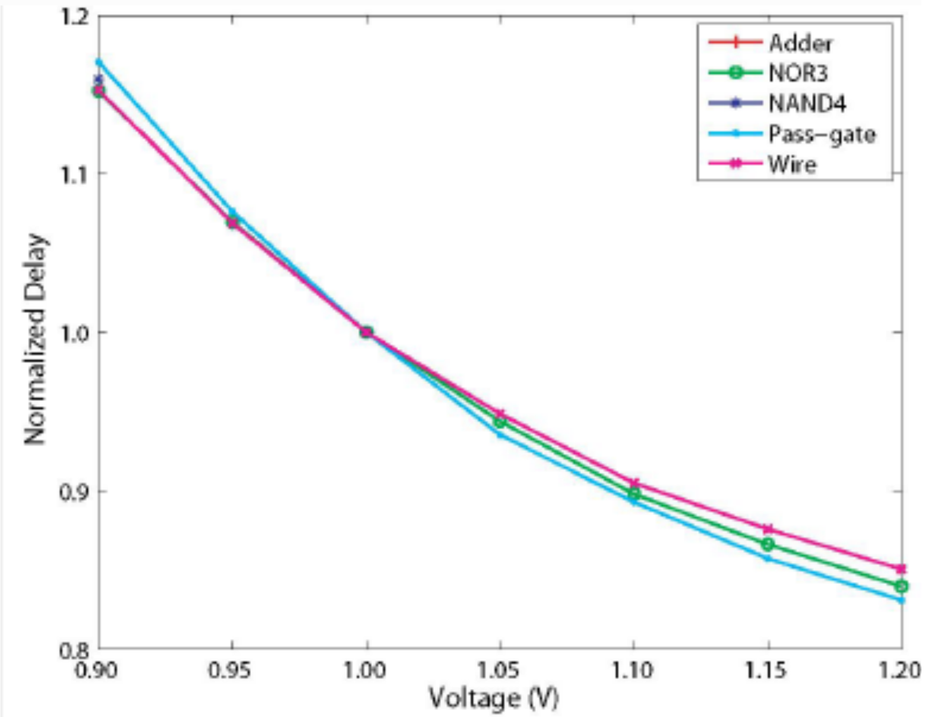
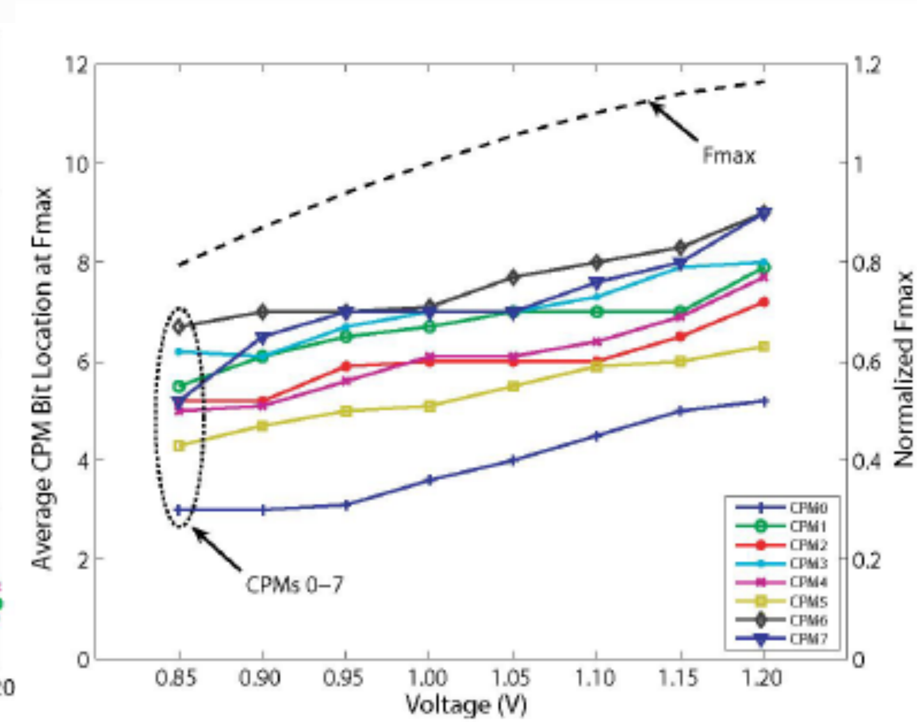


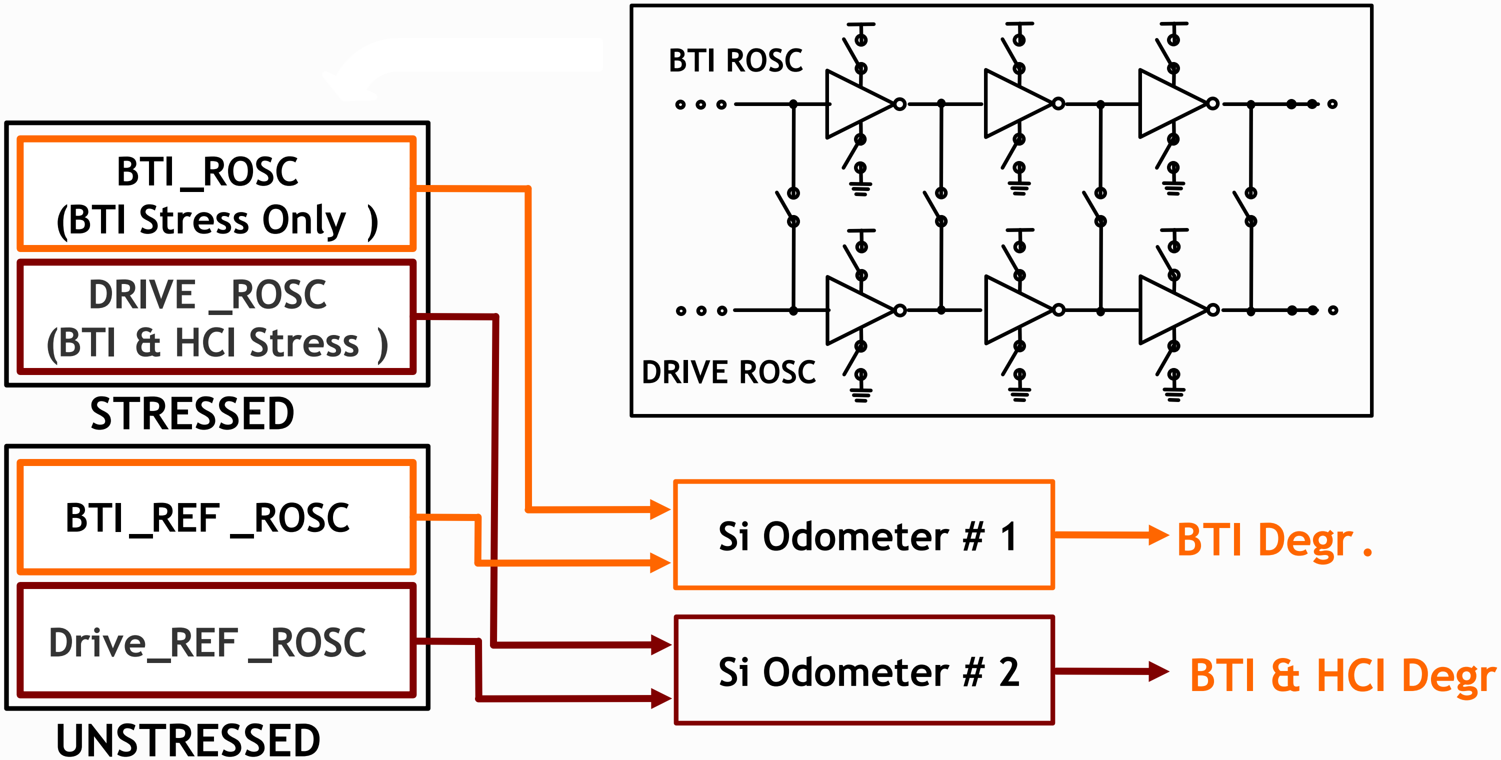


A. Drake et. al. ISSCC 2007

Characterizing Bias Temperature Instability

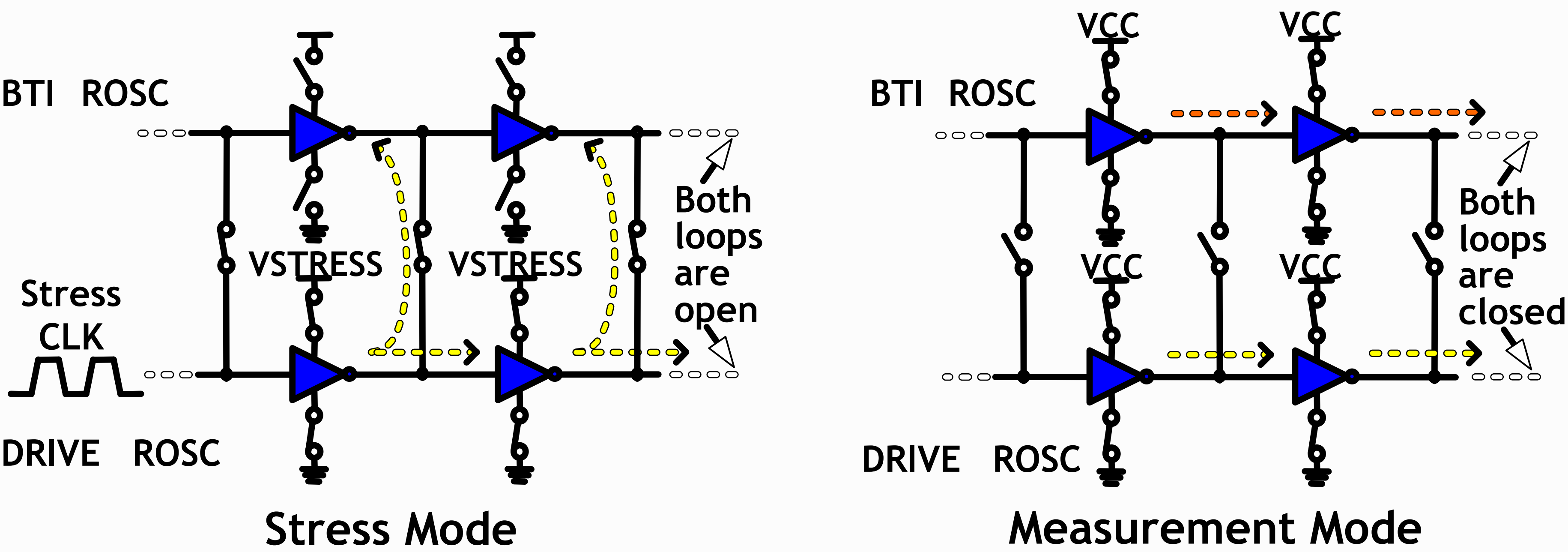
- Challenge
  - Characterize the extent of V_{TH} shift due to aging
  - Isolate the contributions of NBTI vs. PBTI while minimizing noise due to other effects (hot carrier effects, device breakdown)
  - Rapid post-stress measurement (or during stress measurement) to prevent recovery
- Methods
  - I-V measurement of devices using stress pulses
  - Delay (Oscillator Frequency) based measurement

All-in-One Silicon Odometer



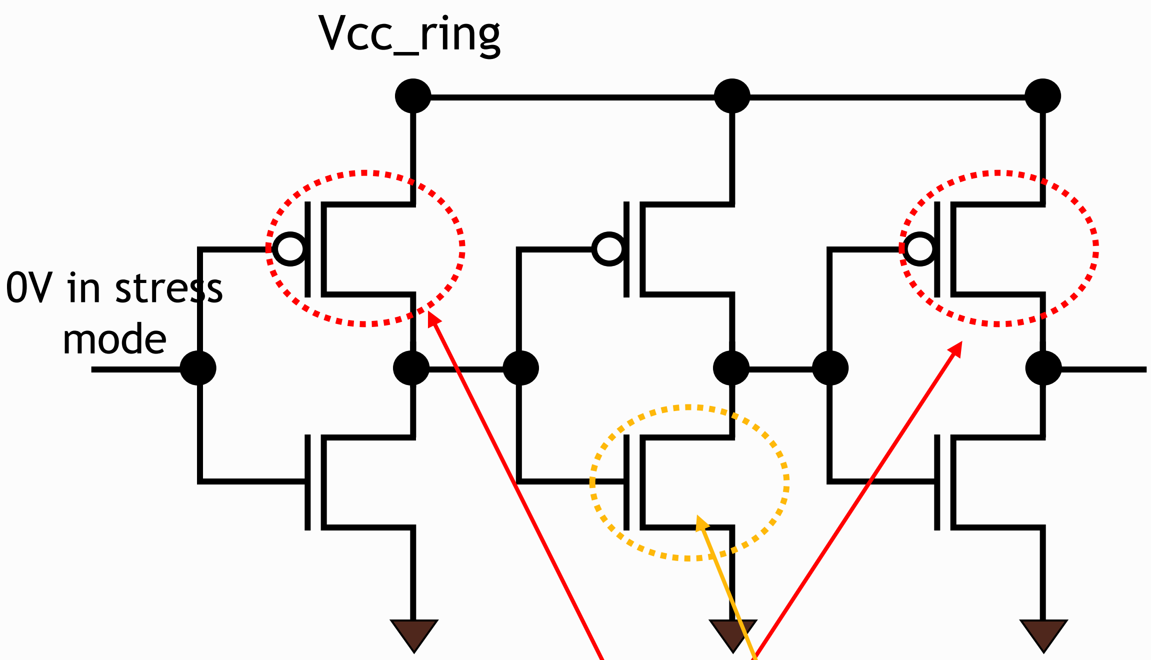
- Isolates BTI, HCI and TDDB effects
- 4 ROSCs : 2 stressed, and 2 unstressed
  - BTI_ROSC degrades due to BTI only; "DRIVE" ROSC ages due to BTI & HCI
- Frequency degradation measured with beat frequency detection circuits

BackDrive Configuration



- <u>Stress Mode</u> (ROSC loops opened)
  - BTI_ROSC gated off, DRIVE_ROSC drives transitions; I/P driven by VCO
- <u>Measurement Mode</u> (ROSC loops closed)
  - Both ROSCs connected to the power supply @ VCC, switches between them are opened

Ring Oscillator Based Circuit



In Stress Mode:
Vcc_ring and/or temperature are raised.
Primary input = 0

In Measurement Mode:
Vcc_ring and/or temperature brought back to normal condition

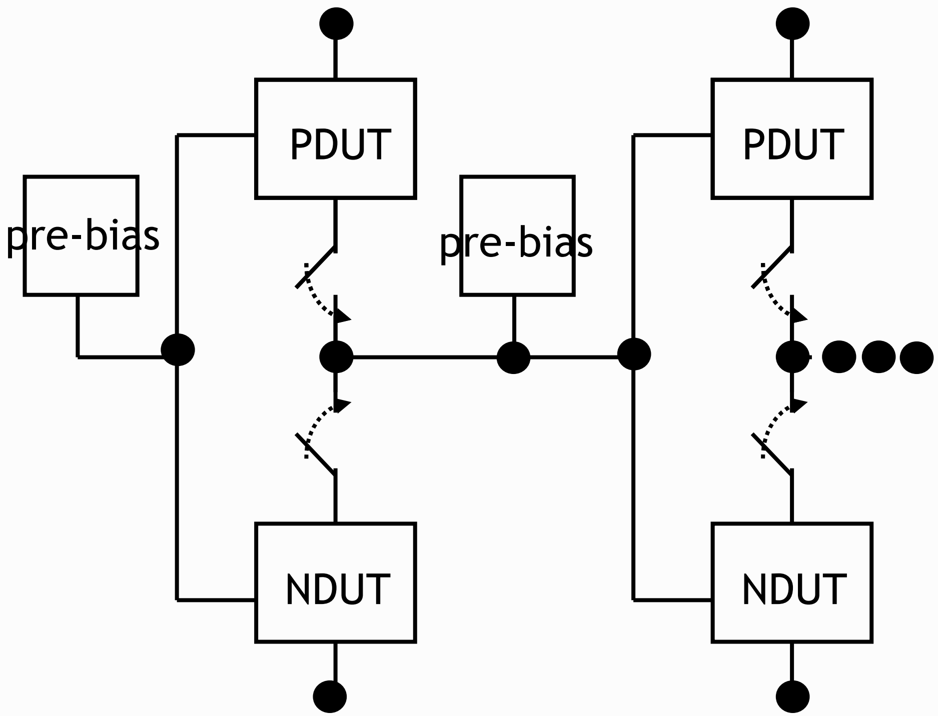
PMOS with 0V input (with **RED Circle** in the figure) is stressed.

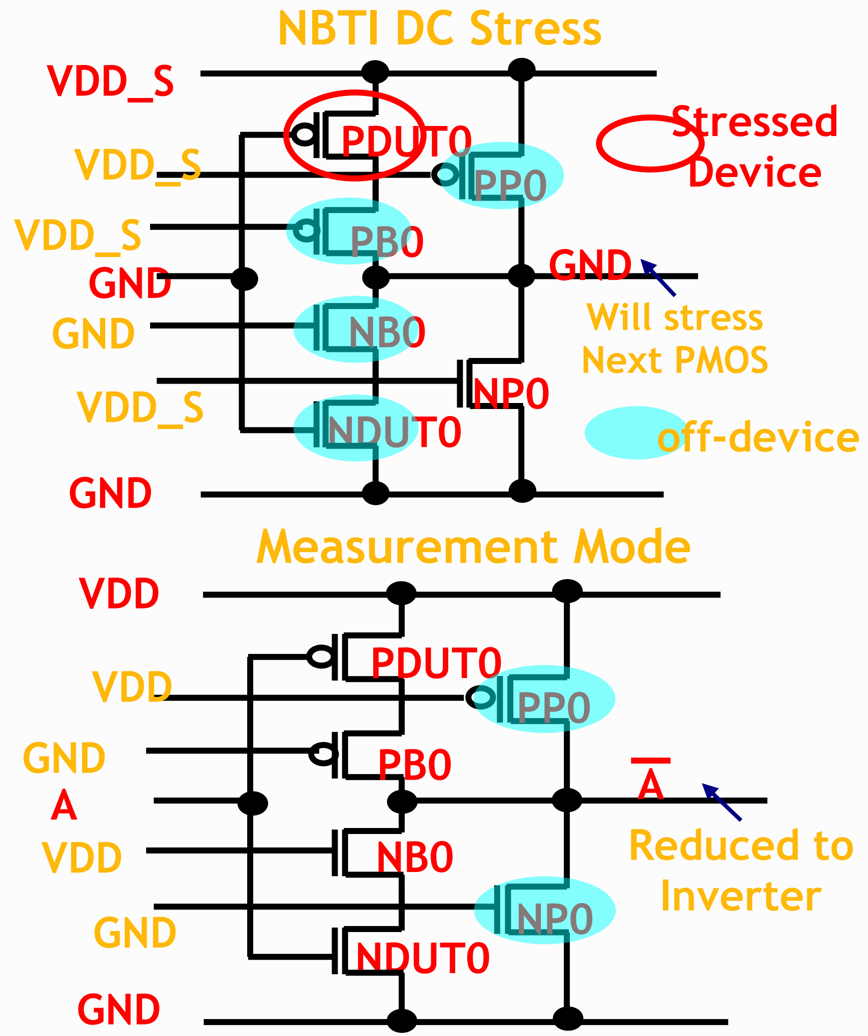
Measure the frequency difference between **stressed** case and **unstressed** case

Impossible to isolate the effect from each of NBTI and PBTI

Unified NBTI - PBTI Sensor

Objective: Maintain the simplicity of RSC style monitoring circuit, while isolating NBTI and PBTI

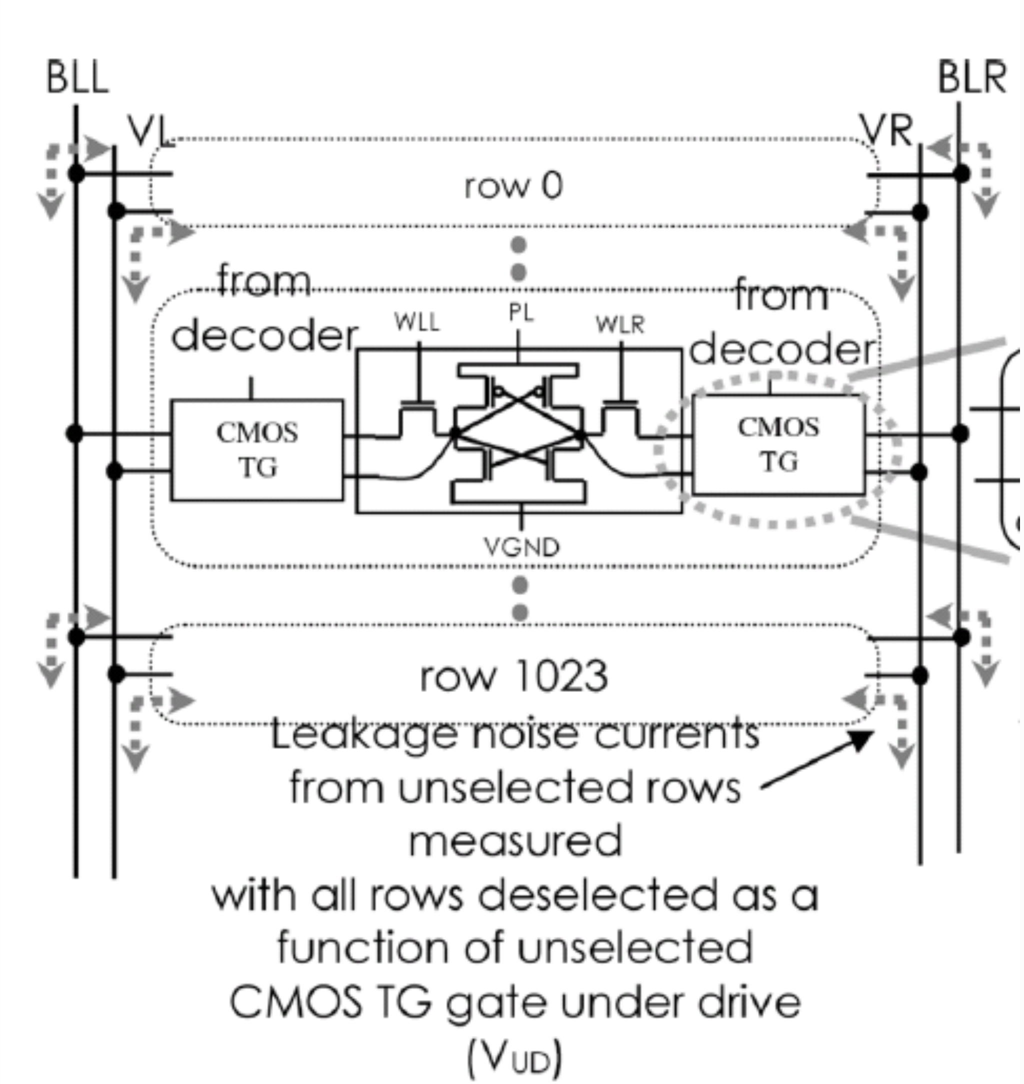


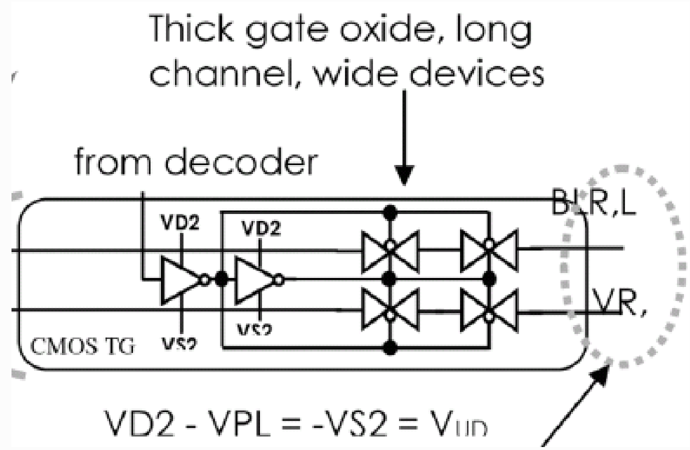


Can we directly characterize more complex circuit properties ?

- Read and Write margin of SRAM
  - Depends on both local variation and global variations
  - Individual device characterization can help but direct characterization of read/write margin can provide better information
- Temperature
  - Using Delay
  - Using Leakage
- Power

SRAM Fluctuation Monitor



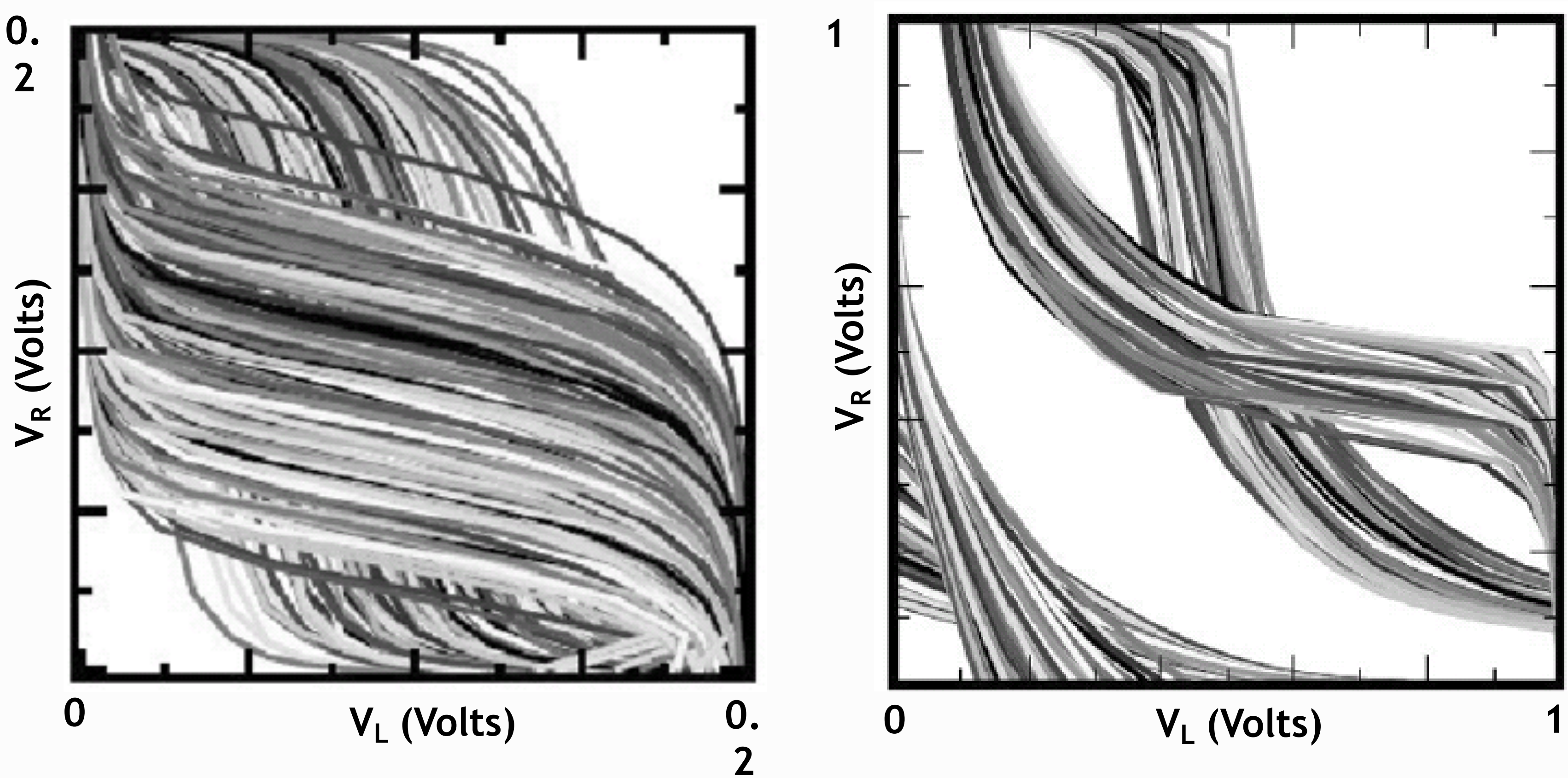


For unselected cells, under-drive pass gates to reduce leakage noise

For selected cell, overdrive pass gate to minimize ON resistance

A. Bhavnagarawala, et. al, JSSCC 2008

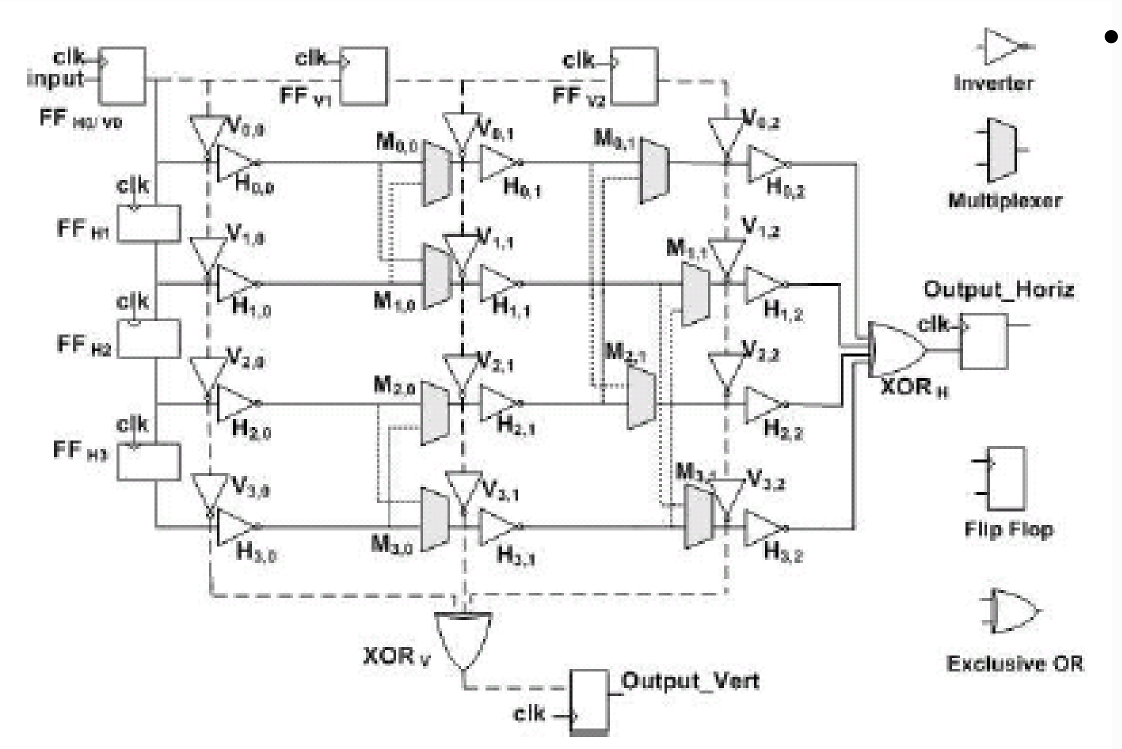
SRAM Fluctuation Monitor



Voltage Transfer Characteristics (measured) for 1k cells for different supply voltages

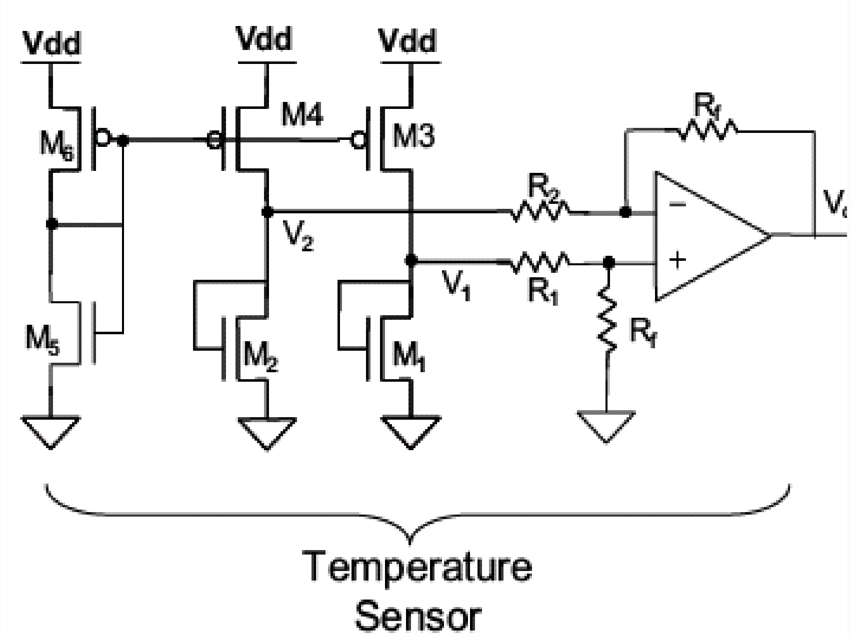
A. Bhavnagarawala, et. al, JSSC 2008

Sensing Temperature Through Delay



- **Delay increases with Temperature**
  - **Matrix structure of gates with multiplexers that enable activation of any path (using scan-chain controls)**
  - **Adjust clock frequency to detect path-delay (temperature)**

Sensing Temperature Through Leakage



Leakage is exponential function of temperature

(Make devices large to eliminate RDF, LER effects)

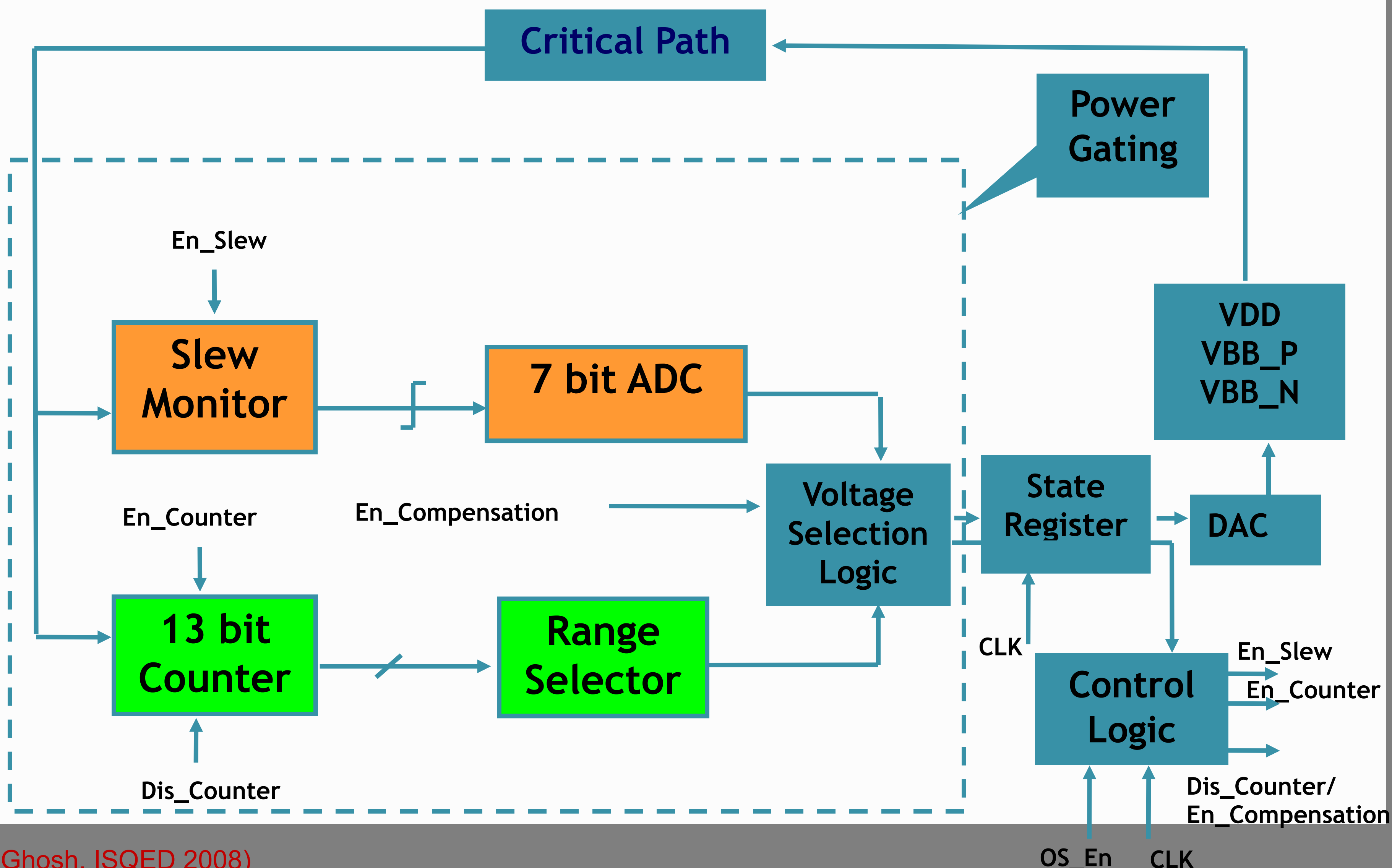
Voltage effects cancelled out

$$V_{out} = \frac{R_f}{R_1}\sqrt[\alpha]{\frac{L}{\mu C_{ox}}}\left(\sqrt[\alpha]{\frac{I_1}{W_1}} - \sqrt[\alpha]{\frac{I_2}{W_2}}\right)$$

M. Mesut, et. al, JSSC 2005

Variation Adaptation

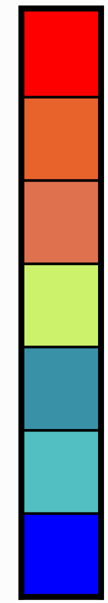
Block diagram of Detection and Compensation System



(A. Ghosh, ISQED 2008)

Adaptive Body-biasing Based on Delay and Rise/Fall Slew Difference

		$\Delta t_{R\text{-}F} > \Delta t_{R\text{-}Fnom}$	$\Delta t_{R\text{-}F} = \Delta t_{R\text{-}Fnom}$	$\Delta t_{R\text{-}F} < \Delta t_{R\text{-}Fnom}$
$f > f_{nom}$	NMOS	LRBB	RBB	SRBB
	PMOS	SRBB	RBB	LRBB
$f = f_{nom}$	NMOS	RBB	No bias	FBB
	PMOS	FBB	No bias	RBB
$f < f_{nom}$	NMOS	SFBB	FBB	LFBB
	PMOS	LFBB	FBB	SFBB

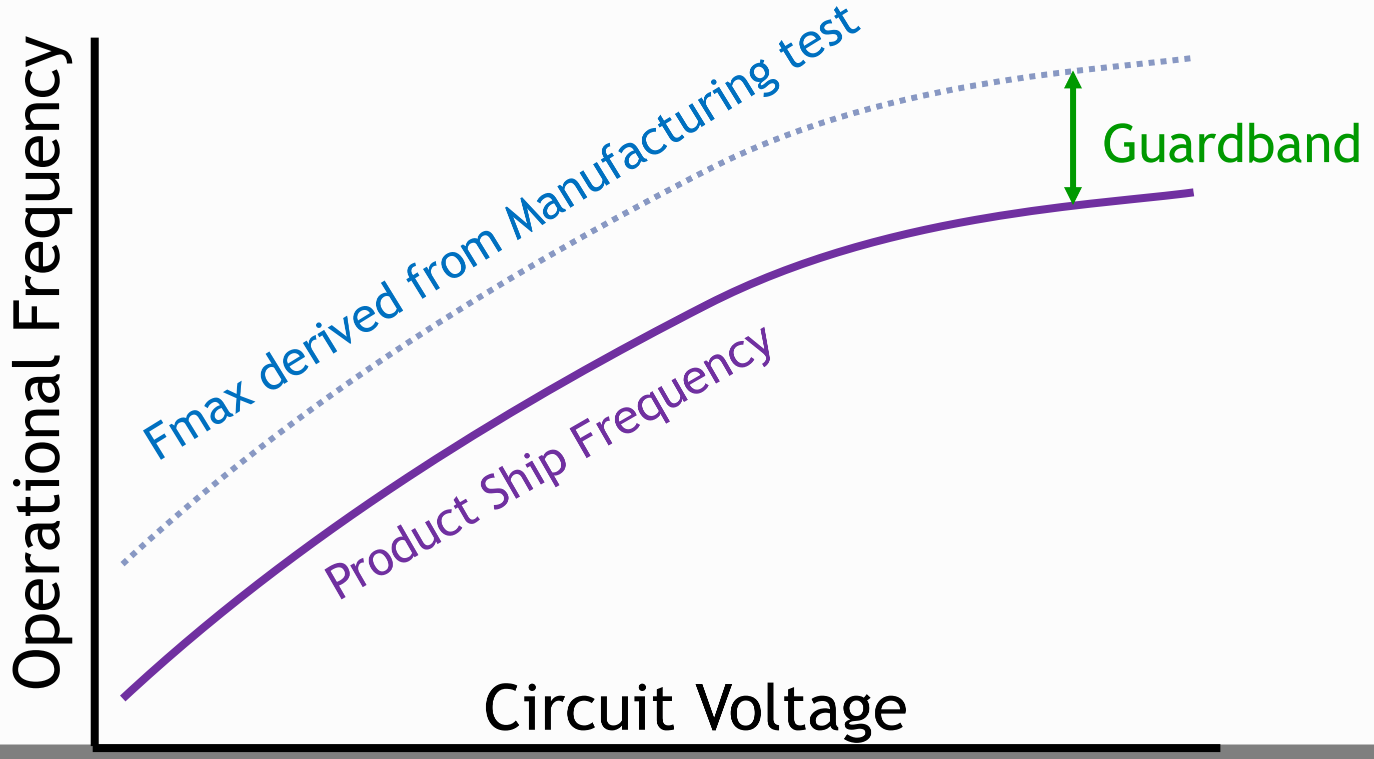


- RBB is effective to reduce leakage
- FBB is effective to improve operating frequency of a design in active mode
- PMOS & NMOS need independent body biasing

(A. Ghosh, ISQED 2008)

Guard bands

- Designs must account for changes over time:
  - permanent physical degradation
  - temporary operational transients



Typical guardband components

- Voltage variation

  power supply & system load-line inaccuracy, droop & noise

- Thermal variation

  environment & workload

- Wear out

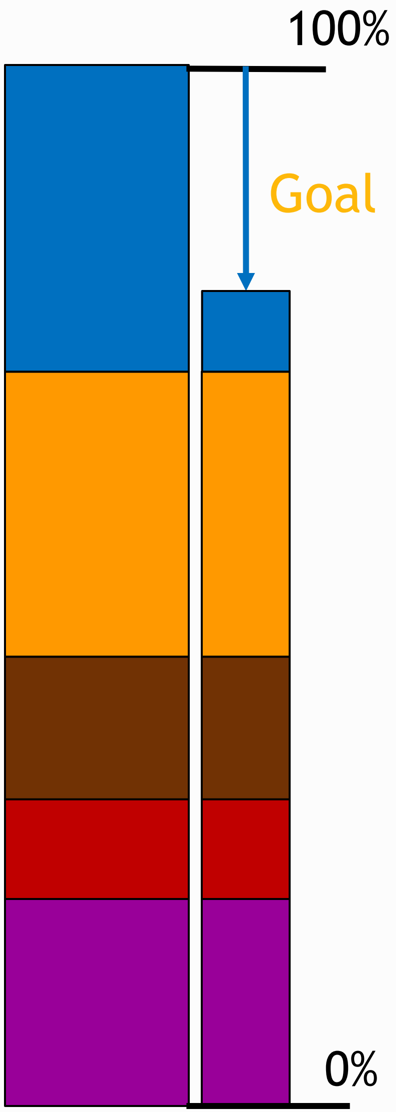
  lifetime degradation

- Manufacturing Test Inaccuracy

  correlation error

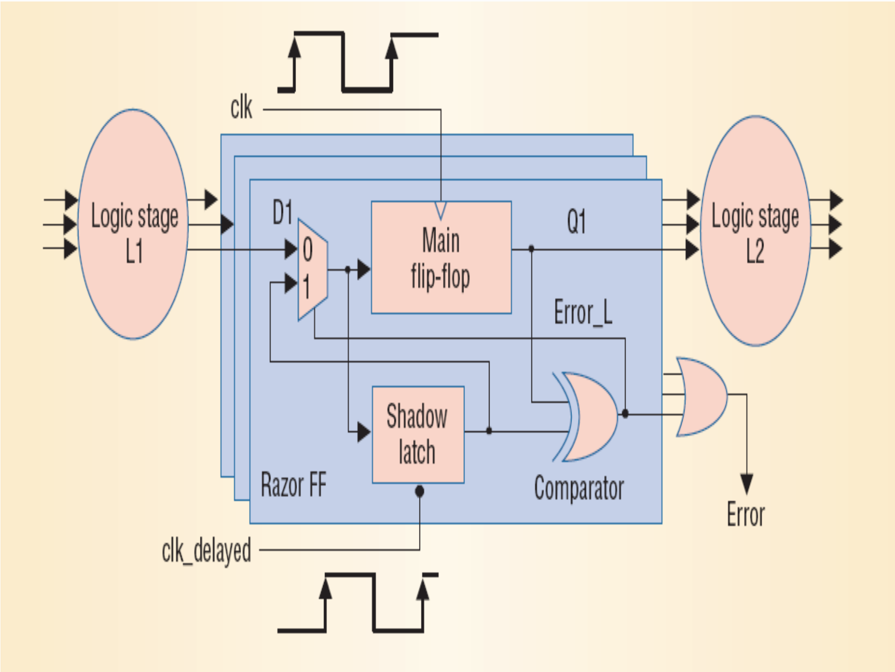
- Uncertainty

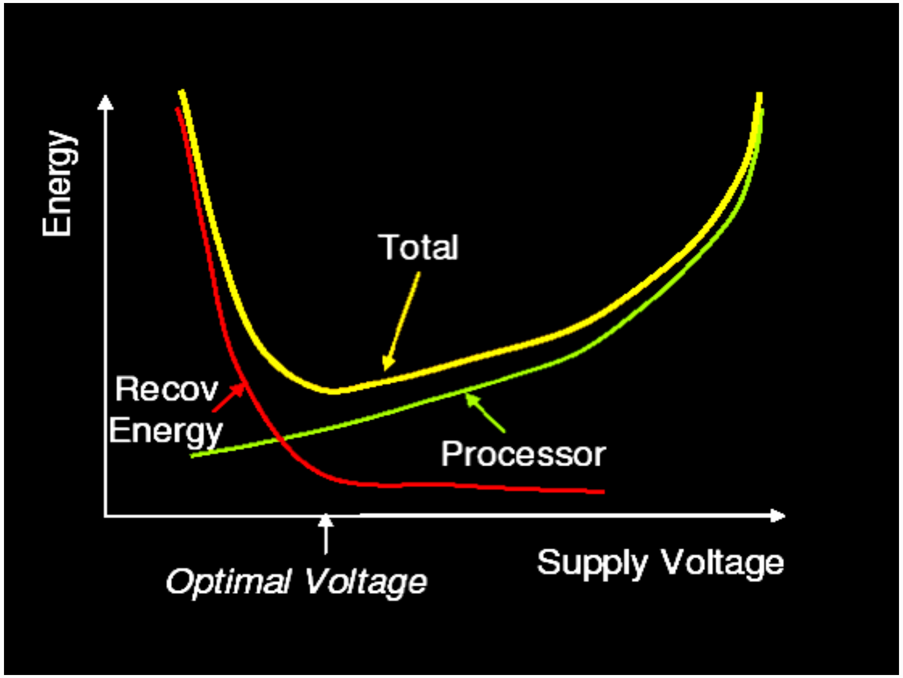
  margin for the “unknown”



Razor CMOS

- Shadow latch with delayed clock used to detect and recover setup time violation at high-frequency or low-voltage
- Tune voltage by monitoring error rate to remove voltage margin
- 64b processor implementing subset of Alpha instruction set in 0.18 μm CMOS
  - Eliminate V_{DD} safety margin, allowing V_{DD} to be scaled 120 mV below 1st failure point
  - 44% energy saving over W.C. conditions @ 0.1% target error rate & 120 MHz





(S. Das, VLSI 2005)