Variation Characterization

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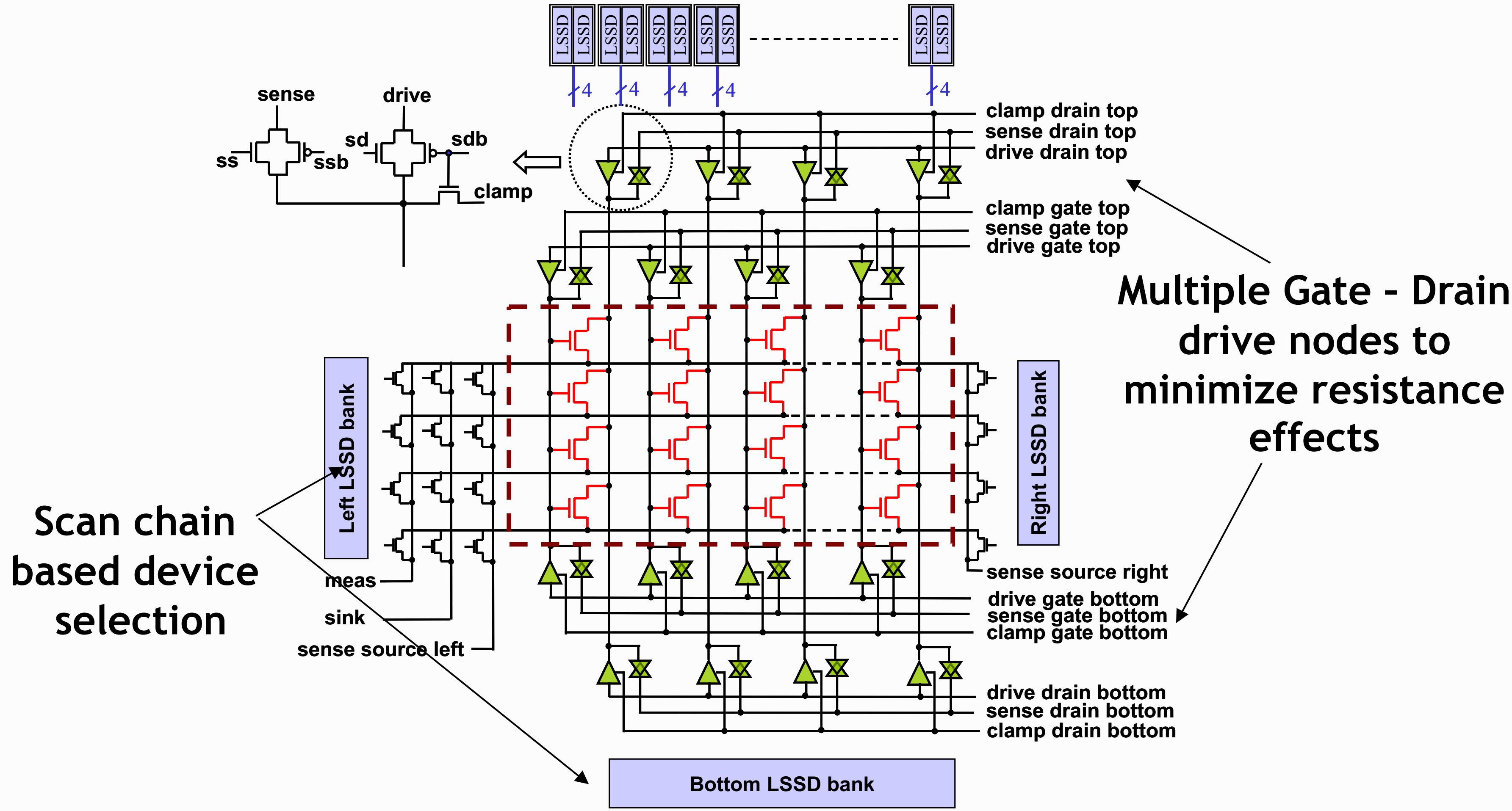
Characterization Circuits

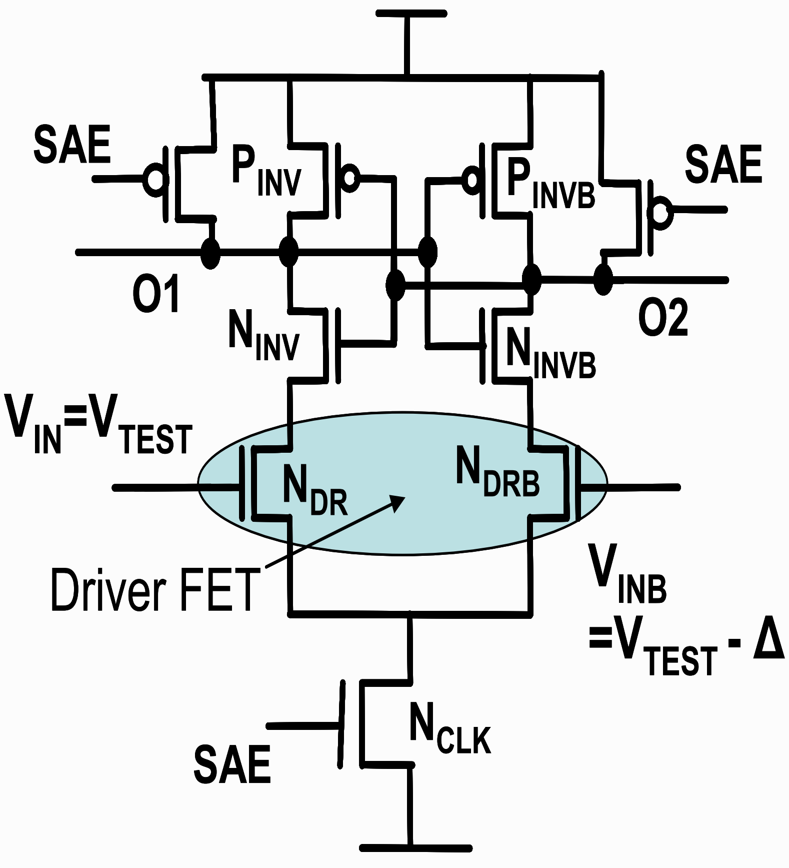
	Local Variation	Global Variation
Process	Early	Mature
What is characterized	Devices (Several)	Circuits
Output Feeds	Models, Technology Tweaks, Design Trade-Offs & Margins	Adaptive Mechanisms (Static / Dynamic), Field Failure Debug
Area Constraint	Ports (PI, Pos, Clk Infrasturcture)	
Power Constraint	Test Infrastructure Max Current Capacity (Test time vs Power)	If Always On. Else, Power Noise to neighboring Ckts
Timing Constraint	Test Time	Sense and React Time
Measurement	Analog or DAC based	Mostly digital
S/N Ratio	Cancel Global effects	Cancel local effects

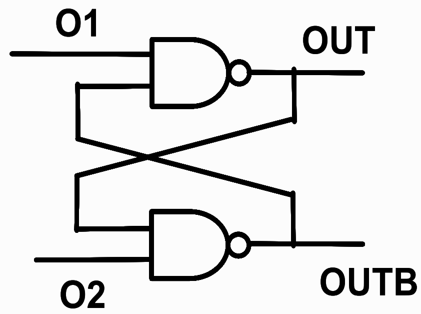
Array Based I-V Characterization Circuits

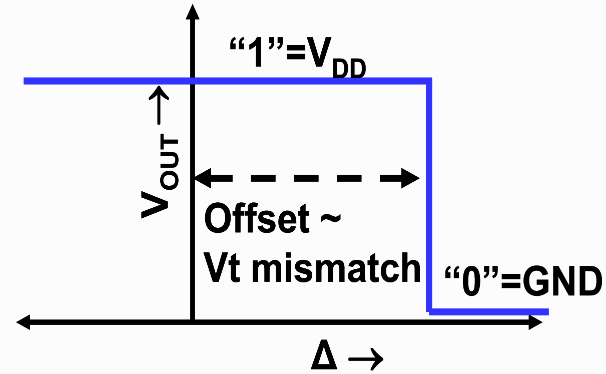


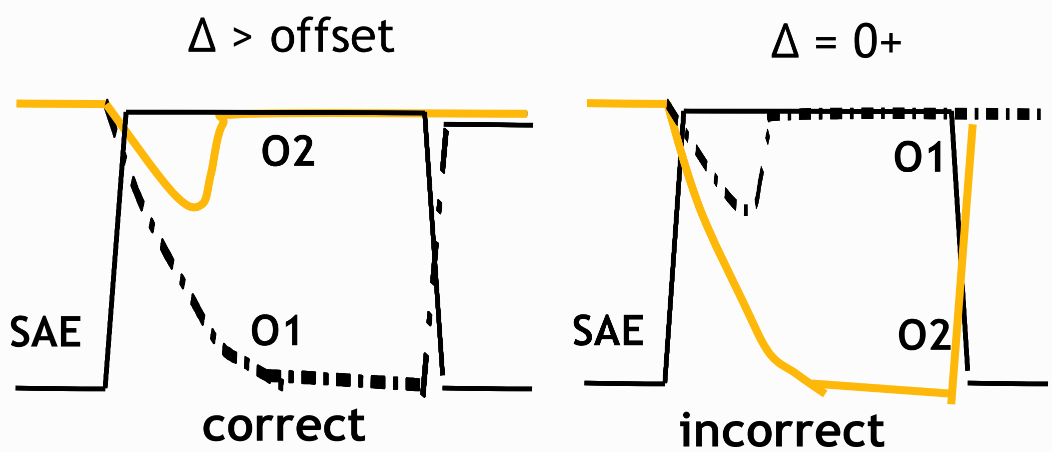
- Measure I-V of devices in an array
- Extract Vt mismatch from “current difference” between identical transistors

Digital Characterization with Current Latch based Sense Amplifier



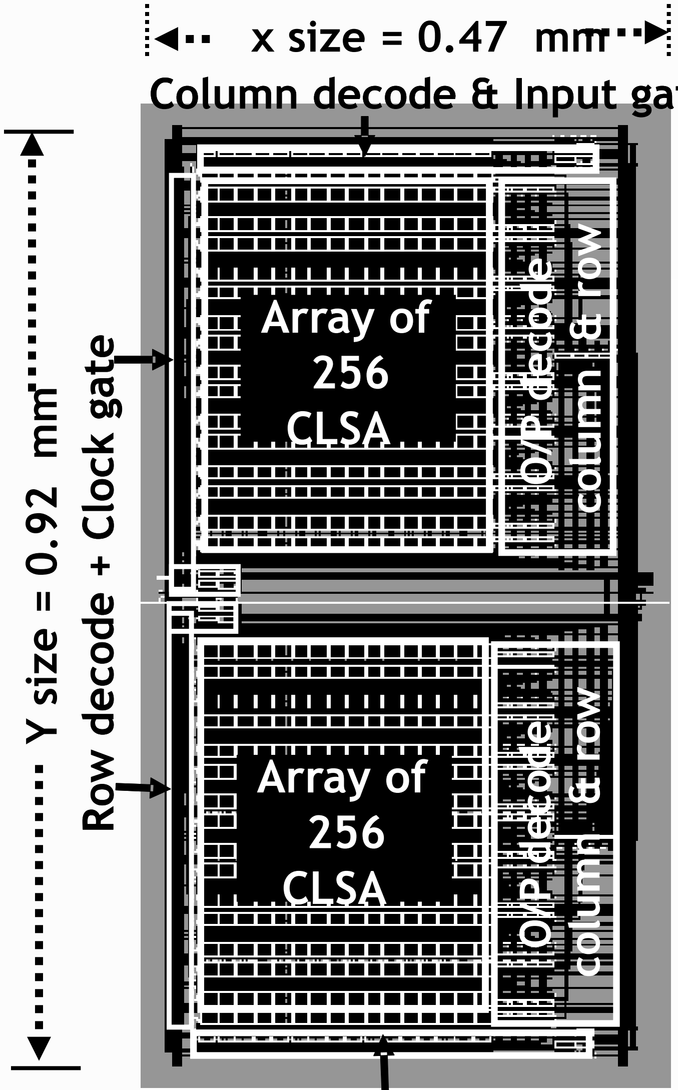




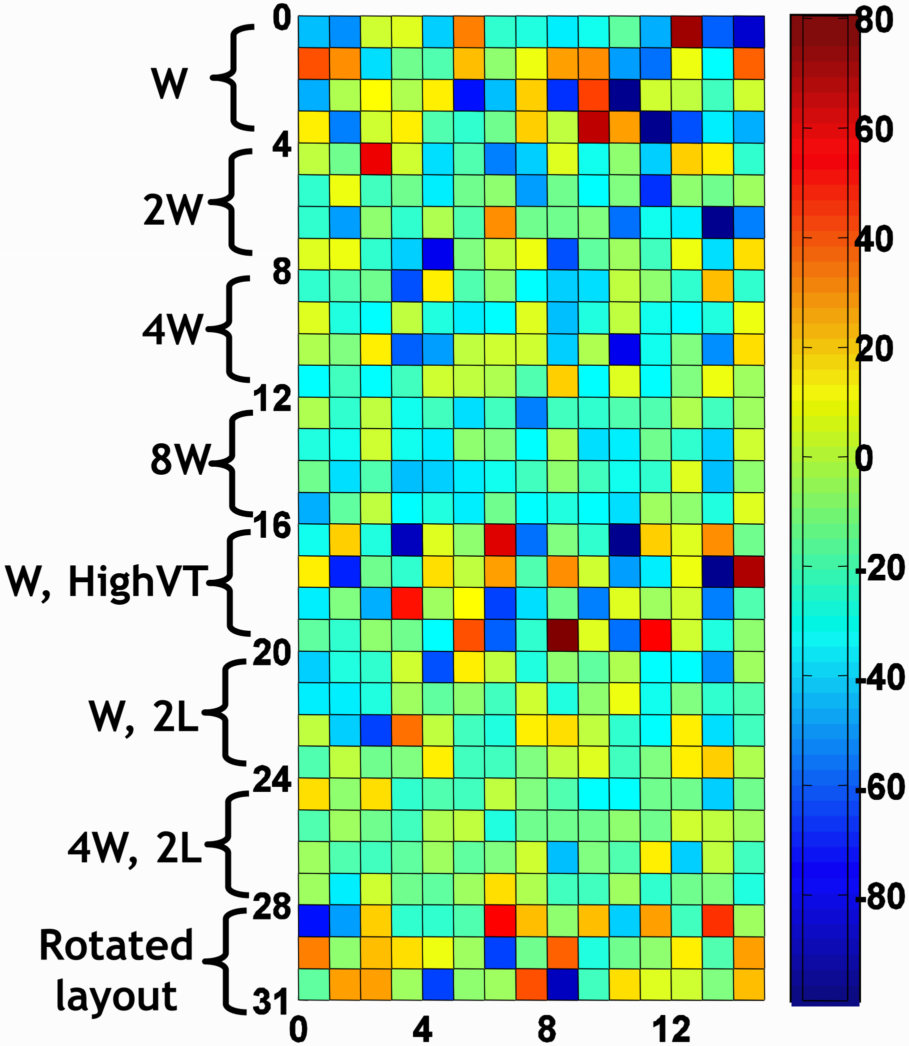


Minimum input voltage difference required for correct sensing (offset) indicates local random mismatch

Measured Values of Local Mismatch



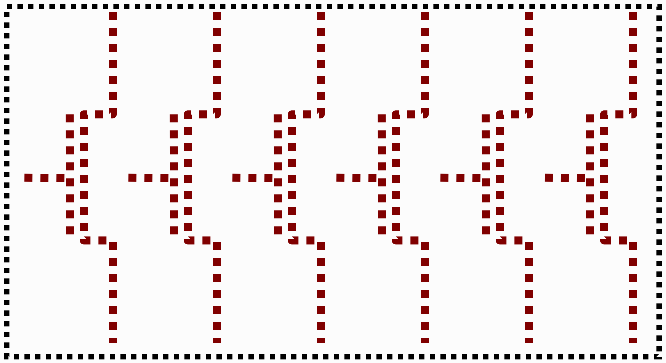
Layout of the proposed test-structure



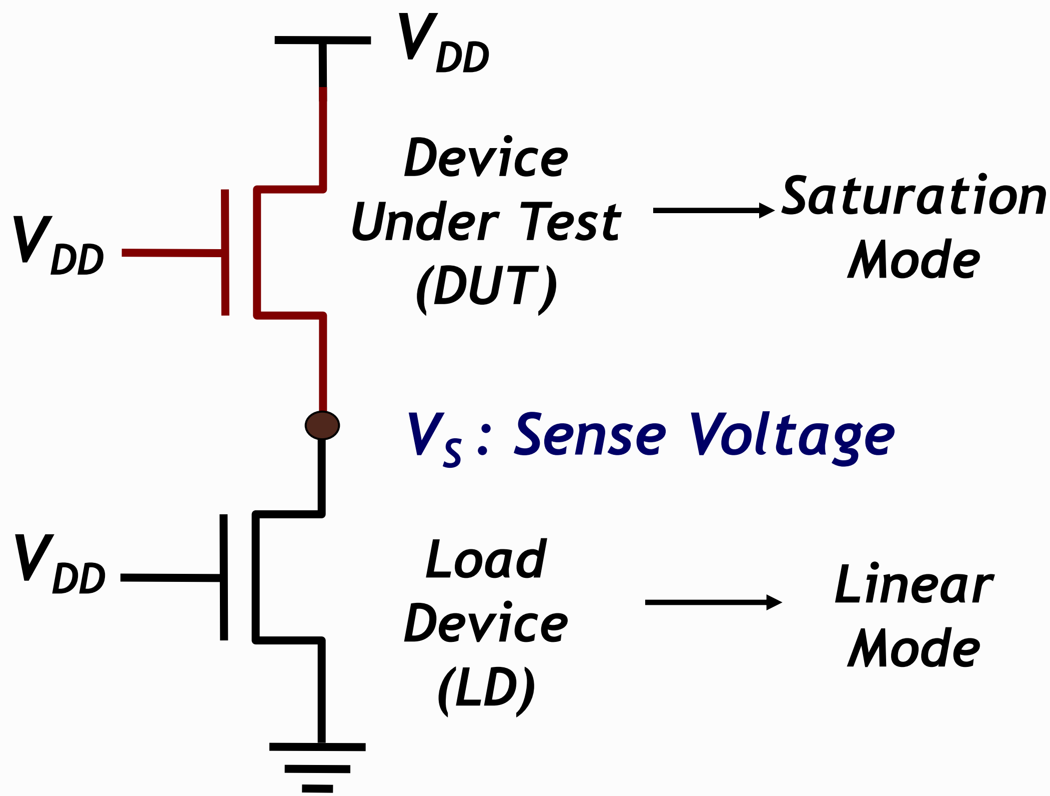
Vt mismatch values (in mV) measured in different location

S. Mukhopadhyay, et. al. JSSC 2008

Statistical Characterization of Local Variations of Individual Device



Array of identical devices



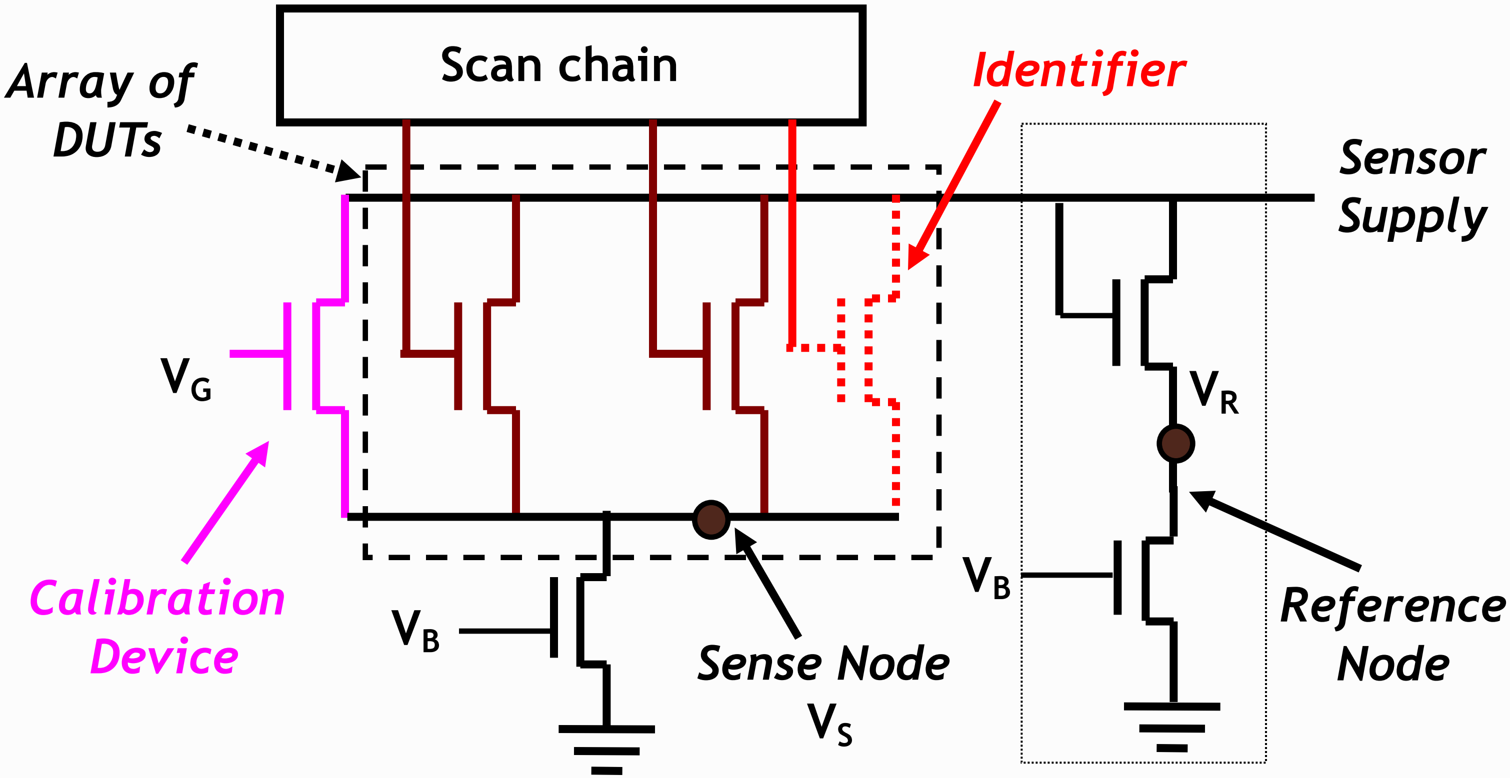
Test structure consisting of array of devices arranged in a stacked configuration with a common load device for local variability characterization

$$V_{S1} = f\,(V_{TH}\,(DUT1),\ V_{TH}\,(LD))$$

$$V_{S2} = f\,(V_{TH}\,(DUT2),\ V_{TH}\,(LD))$$

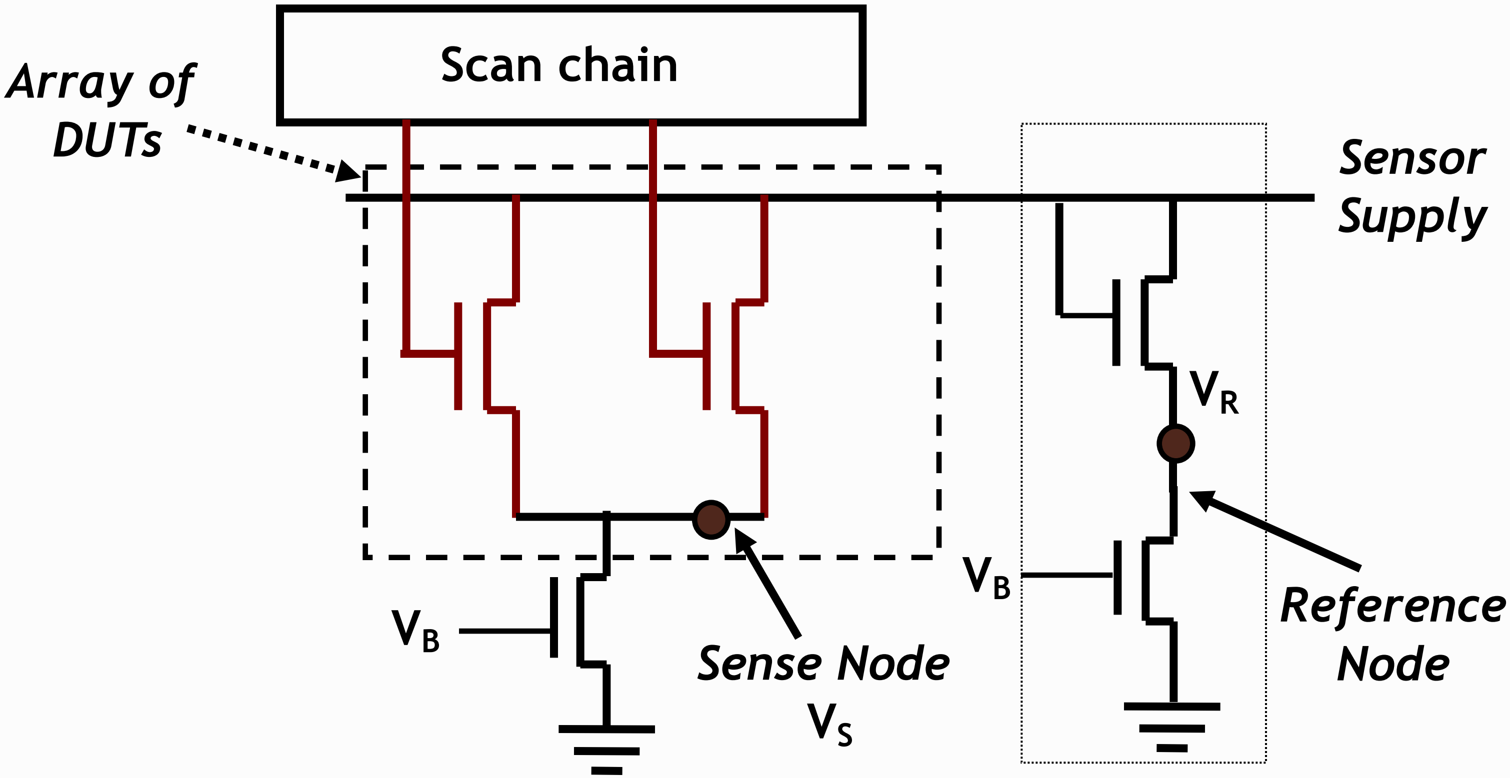
R. Rao et. al. JSSC 2009

Sensor Block



- Select each DUT individually to form stacked configuration with load device
- Determine Sense Node Voltage (V_S)
- Difference in V_S represents current mismatch between the DUTs

Sensor Block



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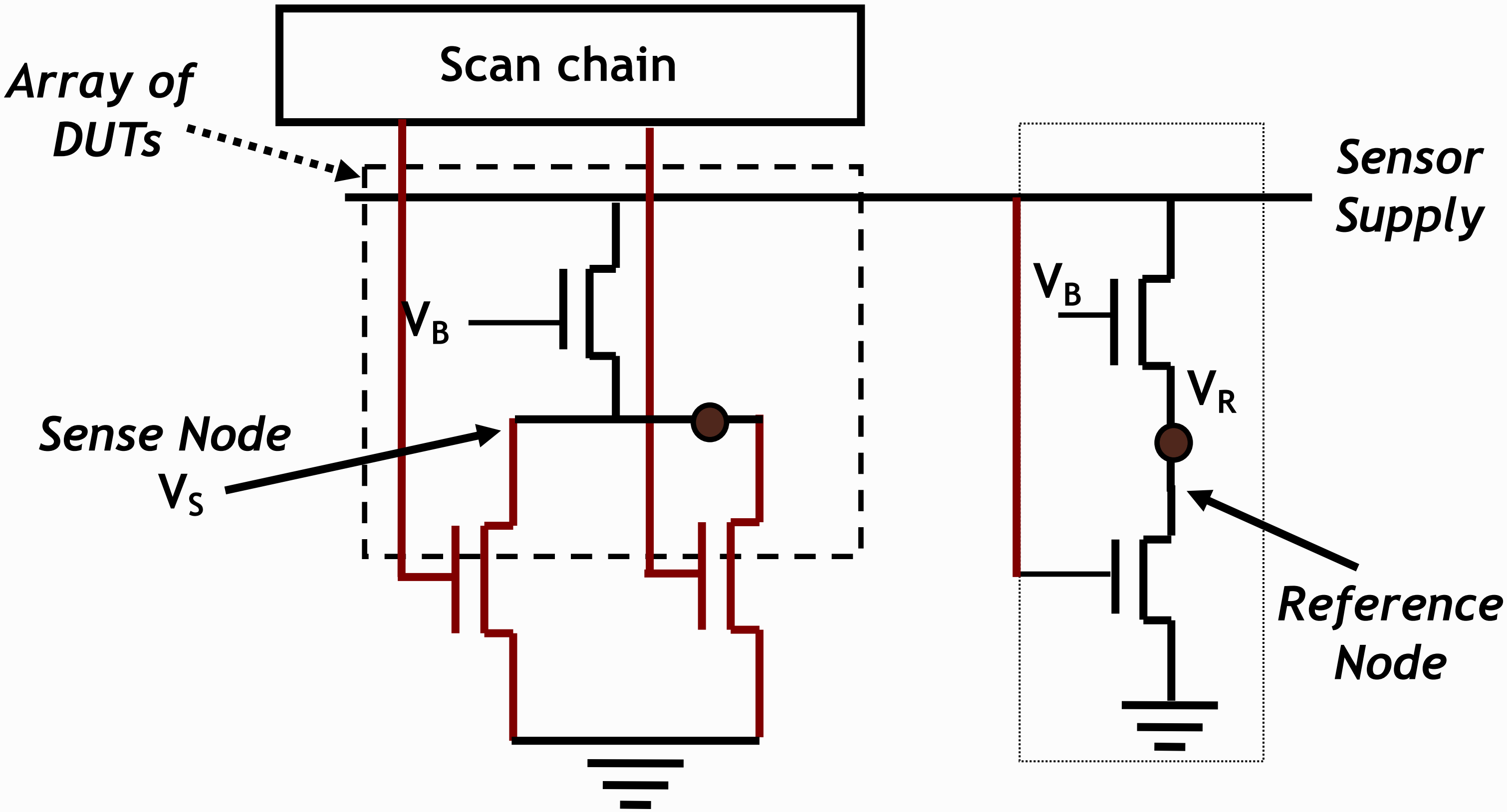
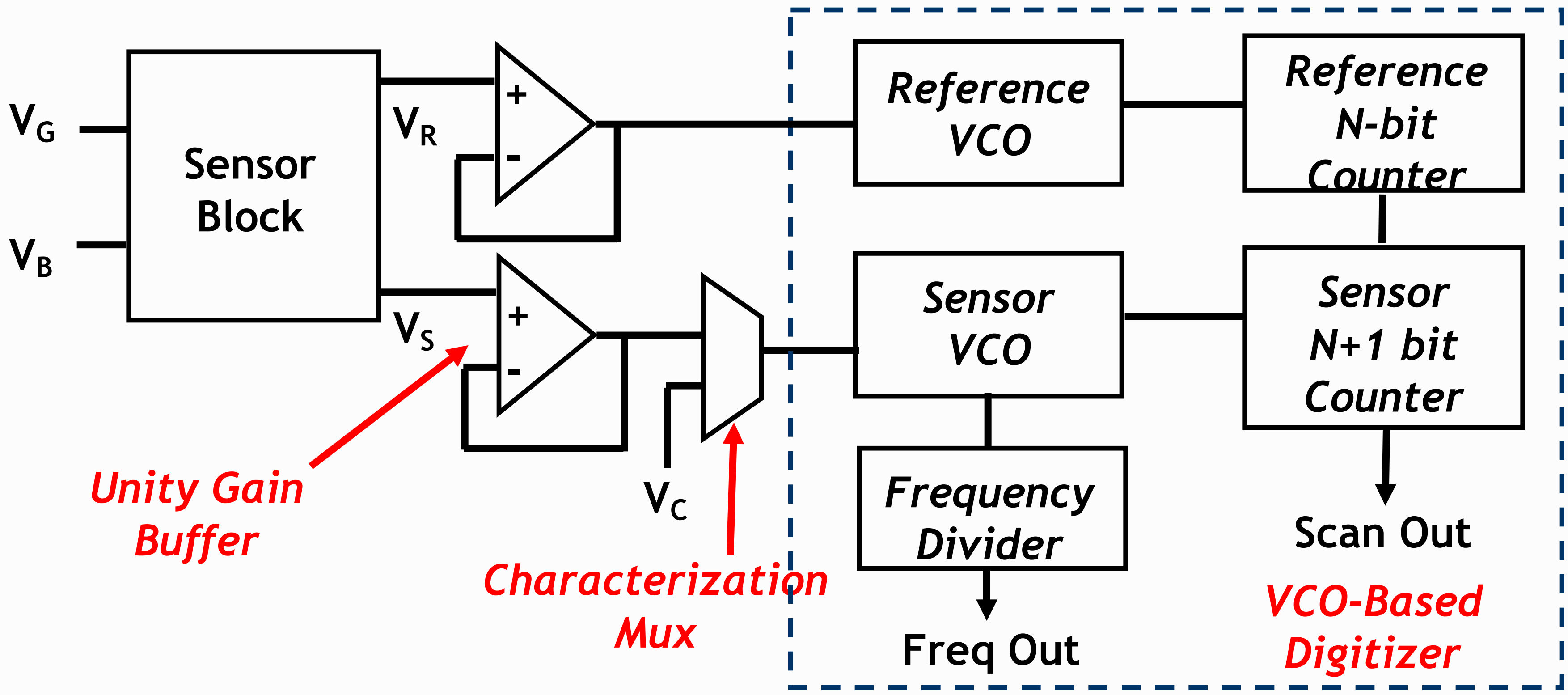


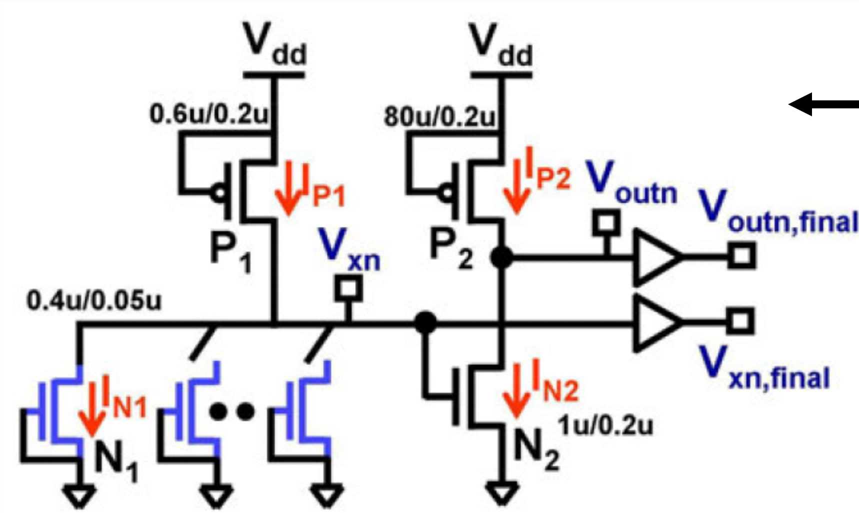
Block Diagram



- Unity Gain Buffer protects sense node from mux / VCO noise
- Reference VCO sets up time – base for Sensor Counter
- Output of Sensor counter is digital indication of sensor VCO frequency and hence a representation of threshold voltage of DUT

R. Rao et. al. JSSC 2009

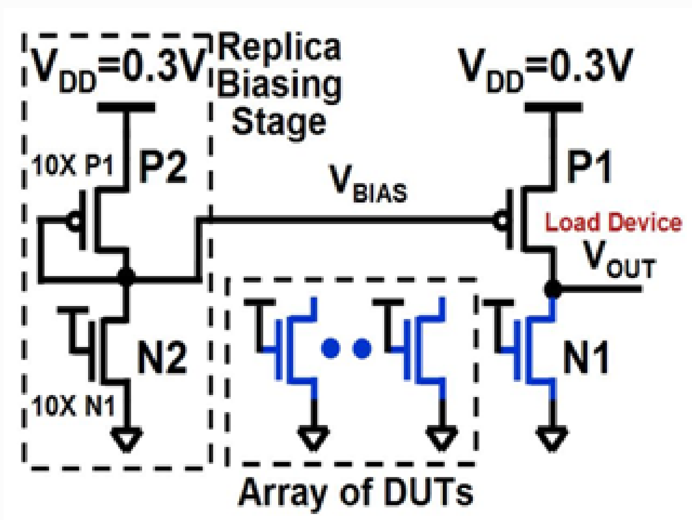
High Sensitivity Variation Sensor



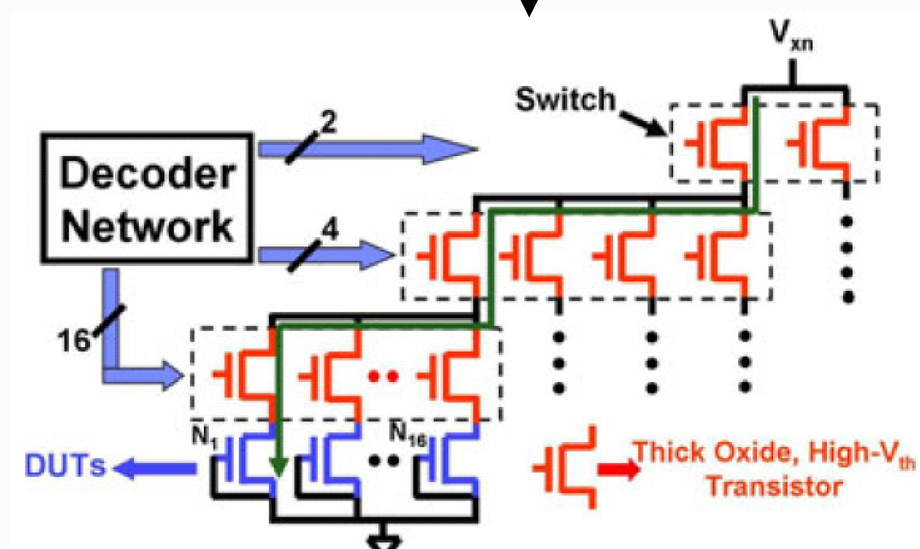
Biasing DUTs in sub-threshold mode to enhance sensitivity

2nd stage is for amplification

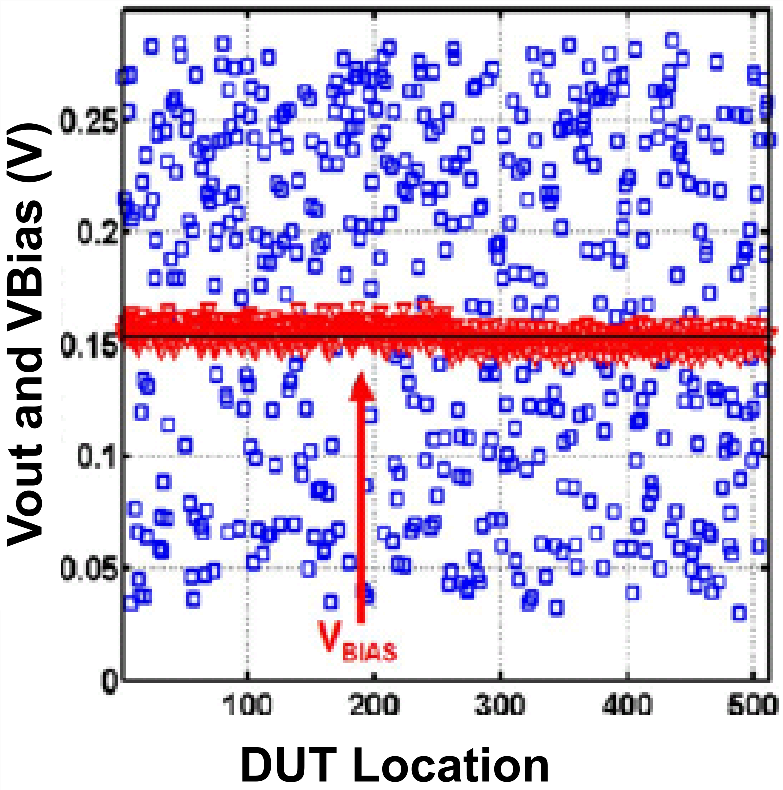
Hierarchical Switch Network to minimize leakage noise from unselected DUTs



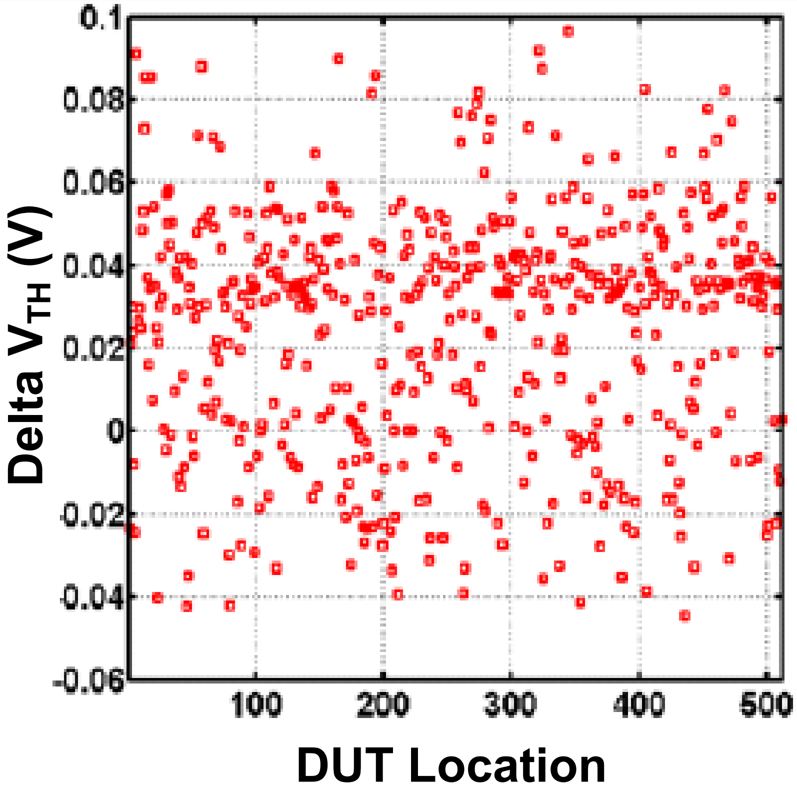
On-chip generation of VBias



High Sensivity Variation Sensor



Measurement for 512 minimum sized DUTs



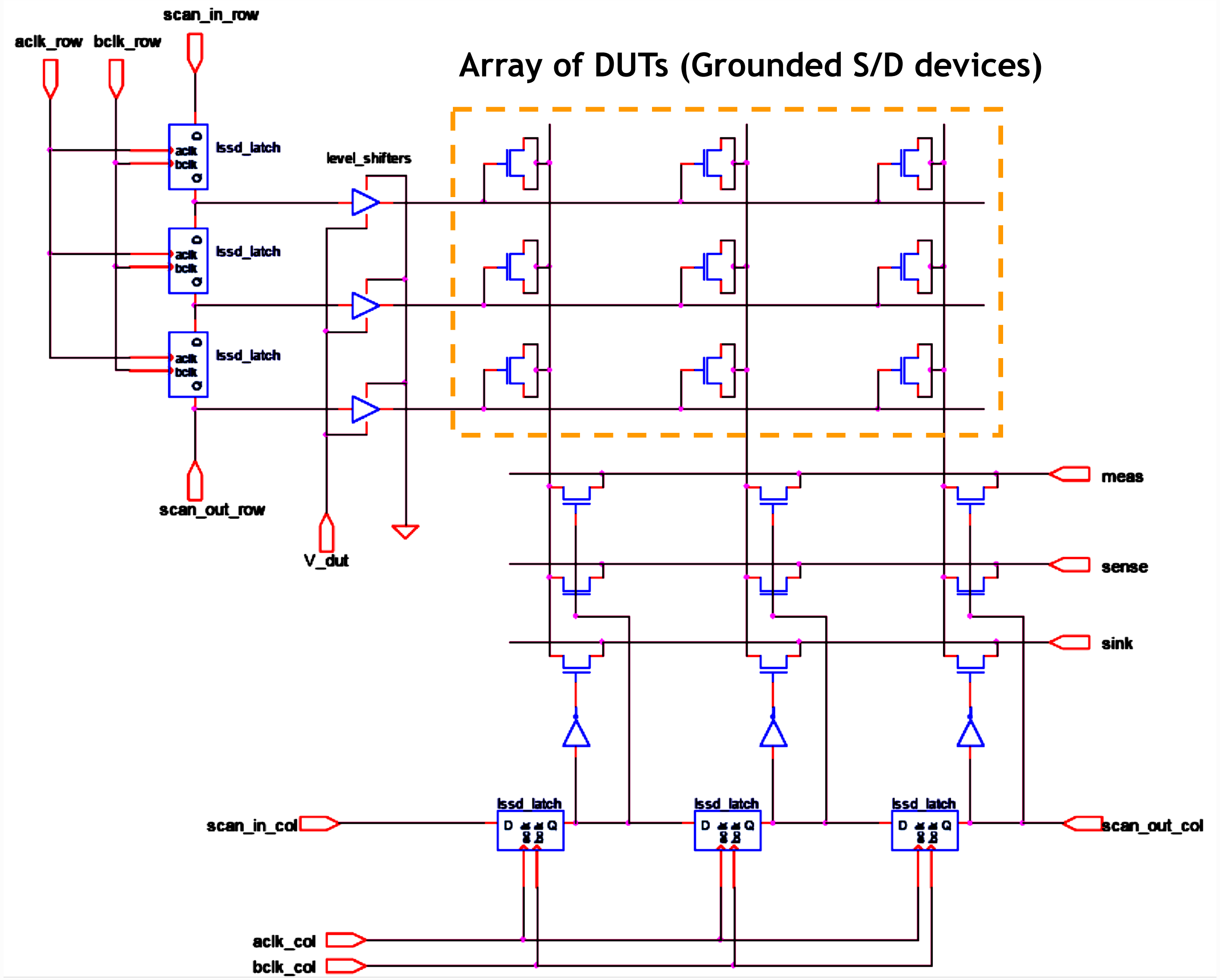
Extracted V_{TH} from measurement

Improving Signal to Noise Ratio

❑ Approaches used to improve signal to noise during measurement include

a) Clamp gates of unselected DUTs to a negative voltage
b) Raise the voltage applied to the selection devices
c) Use voltage measurement instead of current measurement
d) Use forced stacking on the selection devices

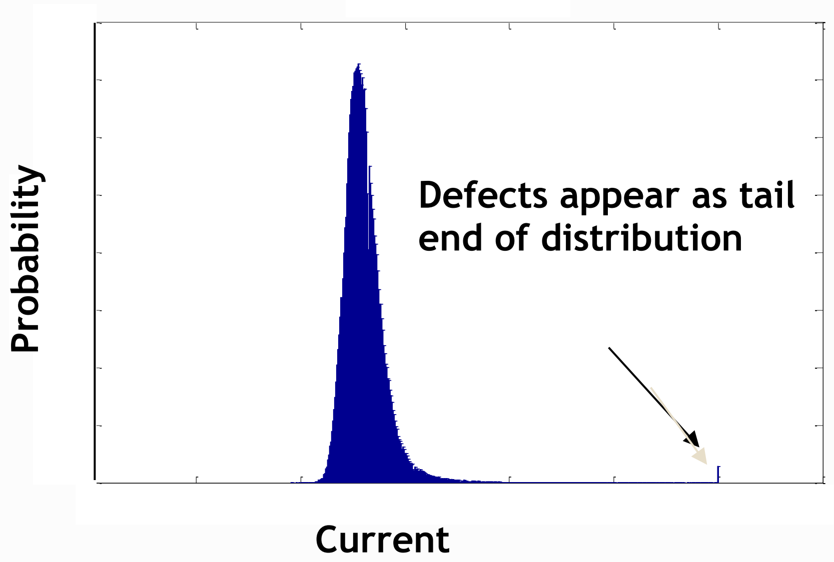
Gate Oxide Monitor



J. Sivagnaname, et. al, US Patent 7409372

Gate Oxide Monitor

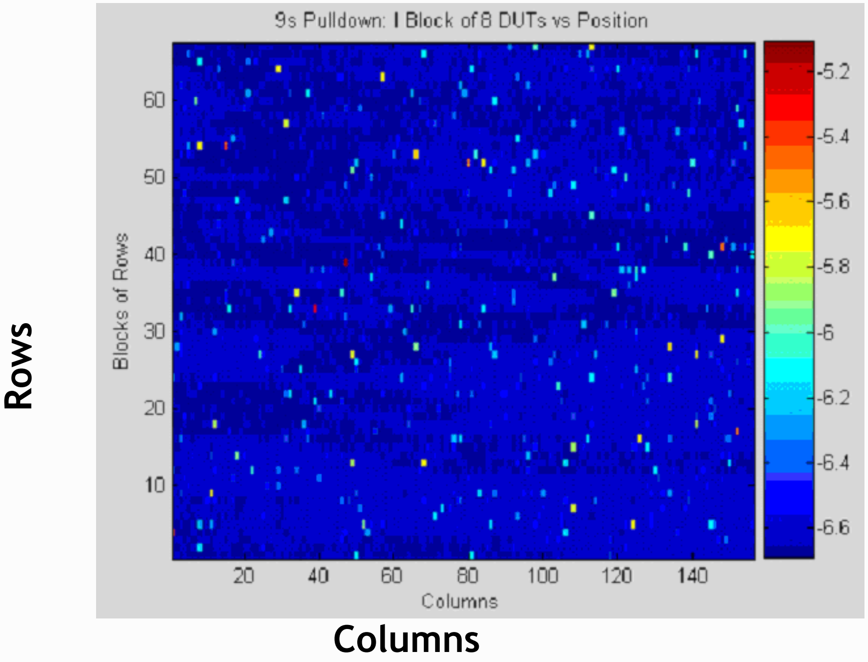
Gate leakage variation



- Characterizes Gate Oxide Defects

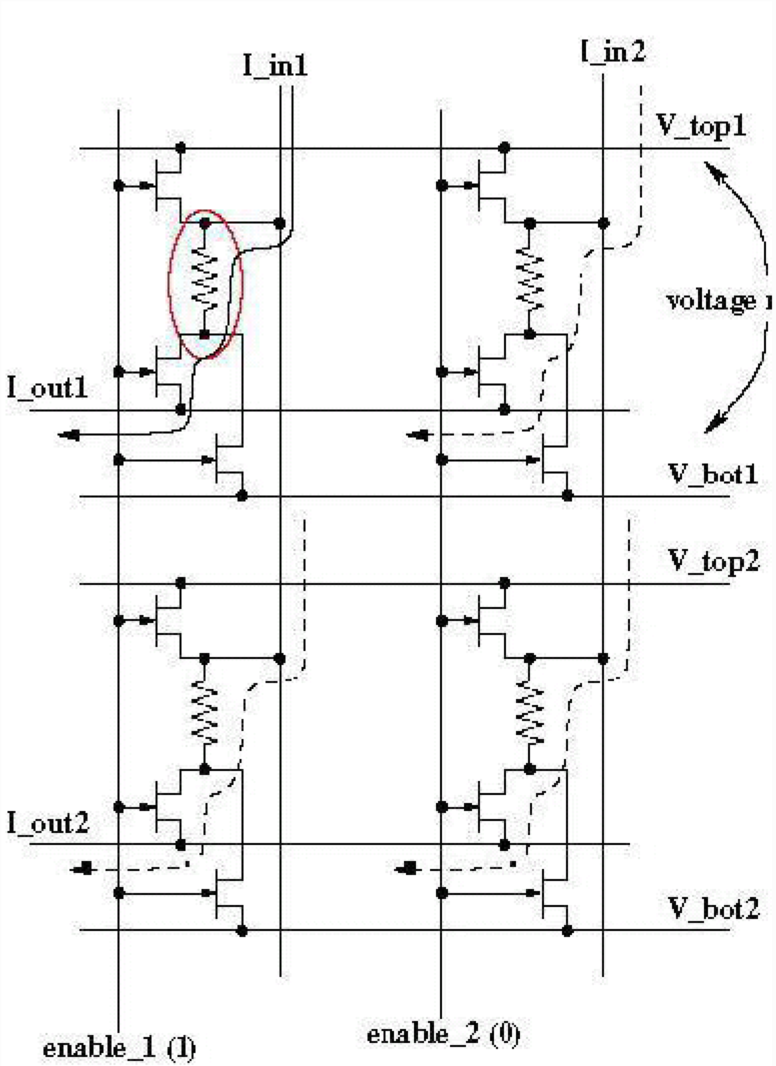
- Millions of SRAM devices in an individually addressable array

- Measure gate leakage currents to identify defects



J. Sivagnaname, et. al, US Patent 7409372

Contact Resistance Sensor

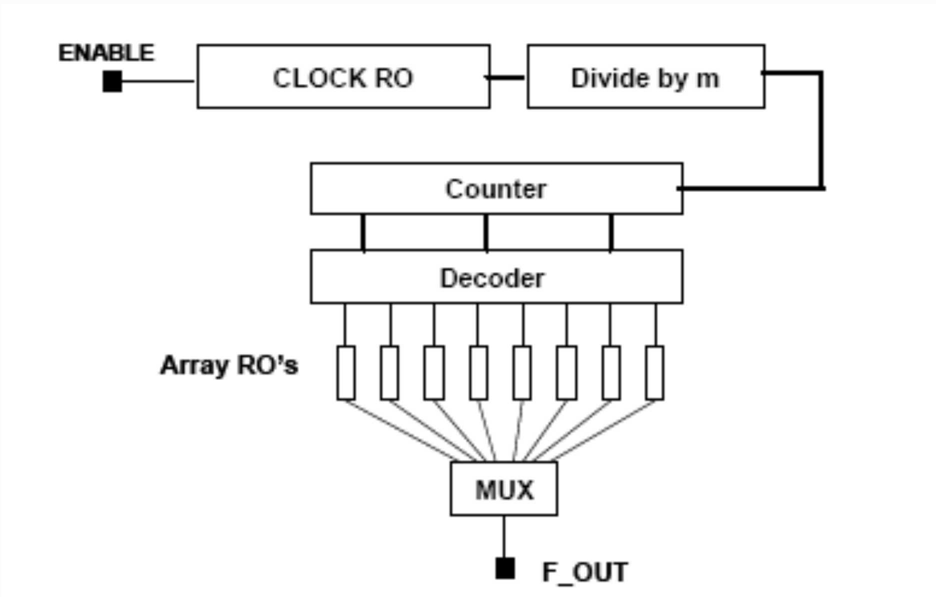


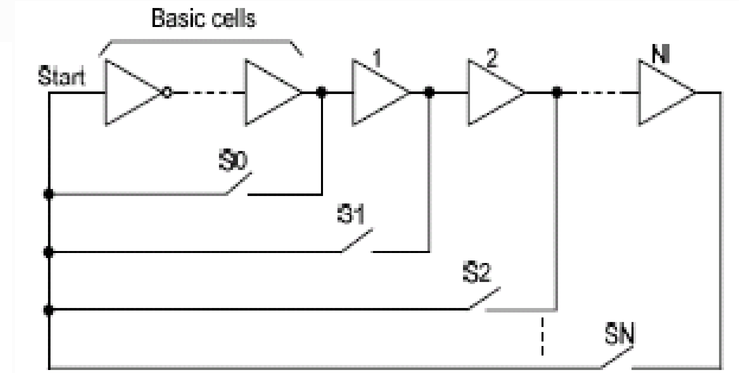
- Array of Contact cells
- Each Row has V_top(i), V_bot(i) and I_out(i)
- Each column has I_in(j) and enable(j)
- For selected DUT, enable(j) ensures that I_in(j) is steered to I_out(i)
- V_top(i) and V_bot(i) are sensed to estimate CA resistance
- For unselected columns, Enable is kept below 0 to reduce leakage noise

How to characterize global or systematic variations in process ?

- Challenge
  - Sense and characterize observable circuit parameters that depend on process parameters
- Methods
  - Delay based sensing
  - Slew based sensing
  - Leakage based sensing

Ring Oscillator Structures



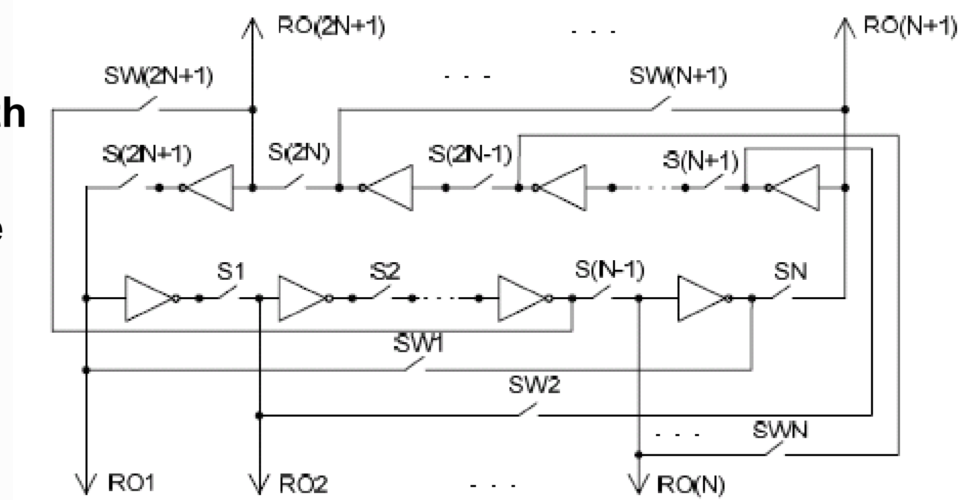


Modified Ring Oscillator

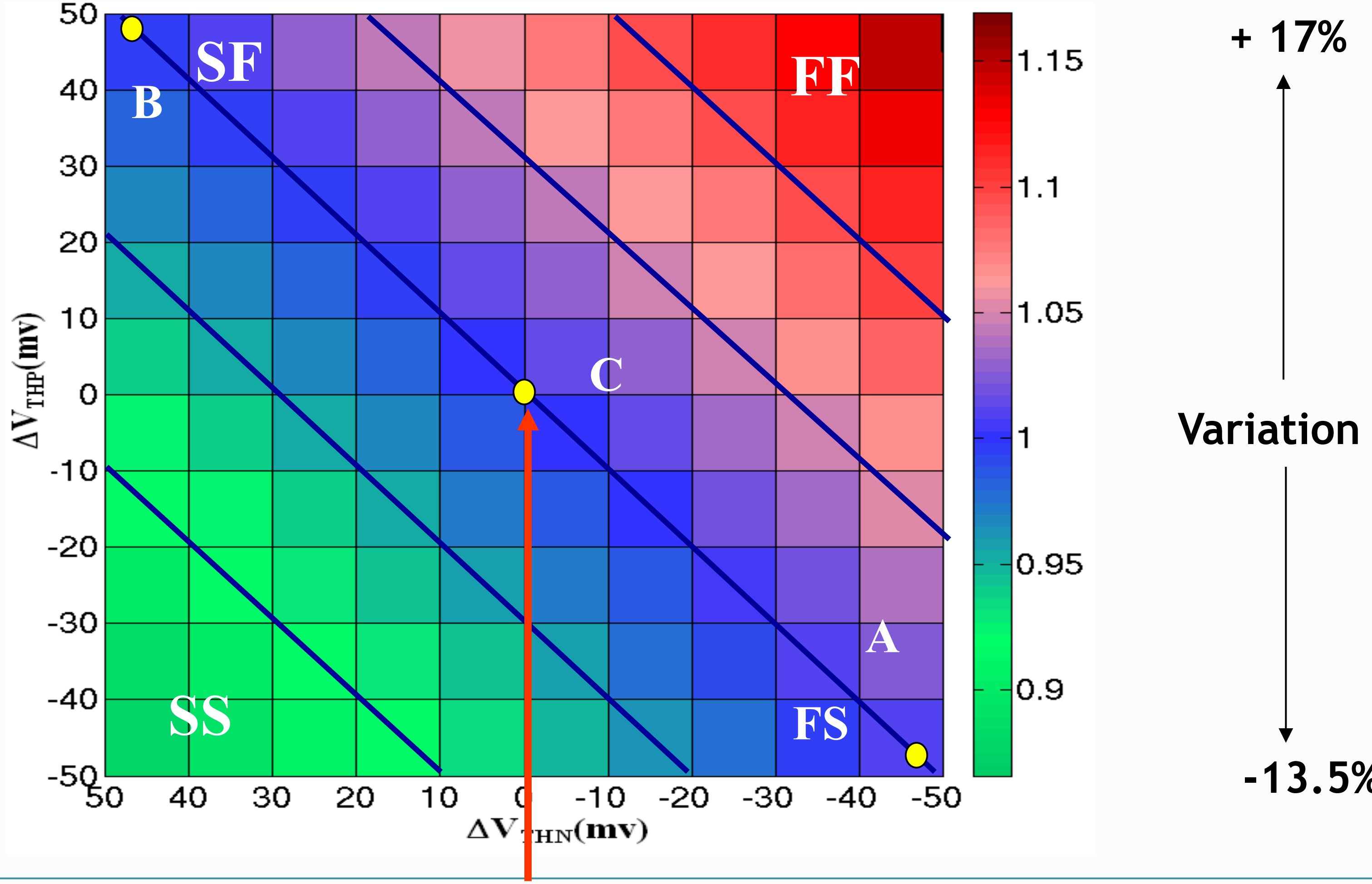
Oscillators of different gate lengths by tapping multiple nodes

Ring Oscillator (RO)

- **FET to FET variation averaged out with large number of stages**
- **Multiple ROs selected through a finite state machine (or counter)**
- **Frequency is independent of down-stream delay of the multiplexer**



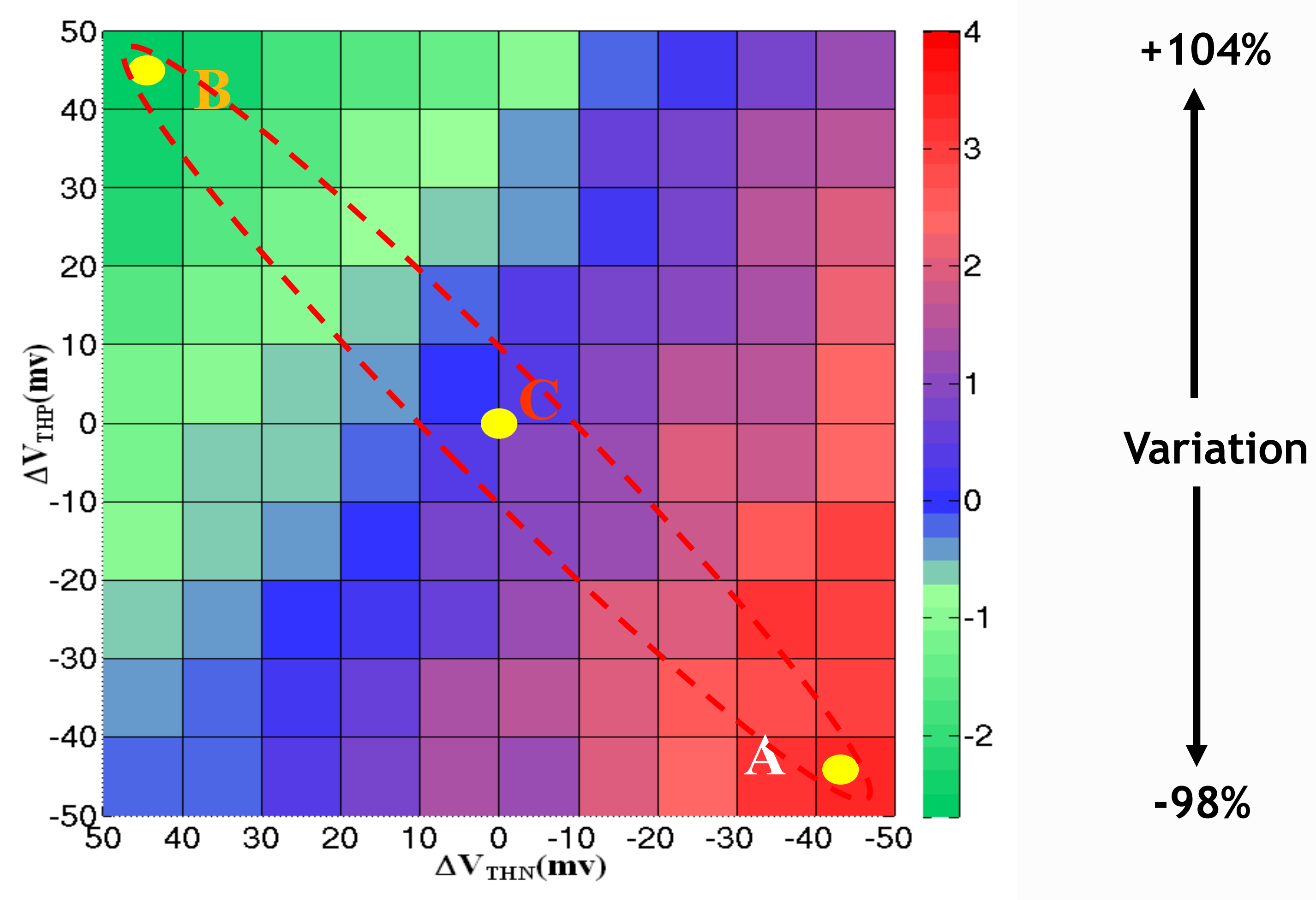
Delay Variation of a Ring Oscillator



Nominal operating point of the circuit with no threshold voltage variation

Delay is good for detection of Slow-Slow and Slow-Fast Corners

Normalized Slew

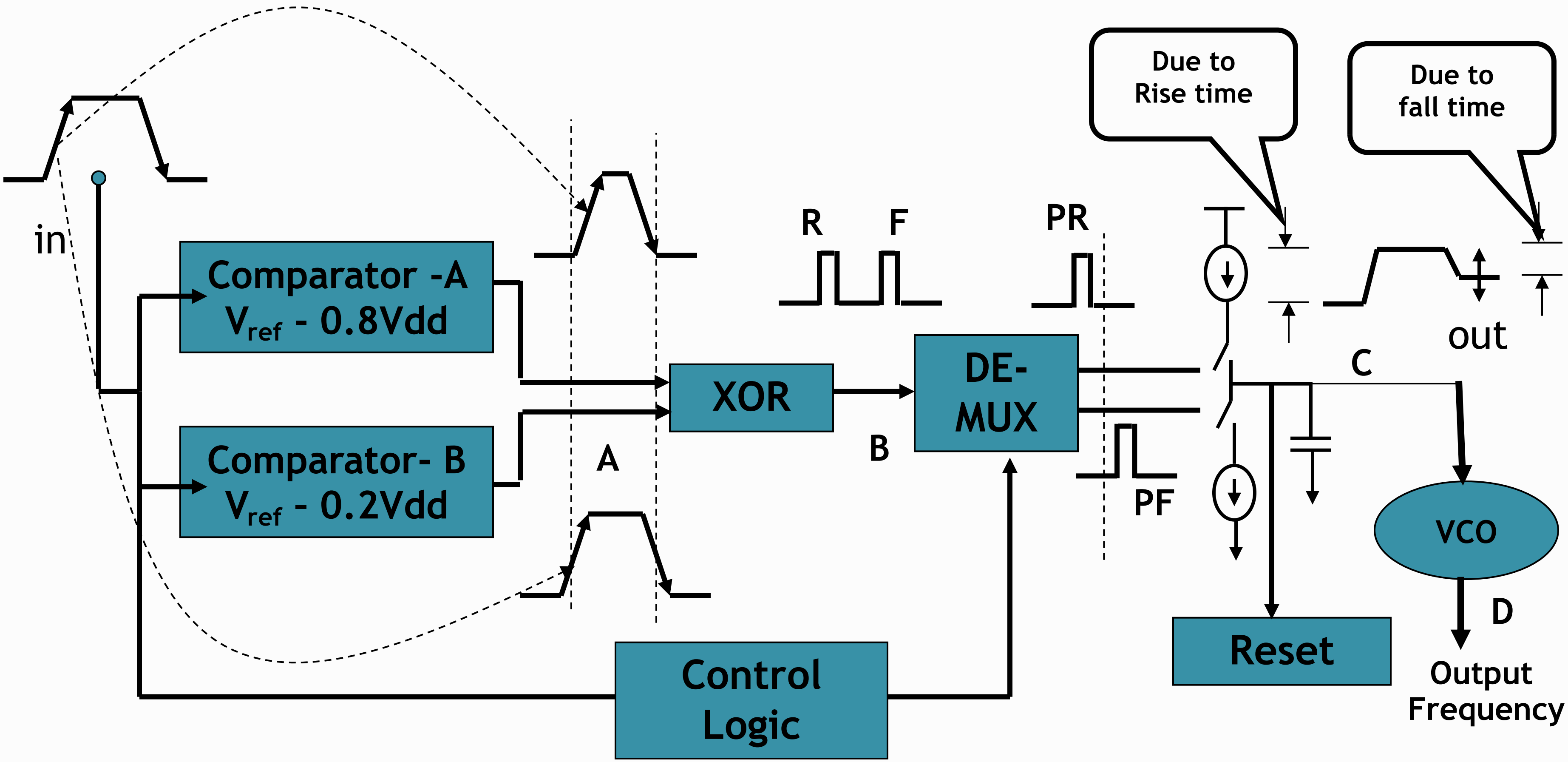


Slew is more sensitive to mismatch in device strengths

Good for detection of Slow-Fast and Fast-Slow Corners

Slew Monitor

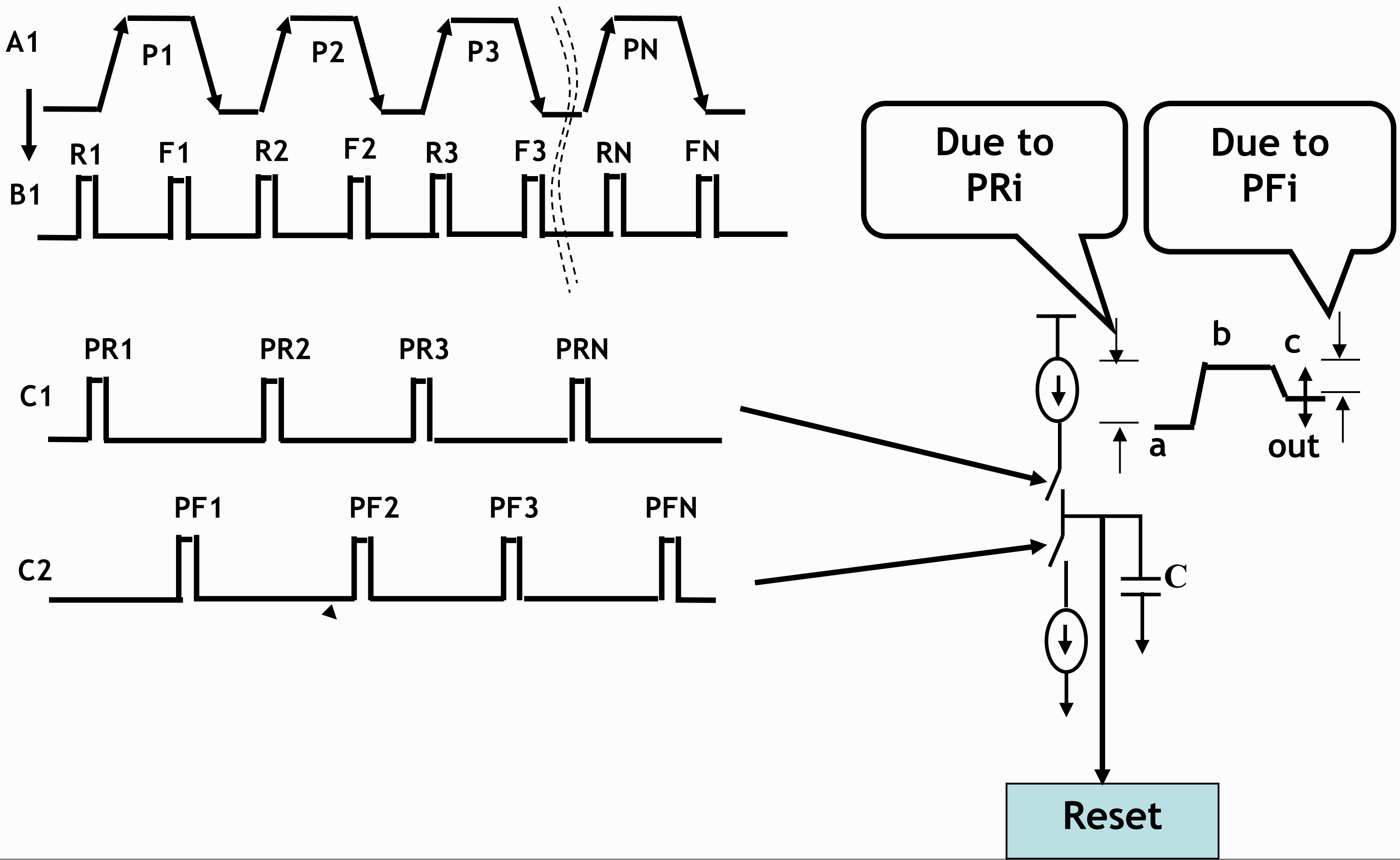
$\Delta_{rise\text{-}fall}$ - the relative mismatch between the strength of the NMOS and PMOS devices



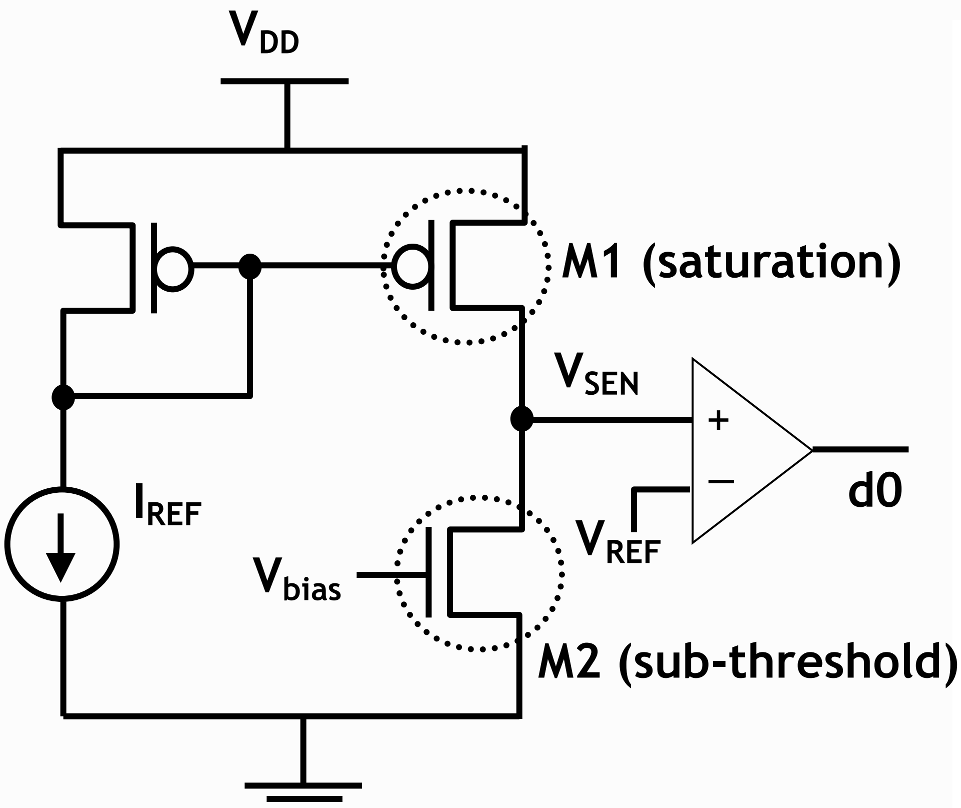
Can be used to drive body bias compensation for NMOS and PMOS devices for leakage control

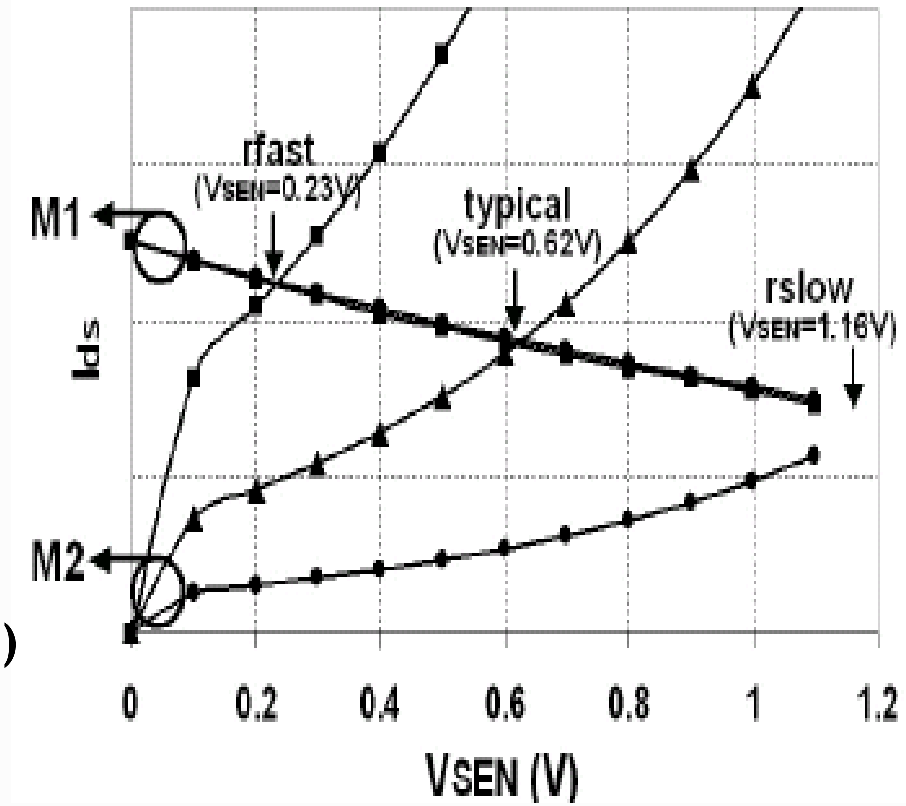
A. Ghosh et. al, VLSI 2008

Using Multiple Pulses to Improve Sensitivity



Leakage Detection Circuit

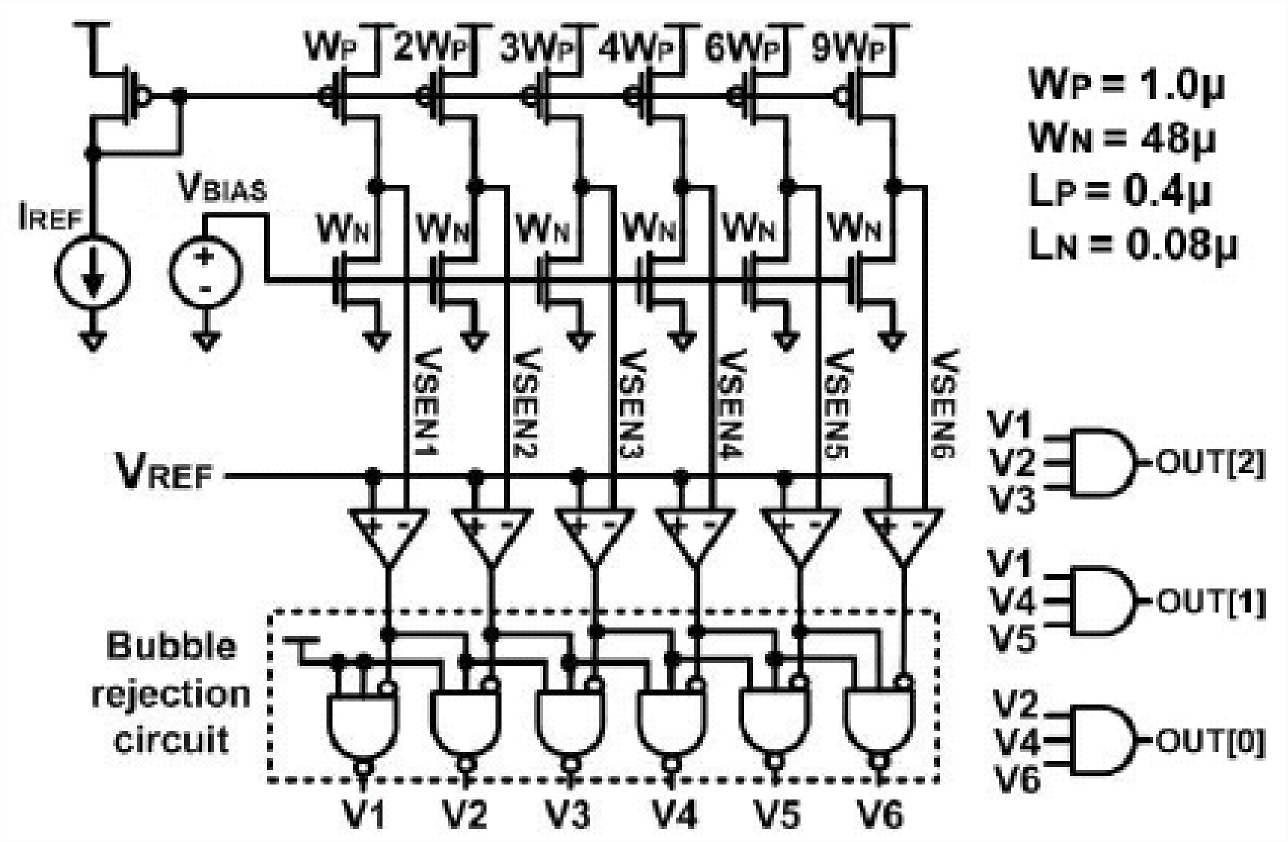




- Sense the current of a transistor in sub-threshold
  - Intersection of the two curves represents the voltage output
  - Generate PVT tolerant I_{REF} and V_{bias}

C. Kim et. al. VLSI 2004

Multi-Channel Leakage Sensor



- **Use PMOS devices of different widths to obtain multiple channel leakage sensor**
  - **Digital signature of analog leakage variation**

C. Kim et. al. VLSI 2004

Improving Signal to Noise Ratio

- ❑ An oscillator with large number of stages

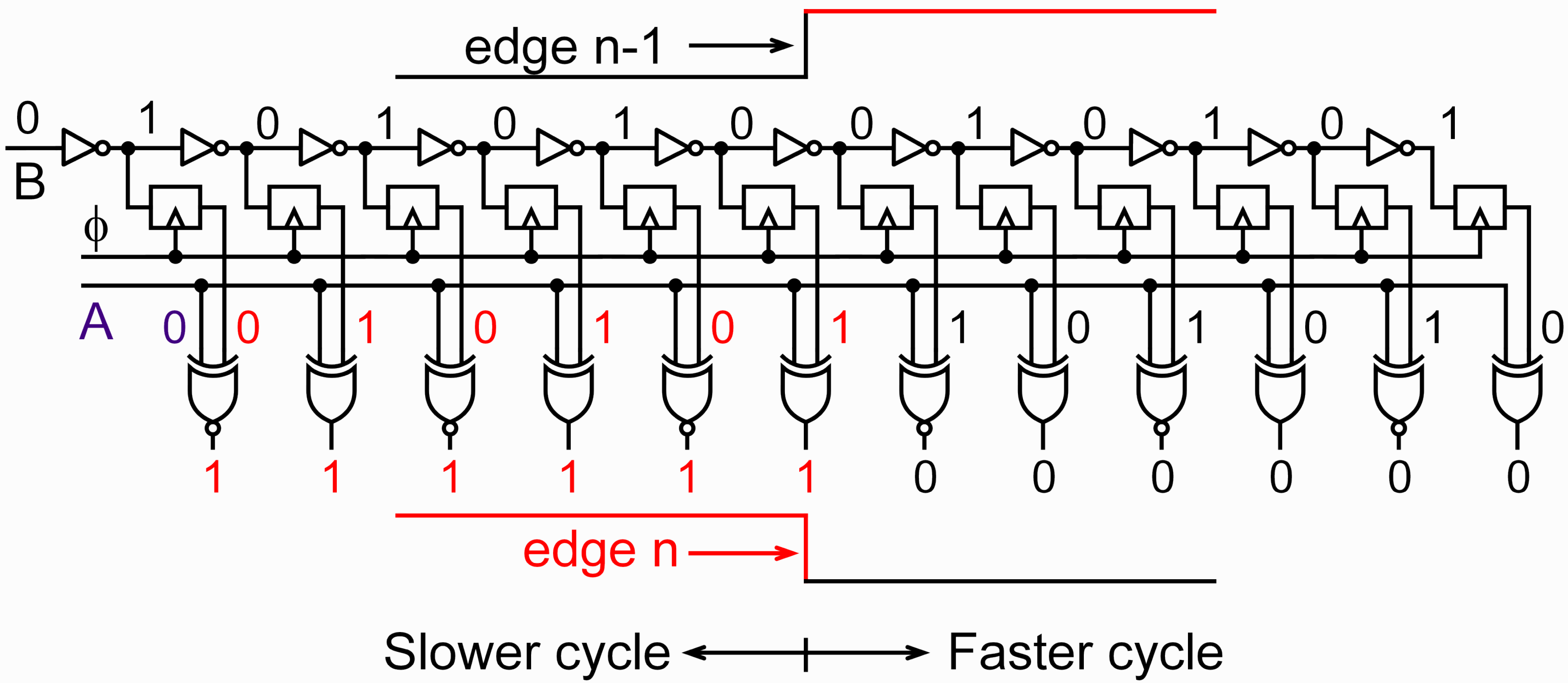
a) Helps differentiate variation by device type

b) Averages out the effect of local variation

c) Requires fewer division stages before readout

d) Shouldn't be used for a VCO operation

Time-to-Digital Conversion Using an Edge Detector

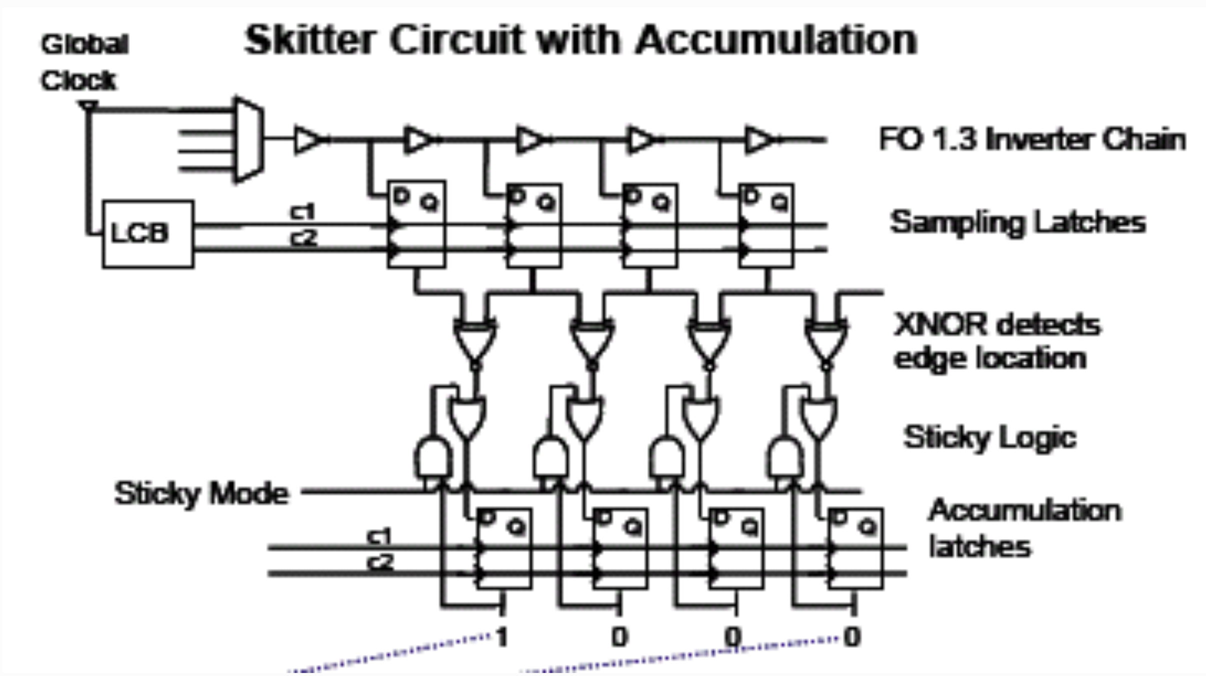


- **Edge movement due to**
  - **Changes in clock cycle**
  - **Changes in path delay**

A. Drake et. al. ISSCC 2007

Skitter (Skew + Jitter) Circuit

- Measure timing uncertainties from all sources
- Track skew between different regions (also environmental effects)
- During debug, detect supply voltage droops, detect failure mechanism
- Complete digital readout through scan-chains
- Cycle-Cycle variation, Best-Worst case detection



R. Franch, ITC, 2007

Skitter (Skew + jITTER) Circuit