Advanced Topics in VLSI

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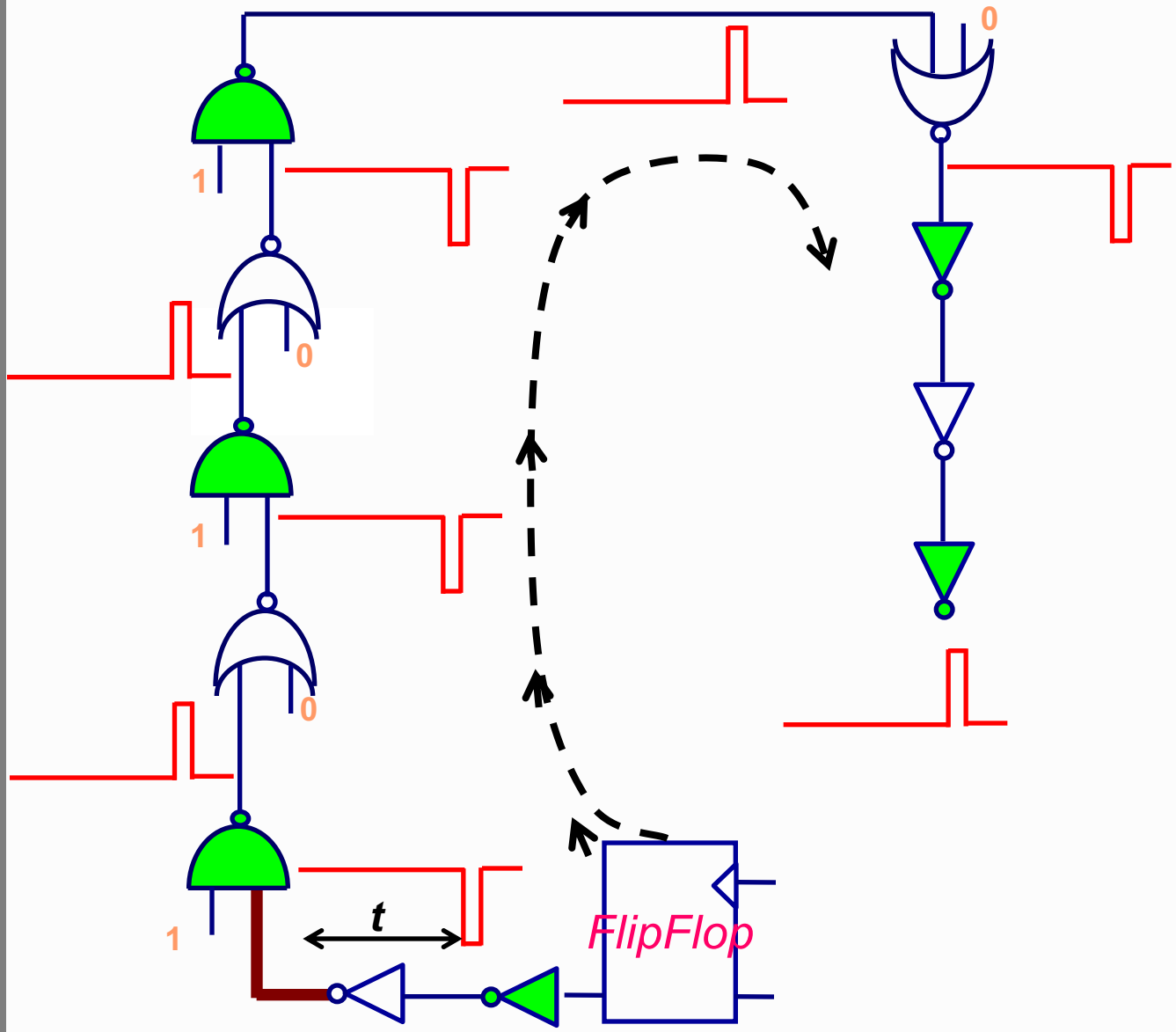
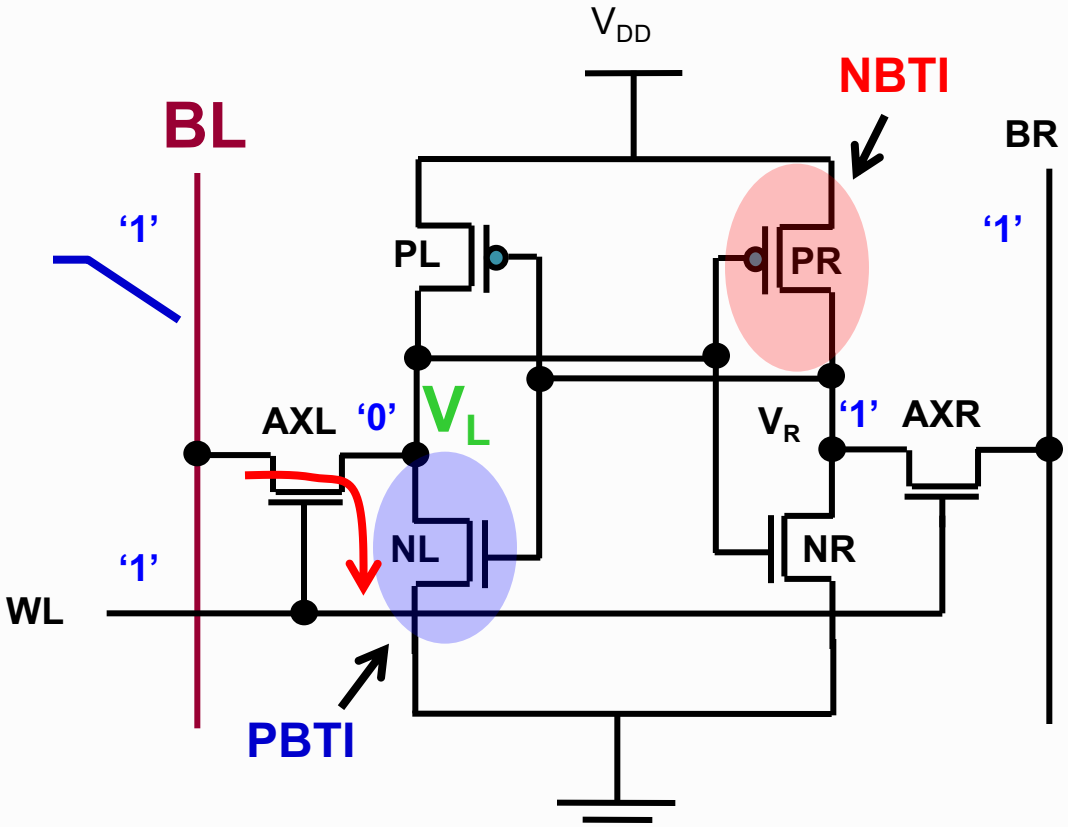
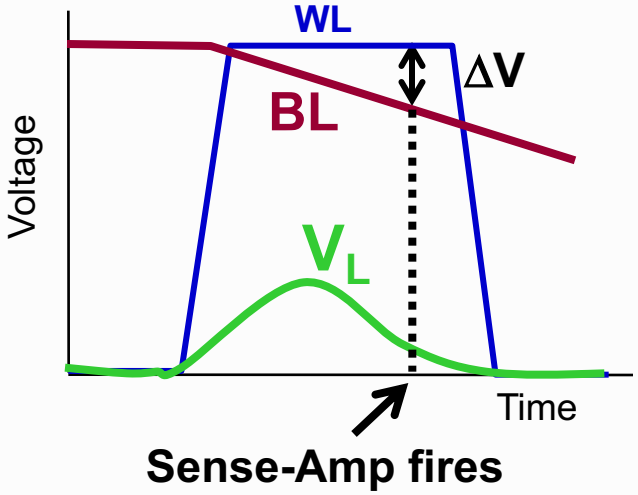
Timing Failure due to BTI



SRAM Operating Mode: READ



BL and BR are pre-charged to VDD and then left hanging

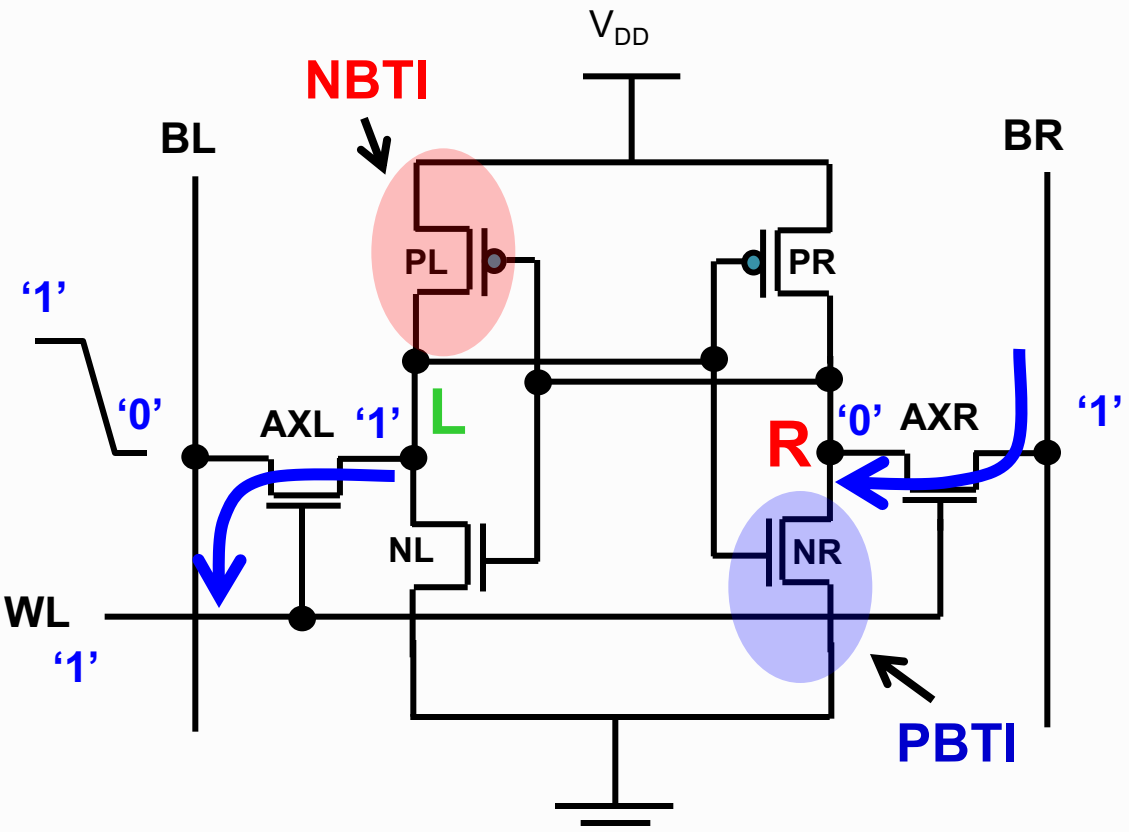


Access FETs (AXL & AXR) are ON for short duration while cell is accessed => assumed negligible degradation

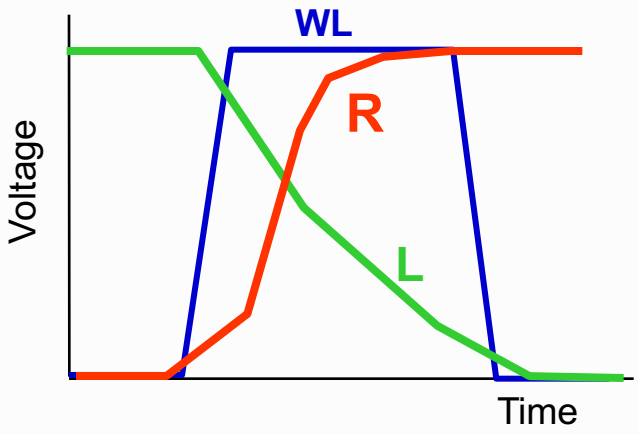
- **The data stored should *not* flip during READ**
  => NL (NR) should be stronger than AXL (AXR): *PBTI can make NL weak (bad!)*
- **Sufficient ΔV to fire SA should be developed while WL = '1'**
  => AXL-NL should fast discharge BL: *Weak NL will slow discharge (bad!)*

(A. Bansal, MicroReliability 2009)

SRAM Operating Mode: WRITE



BL and BR are FIXED to data



Weak cross-coupled inverters (NL-PL and NR-PR) are good for writing

- **The data stored *must* flip during WRITE**

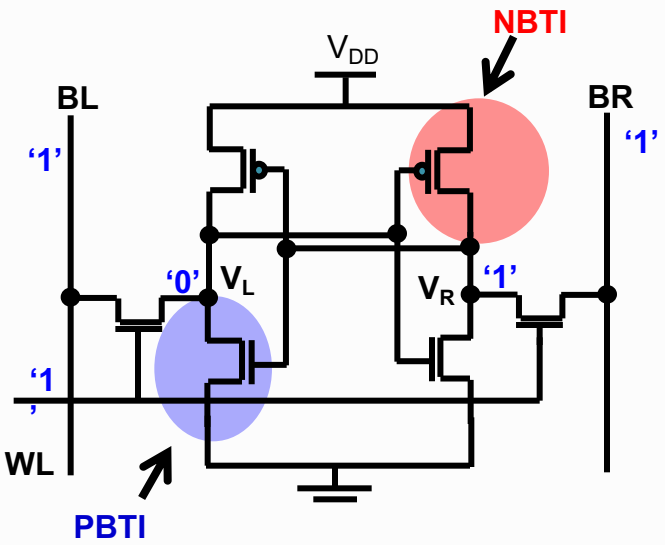
=> AXL (AXR) should be stronger than PL (NR) *NBTI (PBTI) can make PL (NR) weak (good!)*

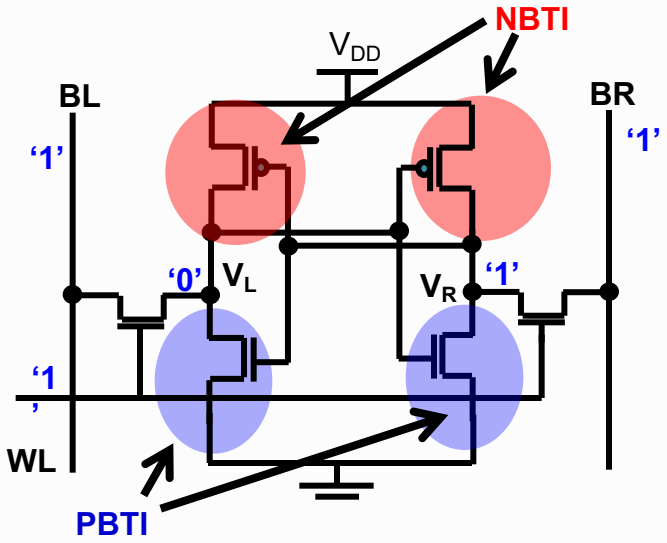
- **Data should flip while WL = '1'**

=> *WL pulse width increased (good)*

(A. Bansal, MicroReliability 2009)

Static and Alternating Stress





Static Stress

- Cell is storing same data for long time => asymmetric
- May be *READ* multiple times but not flipped
- ΔVt for static stress larger than alternating stress (no recovery)
- READ gradually becomes unstable
- Increases READ access time

Alternating Stress

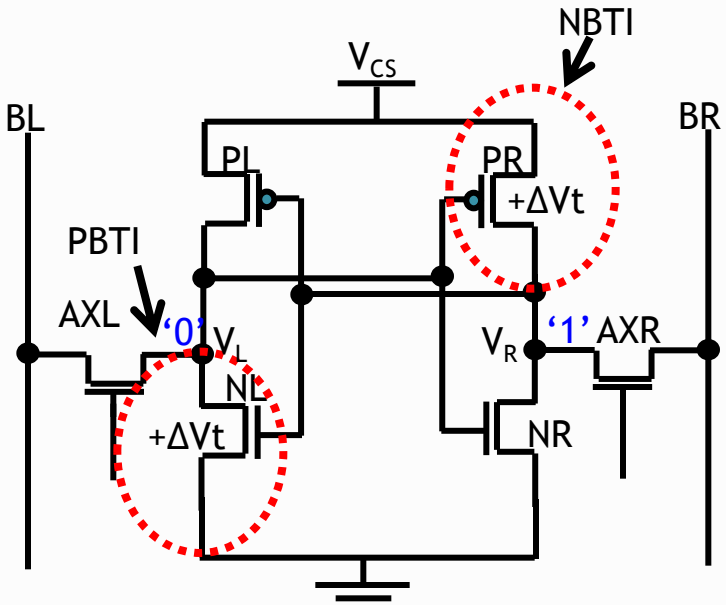
- Cell is regularly flipped => symmetric
- Equal time/relaxation for storing '1' and '0' to maintain symmetry
- ΔVt for same usage is less (low power-on time)
- β-ratio between pull-down and pass-gate FETs varies => PD weakens and READ fail increases
- Increases READ access time

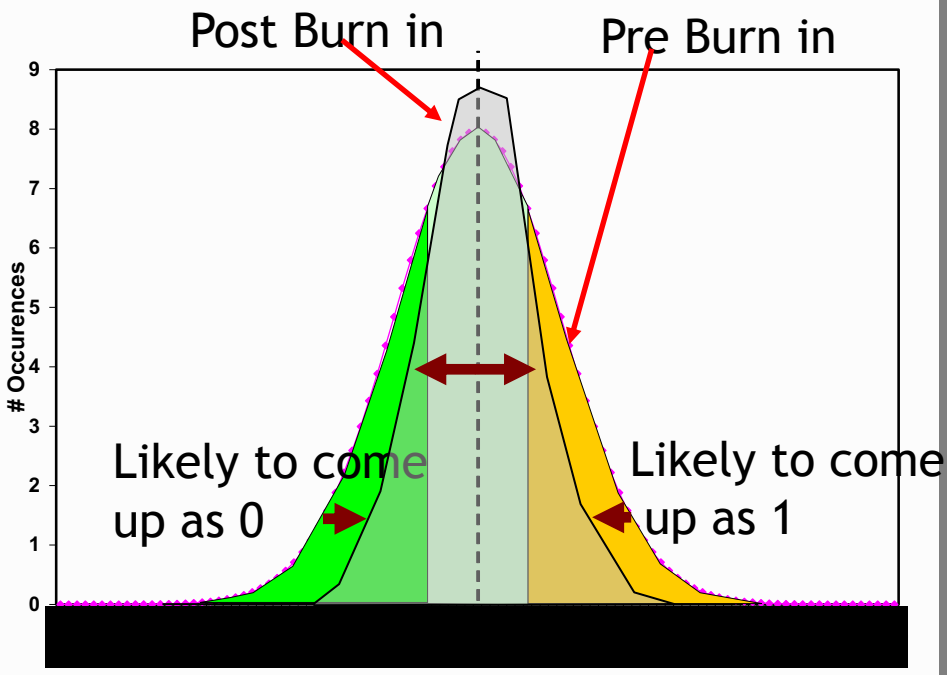
➢ **Typically all cells in between Static to Alternating stress**

(A. Bansal, MicroReliability 2009)

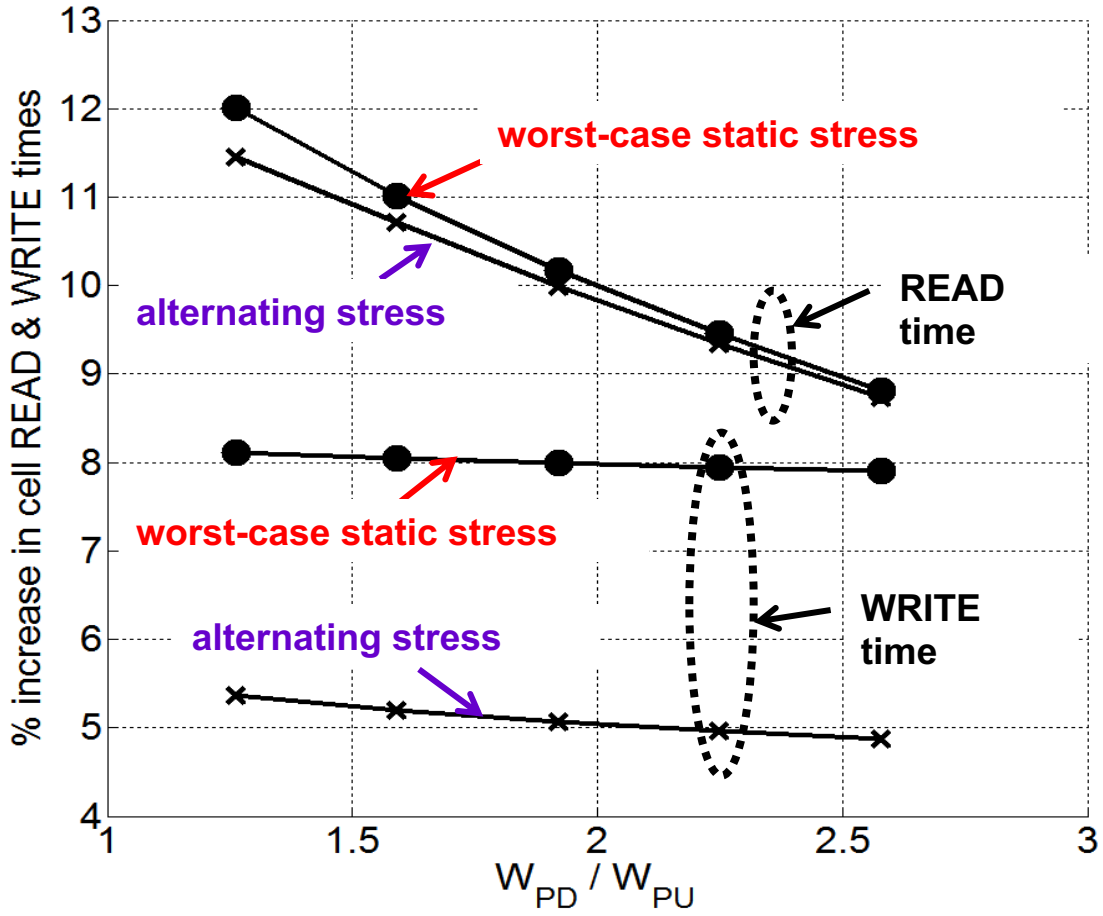
Unbalanced Post-Fabrication SRAM Cells

- Unbalanced cells result in uneven squares in butterfly curve => Reduced noise margin
- Read performance on different read ports become different (in case of single ended read / 8T cells)
- Bring up state:
  - V_L = 0, NL-PR pair is stronger than PL-NR pair
- Pre-condition sram cell state before burn in (depending on stability or performance need)
  - Burn – in with V_L = 0
- Duration of 'conditional' stress can be based on spread of the initial curve
  - Or by # of 1s / 0s in the initial bring up





Impact on Cell READ and WRITE time

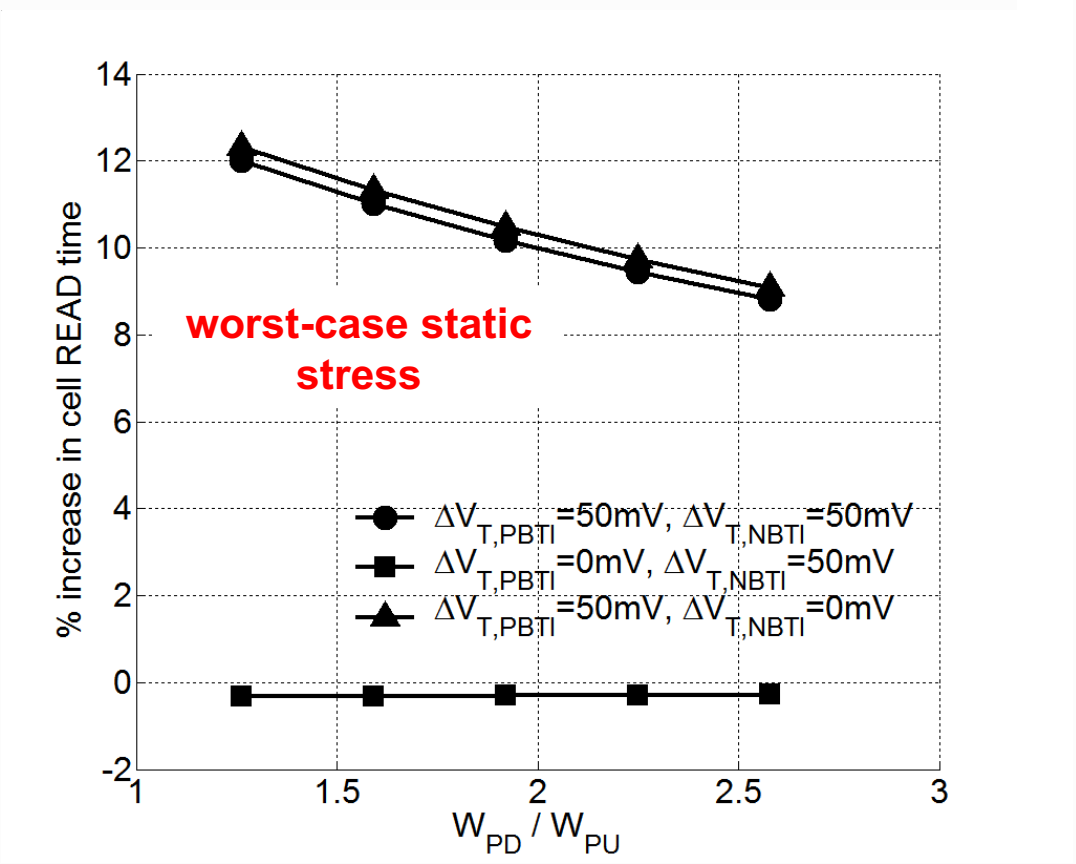


Assuming $\Delta V_T = 50mV$ increase due to NBTI and PBTI at end-of-life

- **READ time reduces as we go from dense to high-performance cell**
- **READ time is *less* dependent on stress condition**

(A. Bansal, IRPS 2009)

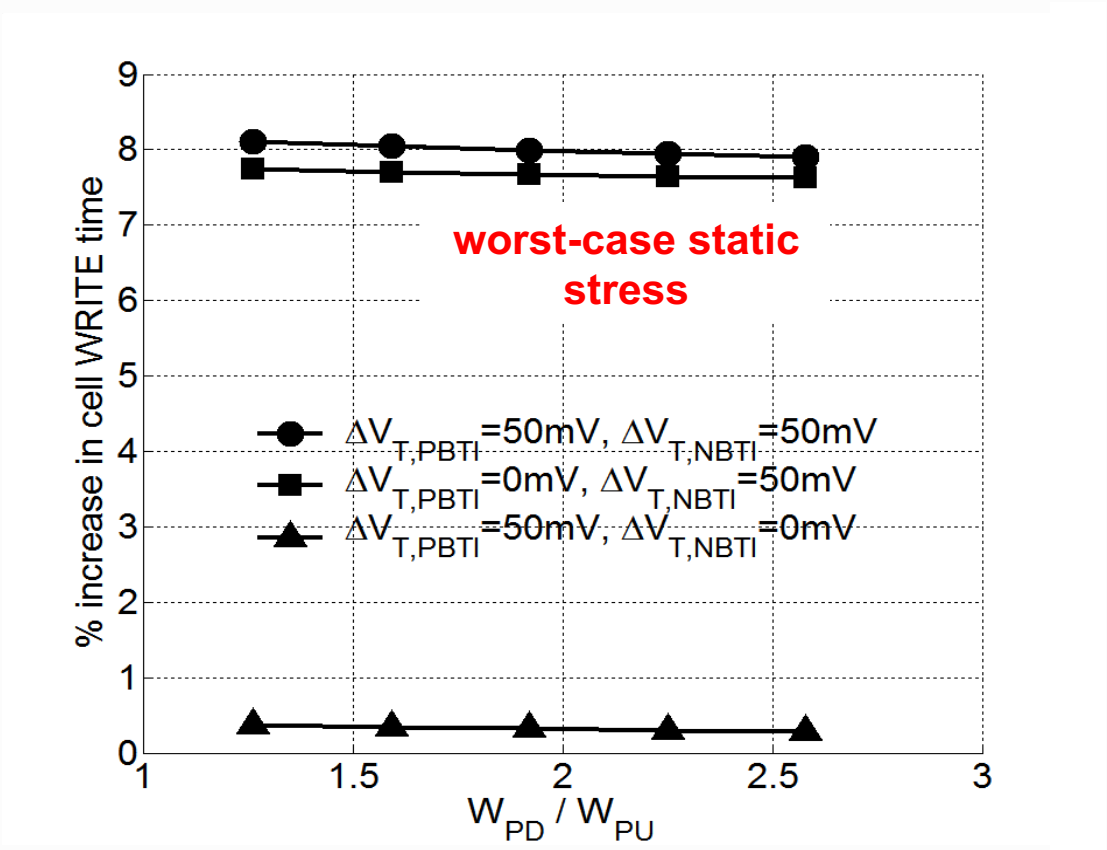
READ access time



- **READ time is *practically immune* to NBTI**
- **READ time degrades ~ 9-12% for 50mV V_T shift due to PBTI**
- ***Stringent PBTI requirements in high-performance cells***

(A. Bansal, IRPS 2009)

WRITE time



- **WRITE time is *practically immune* to PBTI**
- **WRITE time degrades ~ 8% for 50mV V_T shift due to NBTI**
- ***Similar NBTI requirements in high-performance and dense cells***

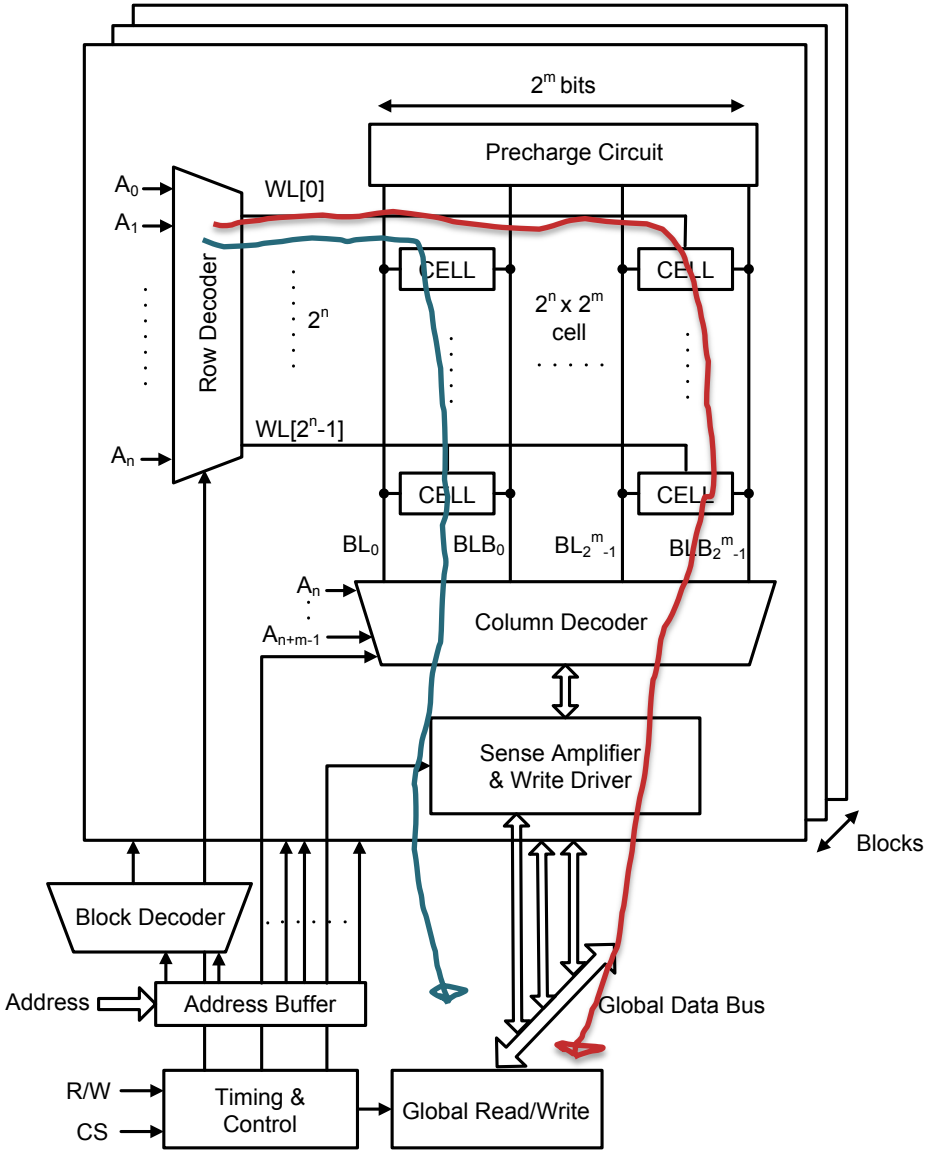
(A. Bansal, IRPS 2009)

Hot Carrier Injection

- The impact of HCI

a) Is more on access transistors than the pull down and pull up transistors
b) Is more on word-line overdrive (WLOD) assisted cells
c) Is higher on frequently written cells than frequently read cells
d) Improves the read access time of 8T cells

Block Diagram



Power Computation

- Apply sequence of patterns aimed at separating power components
  - Initialize array with equi probable 0s and 1s (make A0 = all 0s)
  - Hold operation (P_H) => Leakage + Clock power
  - Write all 0s to Address A0 (P_{w0}) => Power of a write where no cells is actually written => Power of address decode + write drivers (peripherals)
  - Read from Address A0 (P_{r0}) => Should read all 0s, i.e all bit-lines will discharge (in a single ended read scenario)
  - Write 111 to Address A0 (P_{w1}) => Power of a write operation where N cells are actually written
  - Read from address A0 (P_{r1}) => Power of a read operation where no bit lines will discharge (in a single ended read scenario)
  - Vary addresses to get power of decoders

- Power of a write operation where N of M bits actually flip = $P_H + P_{w0} + (P_{w1} - P_{w0})*N/M$

Test

Test

❑ Defect vs Fault

- Defect => A deviation from intended behavior
- Fault => A model for the defect

❑ Structural vs Functional Test

- Structural Test => Testing all nodes of the circuits
- Functional Test => Behaves as desired

❑ Verification vs Test

- Verification => Design is correct
- Test => Hardware is correct

Test

- Stuck At Faults => Cell is stuck at a particular value
- Transition Faults => Cell fails to undergo a particular transition
- Coupling Faults => Cell (v) fails due to Cell (a)
- Pattern Faults => Cell (v) fails due to a multiple set of Cells (a1 – an)

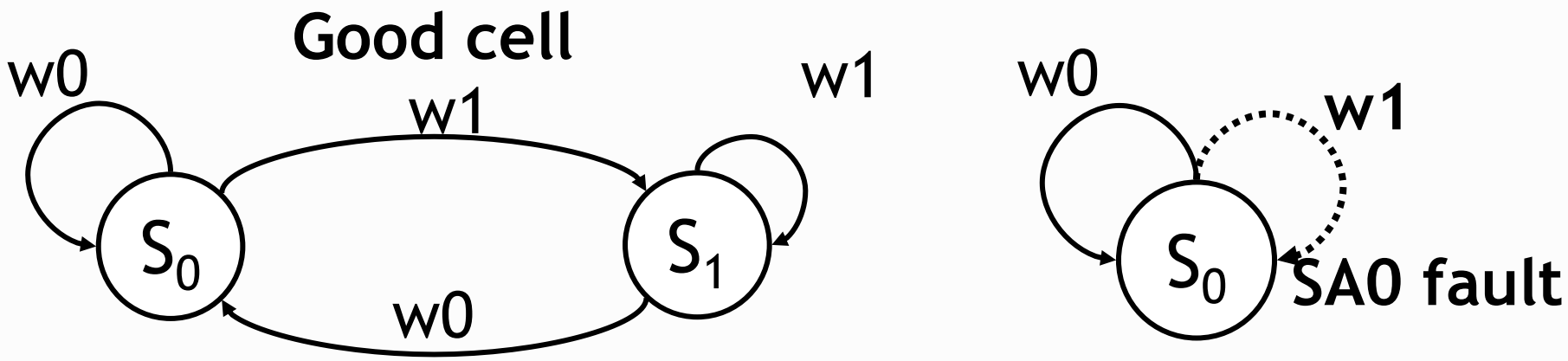
Fault Notation

- <…> describes a fault
- <*S*/*F*> describes a *single-cell fault*
  - *S* describes the state/operation *sensitizing* the fault
    - A fault is sensitized when the fault effect is made present
  - *F* describes the *fault effect* in the *victim cell* (v-cell)
- <*S*;*F*> describes a *two-cell fault* (a Coupling Fault)
  - *S* describes the state/operation of the *aggressor cell* (a-cell) sensitizing the fault
  - *F* describes the fault effect in the v-cell

- Examples
  - <∀/0>: a SA0 fault
  - <∀/1>: a SA1 fault
  - <↑/0>: an ↑ TF
  - <↓/1>: a ↓ TF
  - <↑;0>: a CF
  - <↑;1>: a CF
  - <↓;0>: a CF
  - <↓;1>: a CF

Stuck Faults

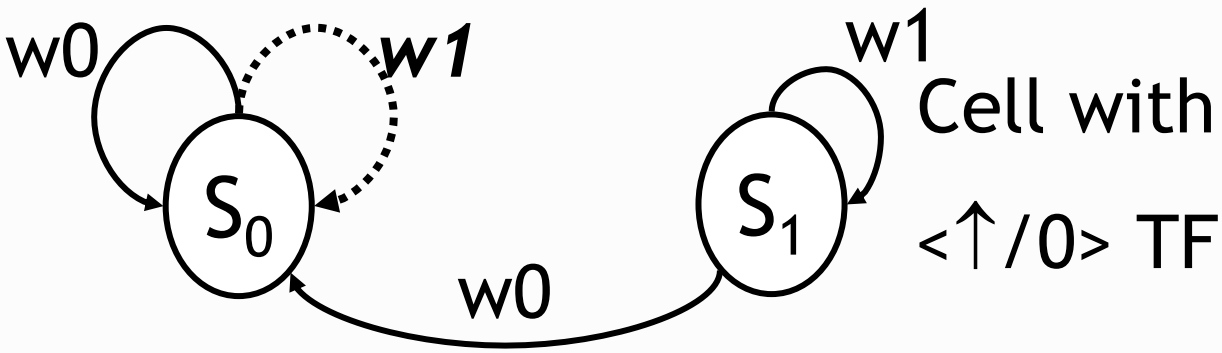
- Stuck At Faults => Cell is stuck at a particular value



- Stuck at Open Fault
  - e.g Word line is broken => When read is performed both BL and BLB remain high

Transition Fault

❑ Transition Faults => Cell fails to undergo a particular transition

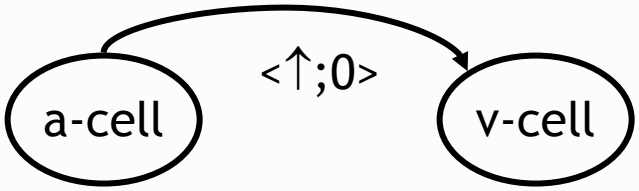


Test: All cells should have a ↑ and ↓ transition and read

❑ Retention Faults => Cell loses value after a while

Coupling Faults

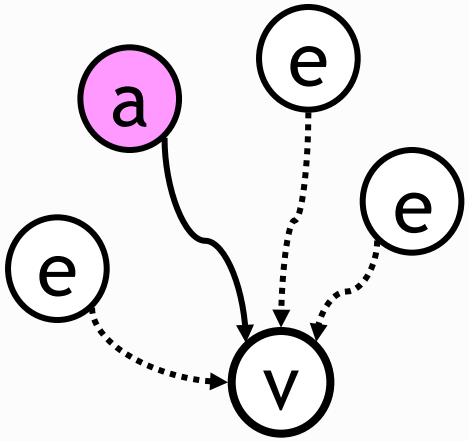
- Coupling Faults => State (or Transition) of Cell A causes a failure in Cell V



- Coupling Transition Faults: <↑;0>, <↑;1>, <↓;0> and <↓;1>
- Coupling state faults: <1;0>, <1;1>, <0;0> and <0;1>
- Coupling inversion fault: <↑;↕> and <↓;↕>

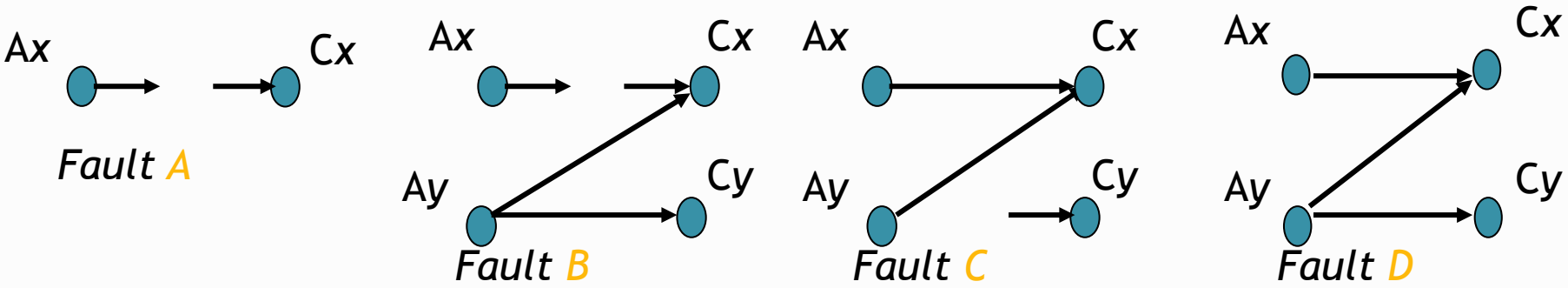
Pattern Sensitive Faults

- The state (transition) or K cells causes a failure in an ith cell
  - NPSF => The k cells are adjacent



Address Faults

- Address (A1) cause no cell to be accessed
- Address (A1) accesses multiple cells
- Cell (C1) is accessed with multiple addresses
- Cell (C1) is accessed by its own and another address



March Tests

- A sequence of operations applied in a particular order aimed at targeting the various fault models
- March C

{⇕(w0);⇑(r0,w1);⇑(r1,w0);⇕(r0);⇓(r0,w1);⇓(r1,w0);⇕(r0)}

- Intermediate r0 shown to be redundant => March C-

{⇕(w0);⇑(r0,w1);⇑(r1,w0);⇓(r0,w1);⇓(r1,w0);⇕(r0)}

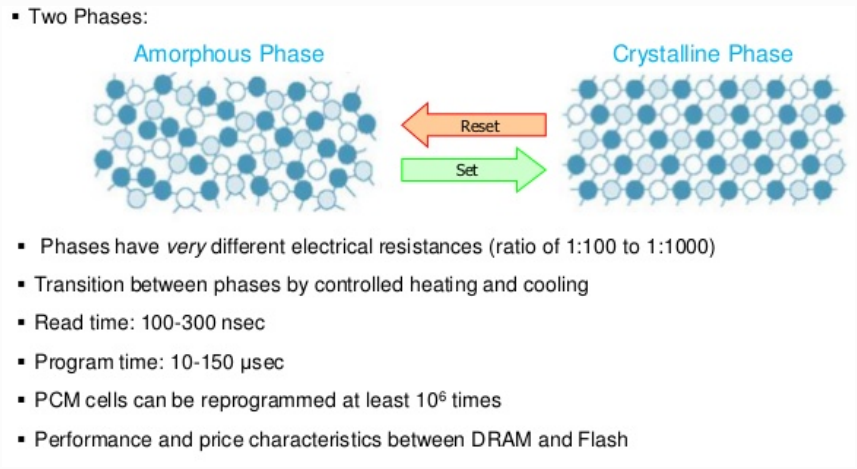
Memory Technology Comparison

	SRAM	DRAM	Flash (NOR)	Flash (NAND)	FeRAM	MRAM	PRAM	STT-RAM
Non-volatile	No	No	Yes	Yes	Yes	Yes	Yes	Yes
Cell size (F^2)	50–120	6–10	10	5	15–34	16–40	6–12	6–20
Read time (ns)	1–100	30	10	50	20–80	3–20	20–50	2–20
Write / Erase time (ns)	1–100	50 / 50	1 µs / 10 ms	1 ms / 0.1 ms	50 / 50	3–20	50 / 120	2–20
Endurance	10^{16}	10^{16}	10^{5}	10^{5}	10^{12}	$>10^{15}$	10^{10}	$>10^{15}$
Write power	Low	Low	Very high	Very high	Low	High	Low	Low
Other power consumption	Current leakage	Refresh current	None	None	None	None	None	None
High voltage required	No	2 V	6–8 V	16–20 V	2–3 V	3 V	1.5–3 V	<1.5 V
	Existing products						*Prototype*	

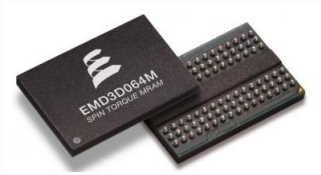
Source: Grandis Corporation, 2008

Emerging Memory Technologies

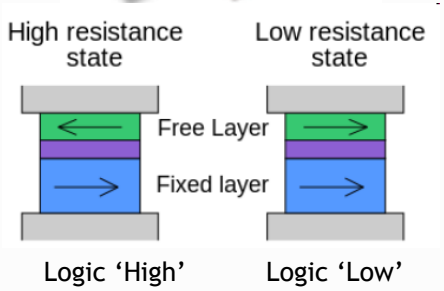
- PCRAM (Phase-Change RAM)
  - Medium Performance
  - Storage Class Memory
  - Apply current to change material phase & measure R by phase



- STT-MRAM (Spin Transfer Torque RAM)
  - DRAM alternatives/embedded MRAM
  - Expensive
  - Apply current to change magnet polarity & measure R by polarity

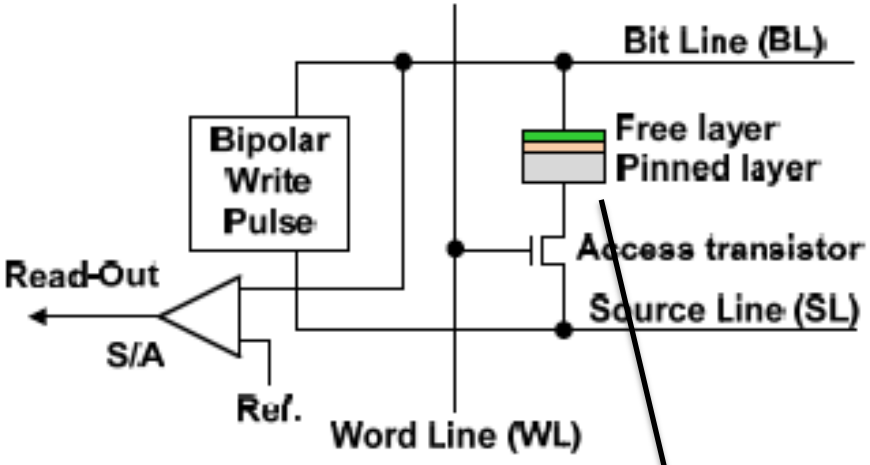


- ReRAM (Resistive RAM)
  - Medium Performance
  - Storage Class Memory
  - Apply current to change atomic structure & measure R by atom distance

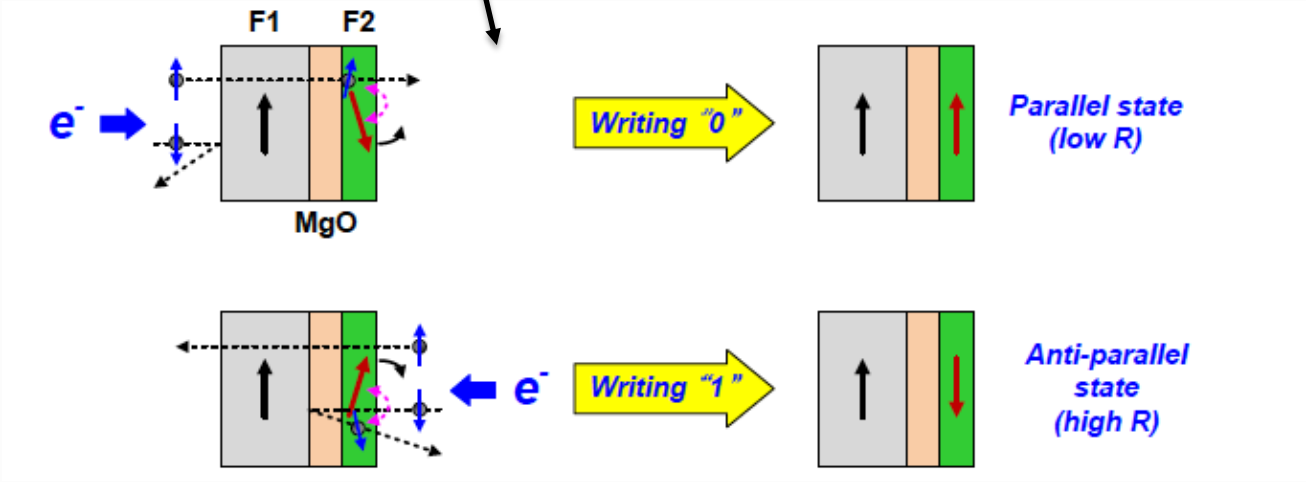


Courtesy: S. Sethuraman, IBM

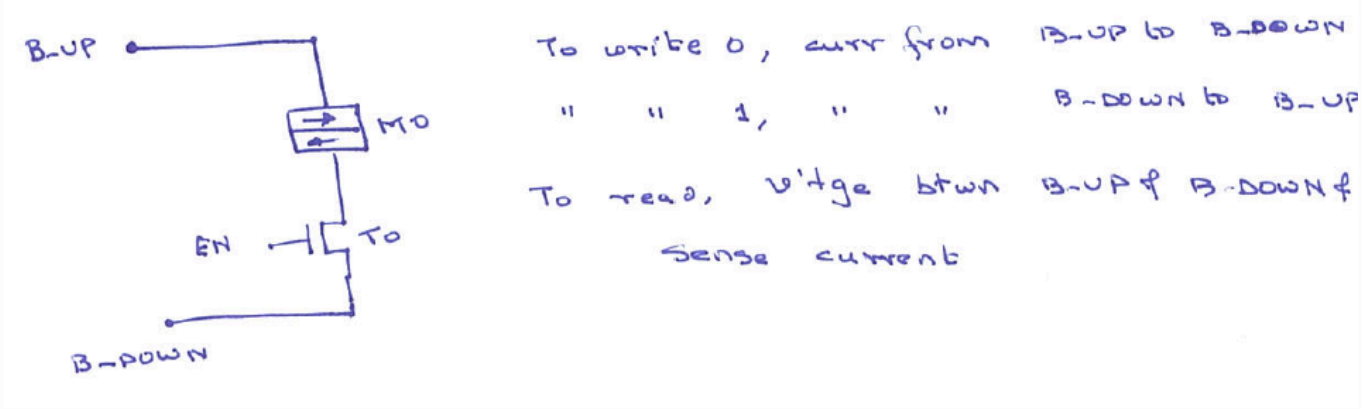
STTRAM cell

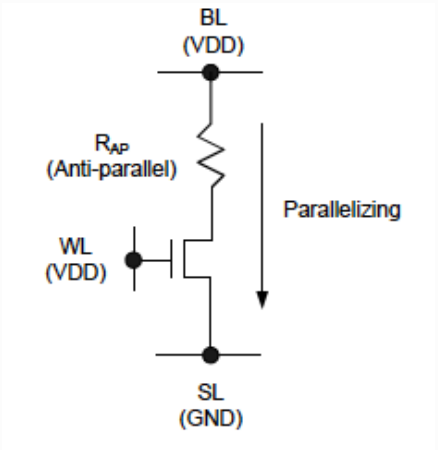


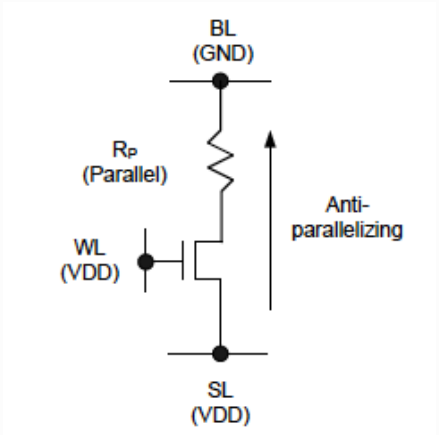
M. Hosomi et al, IEDM05, Sony



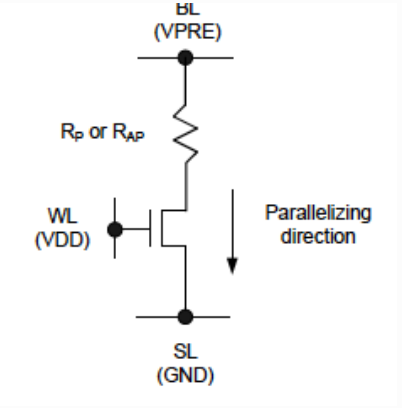
STTRAM cell

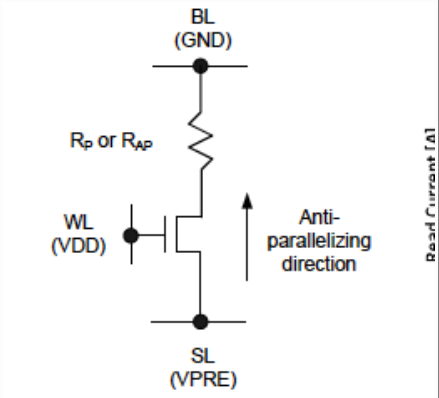






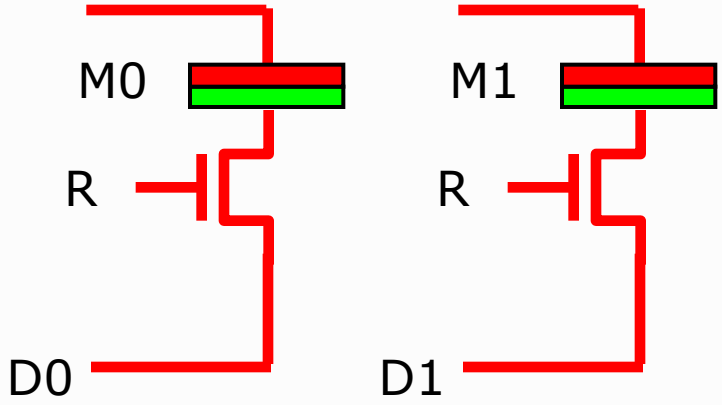
Write



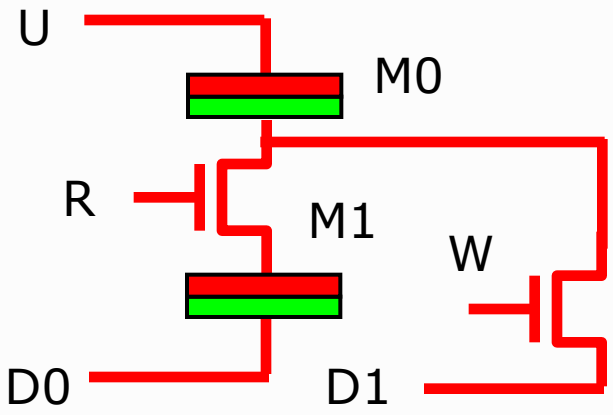


Read

Merged MTJ cells with logic



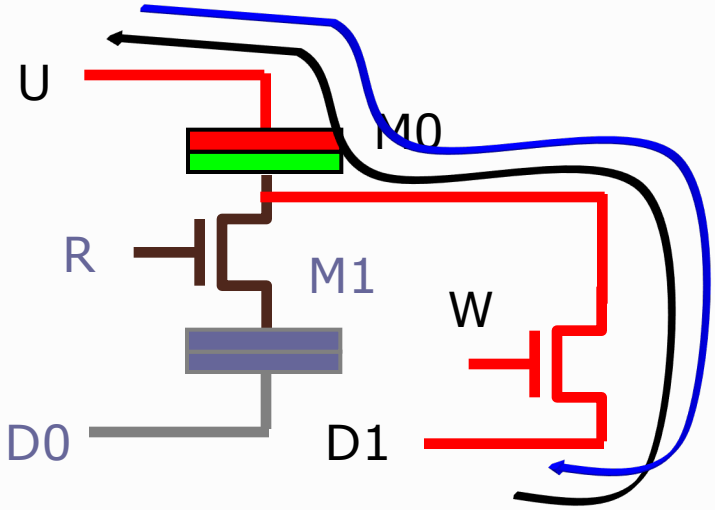
Independently read each cell (MTJ)
Independently write each cell (MTJ)
Cannot read the combination of both cells



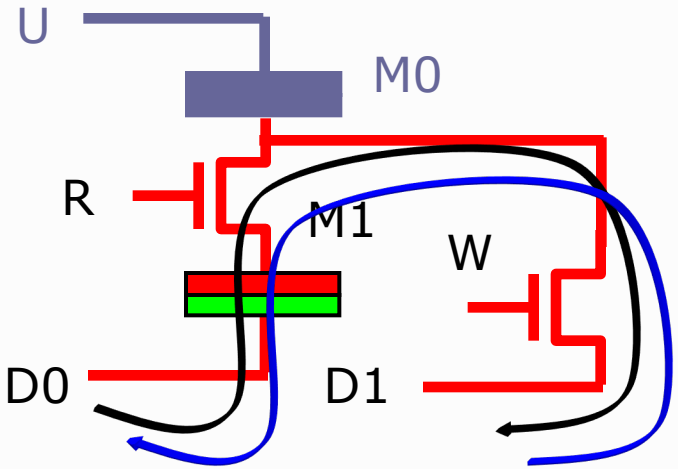
Can independently write to each cell (MTJ)
Can independently read each cell (MTJ)
Can read the combination of both cells

Write operations

Write M0

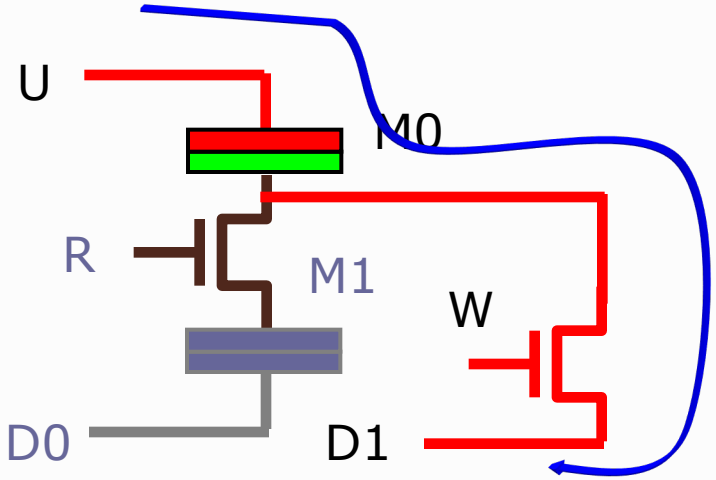


Write M1

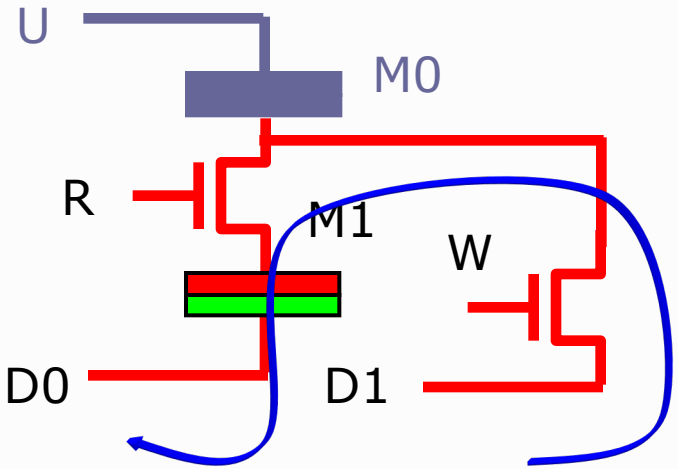


Read operations (individual cells)

Read M0

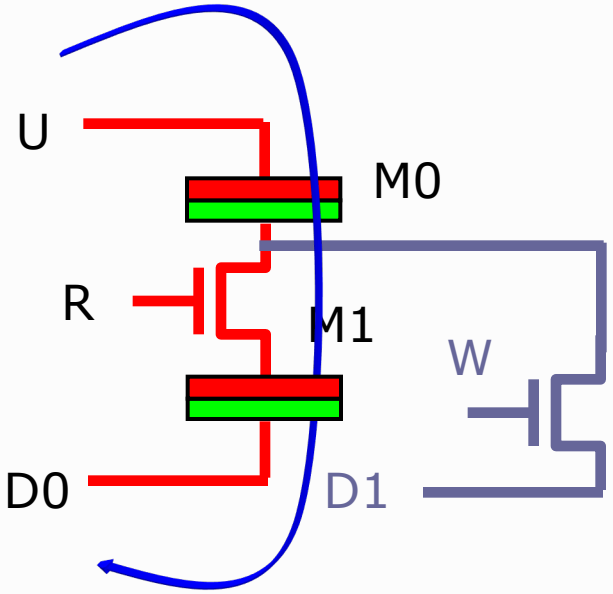


Read M1



Read combination

Read (M0 = 0 and M1 = 0)



Variation Characterization

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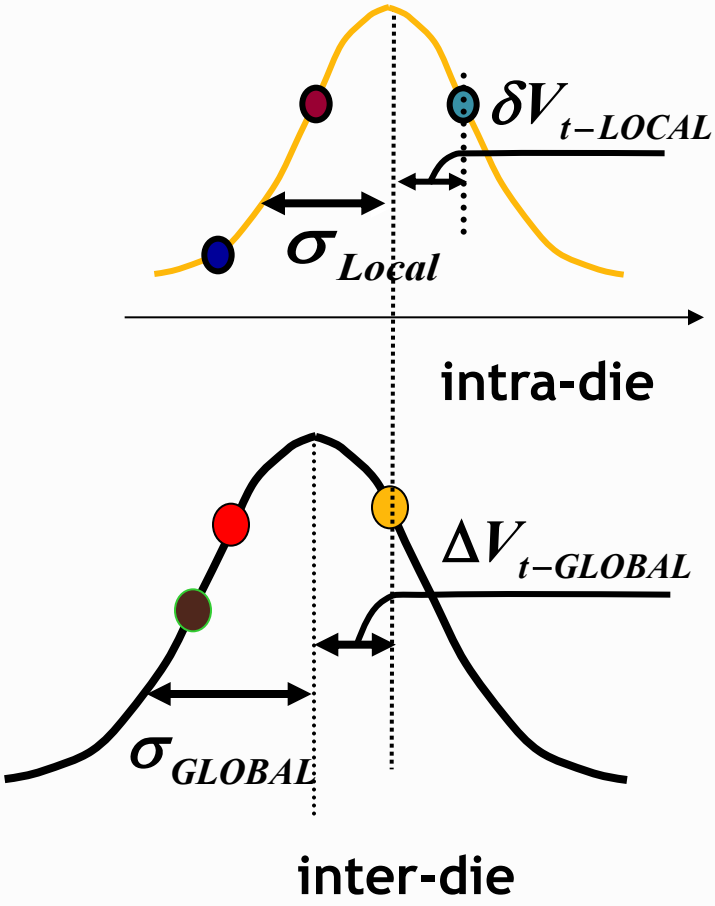
Characterization Circuits

- Process Characterization
  - Understand effect of different process steps
  - Characterize extent and impact of various effects
  - Feed back to modeling and technology team
  - Guidelines for good topologies, design styles
  - Examples
    - Array of Devices for I-V Characterization
    - Local vs Global Variation Sensors
    - NBTI / PBTI Isolation Circuits
- Mature Process
  - Topologies to ensure that process is well behaved
  - Process corner detection circuits for static compensation
  - Dynamic (on-line) characterization for adaptive systems
  - Sensors for debug of failure mechanisms
  - Examples
    - Critical Path Monitors / Skitter Circuits
    - Slew Monitor
    - In-situ Power Monitor

Characterization Challenges

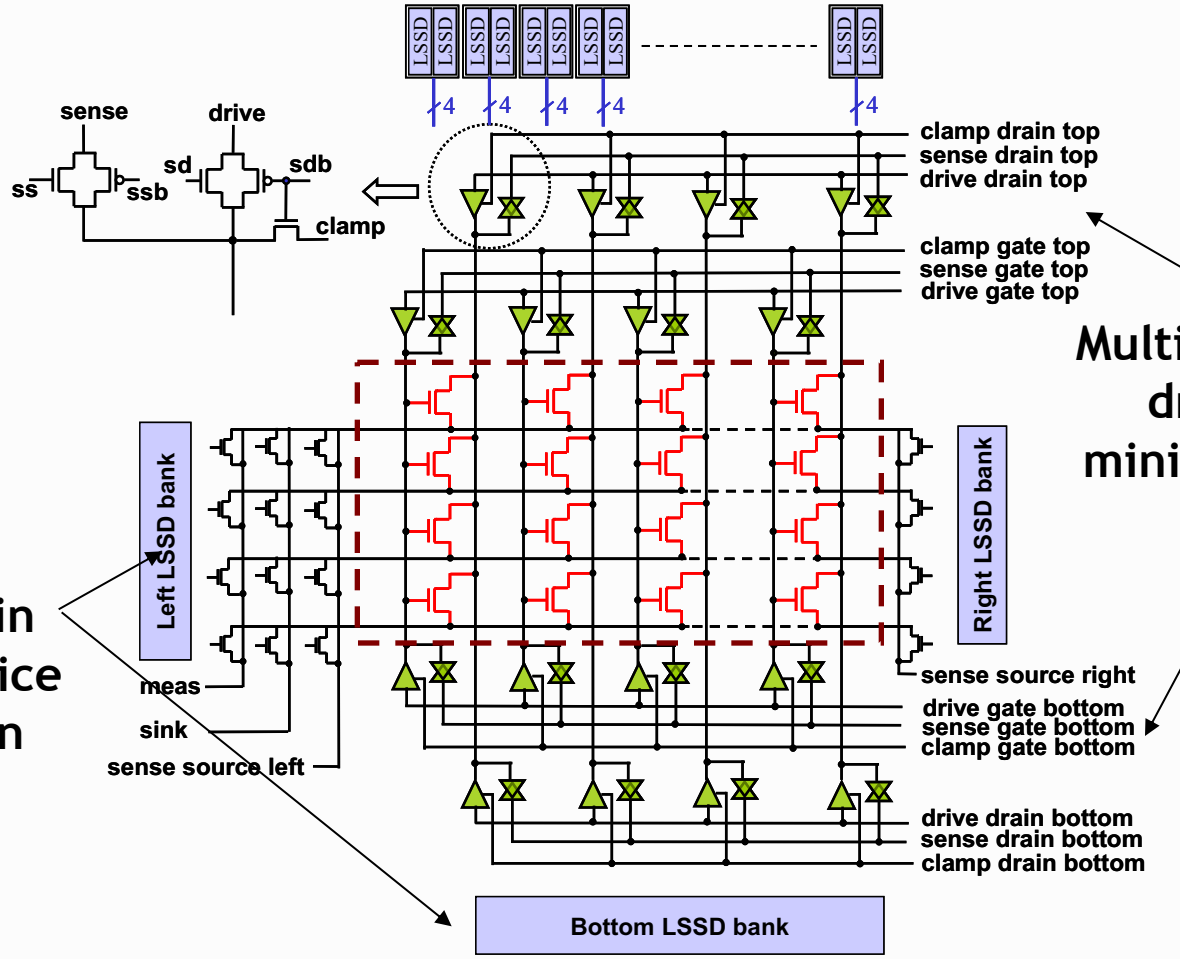
- Limited silicon and characterization resources
- I-V Characterization Simplifications
  - Limited physical configurations (neighborhood/density, stress-related geometries, device sizes)
  - Limited operating conditions (voltage, history, self-heating)
  - Sampling of manufactured devices
  - Snapshot of process and lifetime

Global vs Local Characterization



- Local Variation Sensors
  - Eliminate the influence of global and systematic variations that effects all devices equally
  - Minimize noise due to common environmental factors
- Methods
  - I-V measurements
  - Measuring digital signatures of analog variations
  - Measurement of mismatch and measurement of individual device variations

Array Based I-V Characterization Circuits



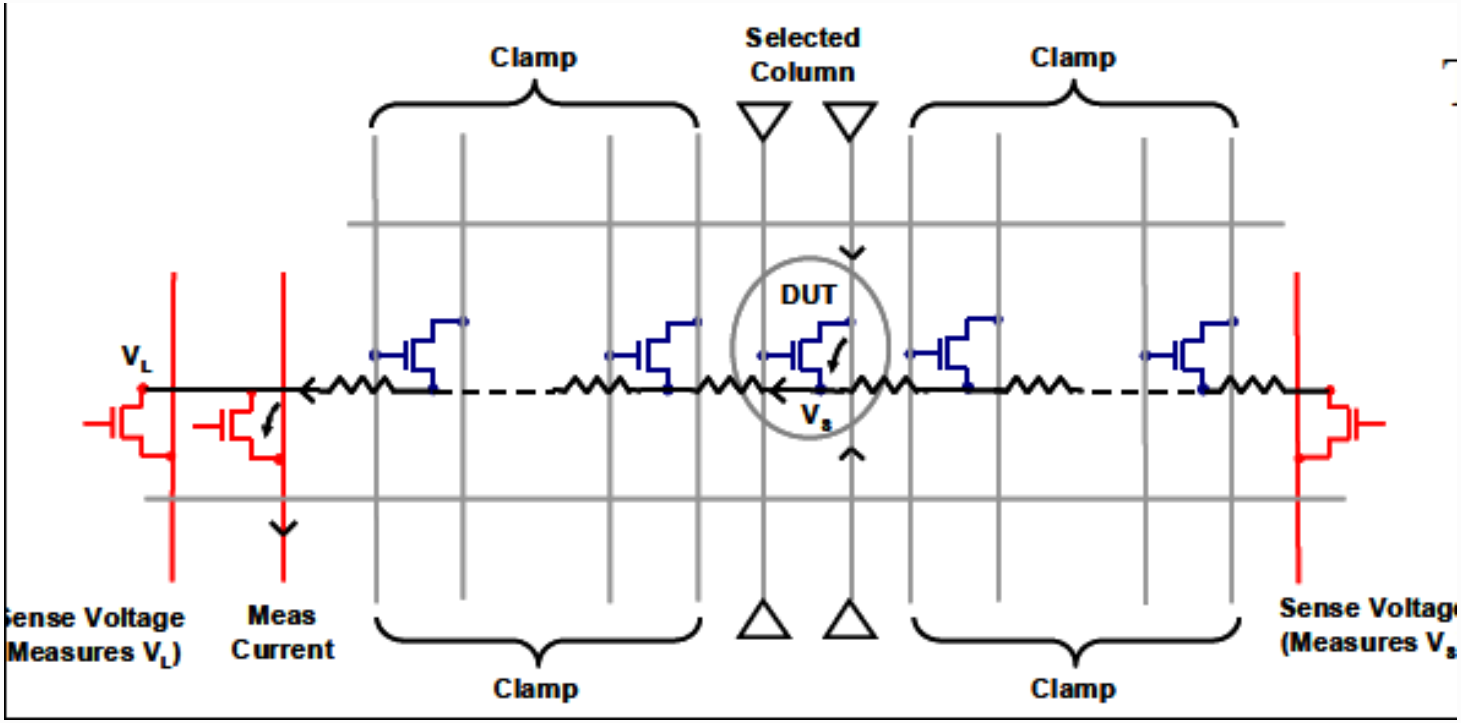
Multiple Gate – Drain drive nodes to minimize resistance effects

Scan chain based device selection

- Measure I-V of devices in an array
- Extract Vt mismatch from “current difference” between identical transistors

K. Agarwal, et. al. DAC 2007

Array Based I-V Characterization Circuits



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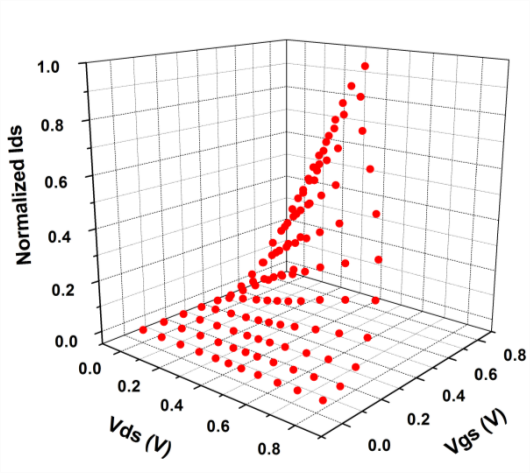
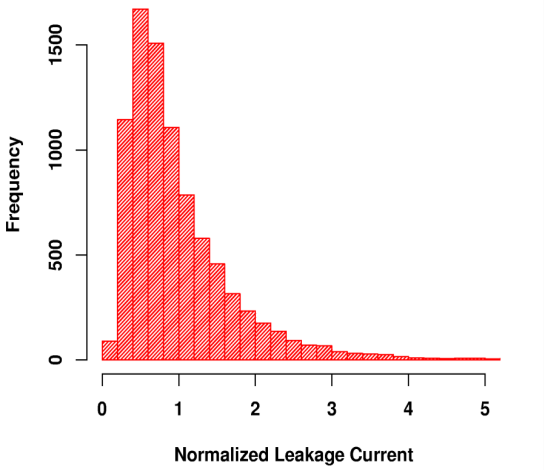
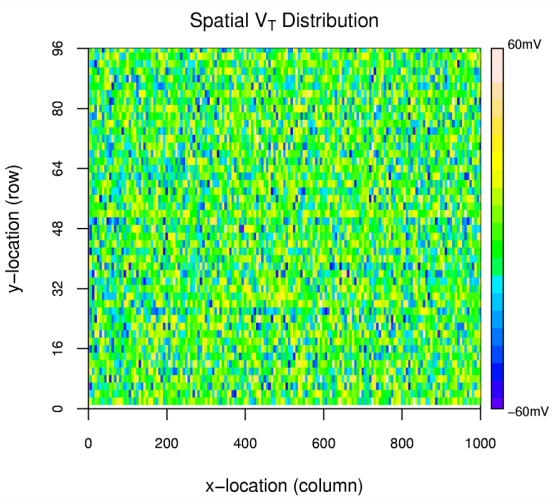
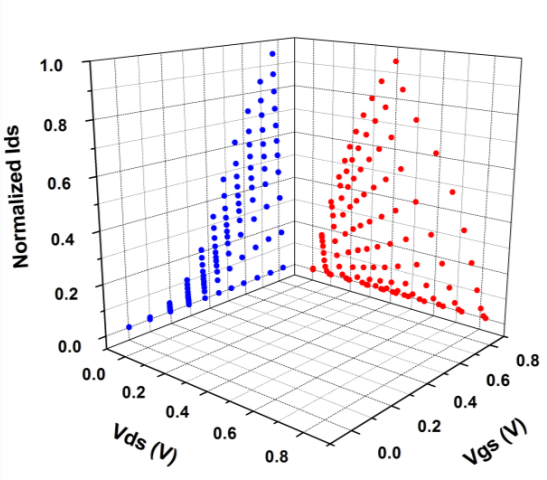
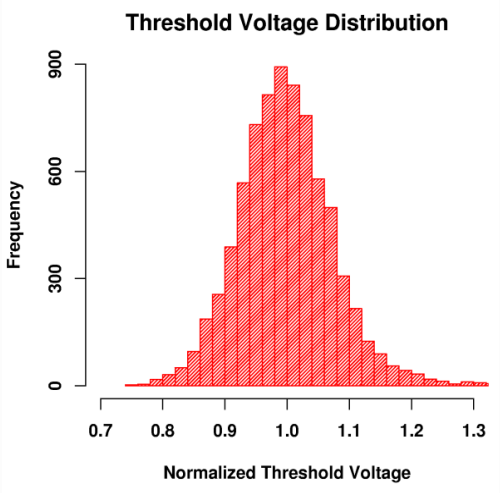
Array Based I-V Characterization Circuits

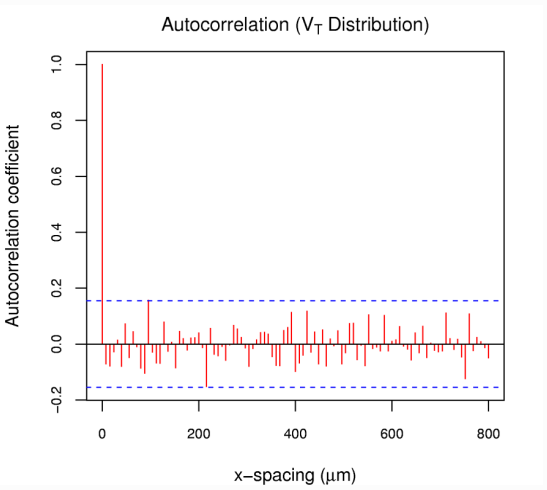












Sample I-V curves

Parameter Distributions

Spatial Correlation

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