Advanced Topics in VLSI

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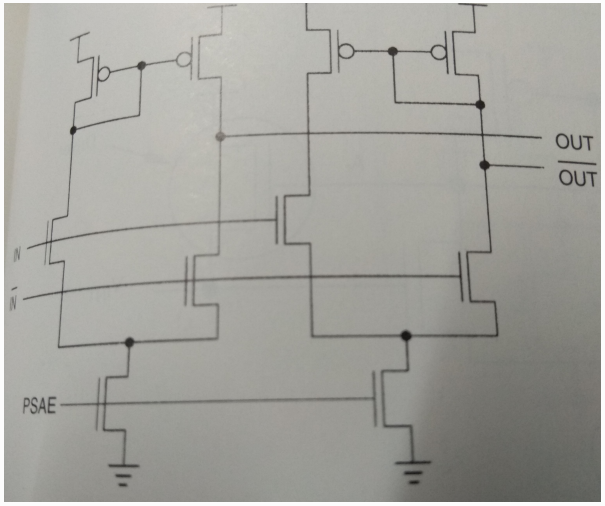
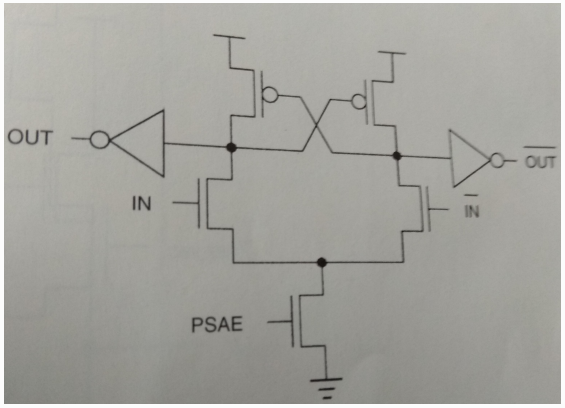
Sense Amplifiers (Alternate)



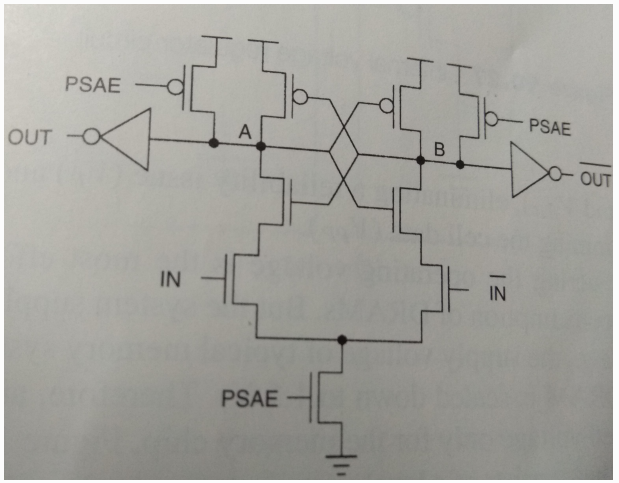
Current Mirror Based

Common mode rejection ratio



Half Latch Based

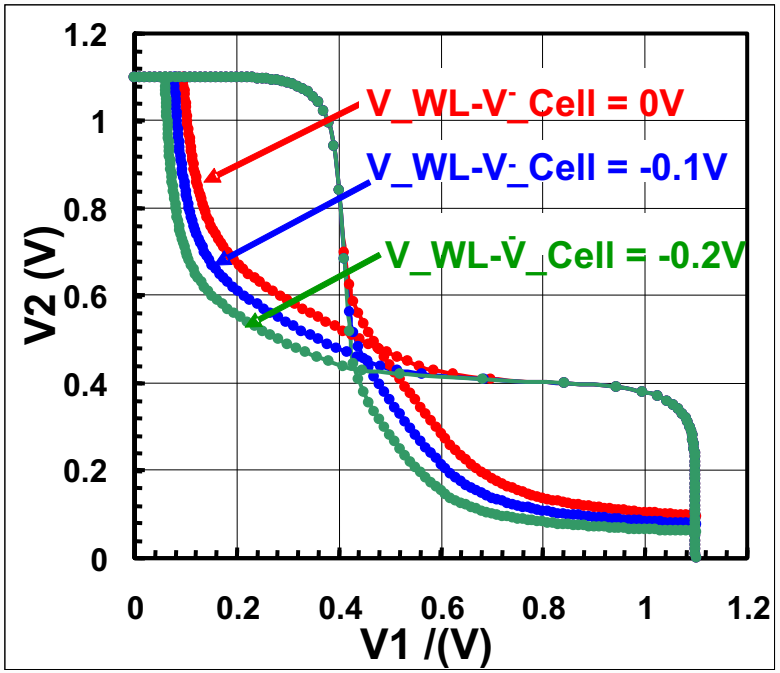
Compactness, semi performance

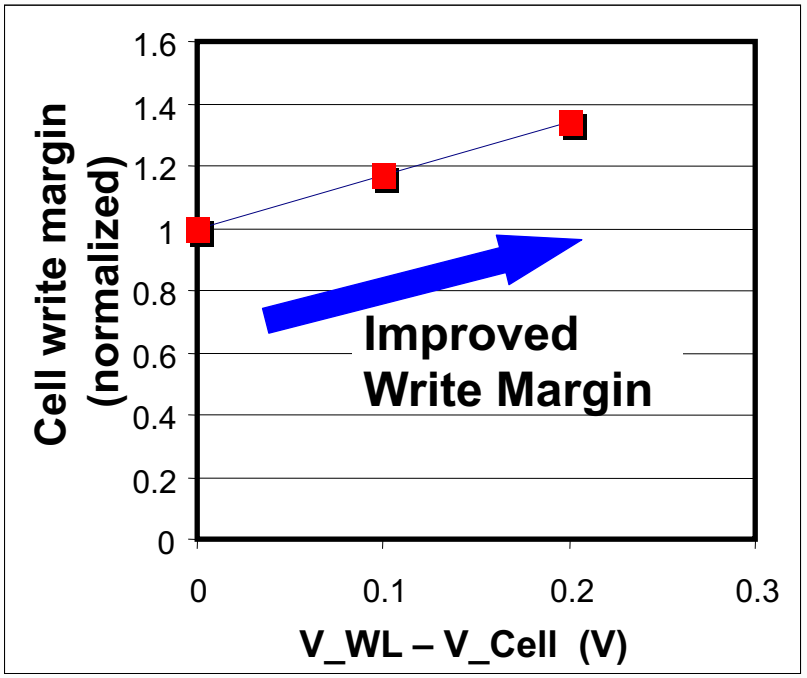


Full Differential

Full swing + performance

Example: Multi-VCC for SRAM Cell

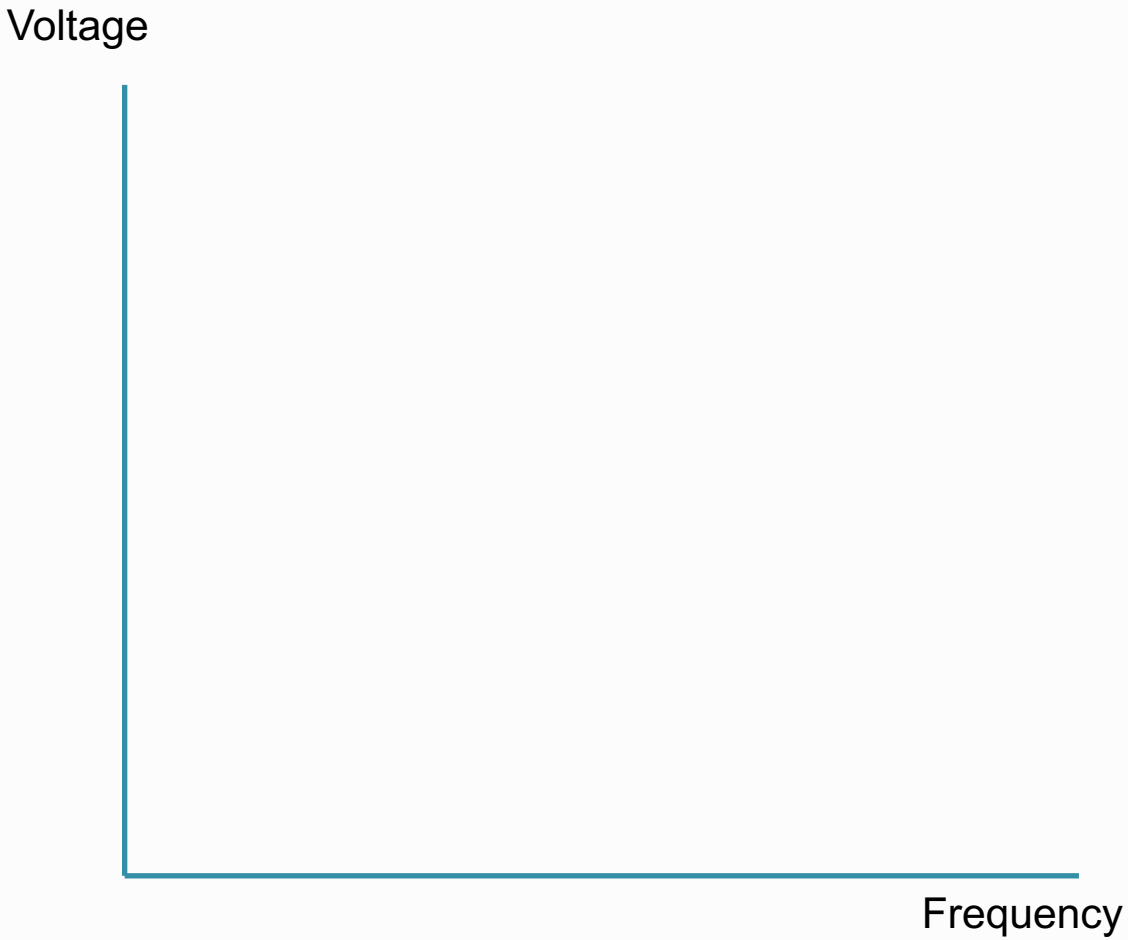




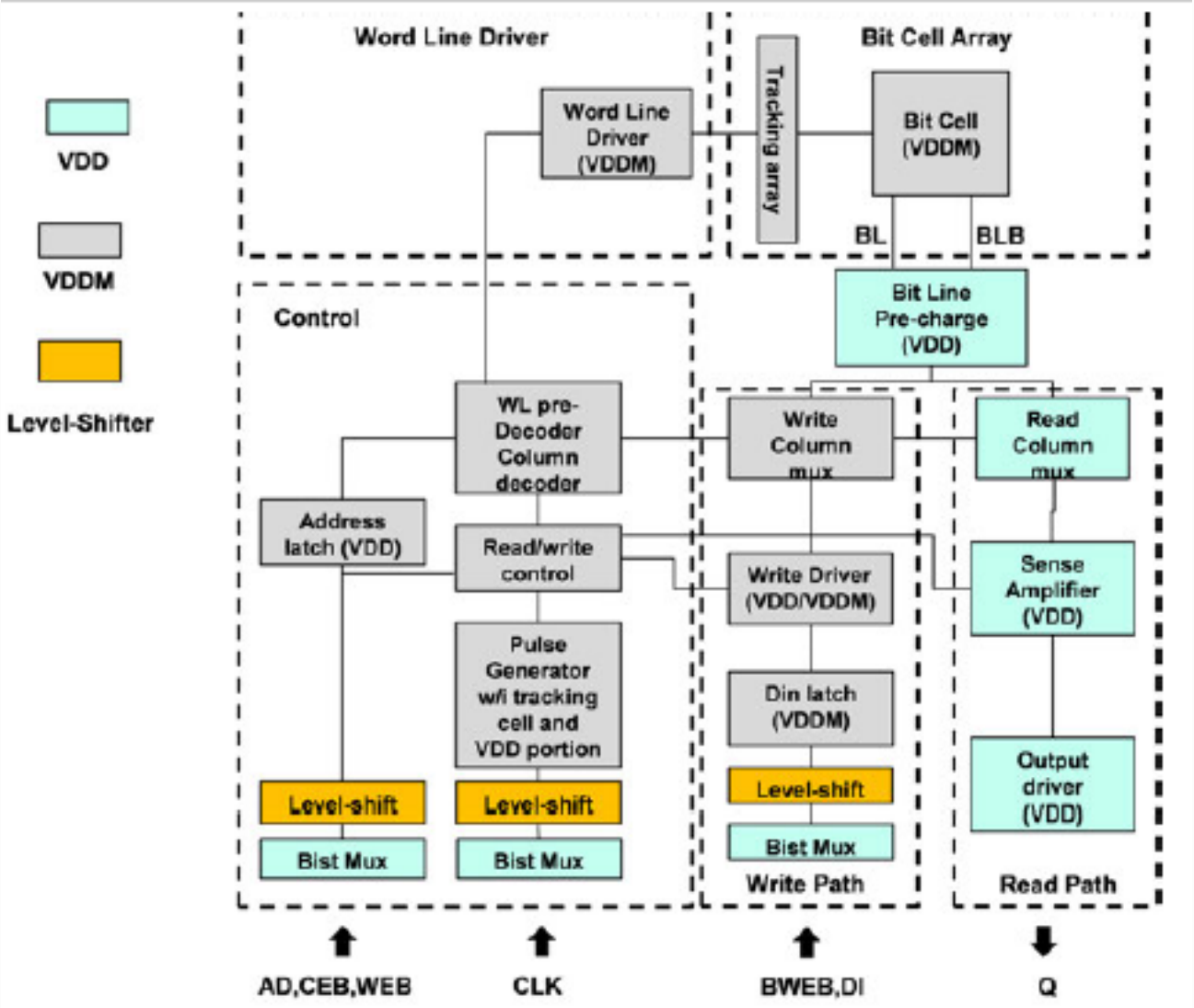
- Create differential voltage between WL and Cell to decouple the Read & Write
  - Write: V_WL > V_Cell
  - Read: V_WL < V_Cell

Source: K. Zhang et. al. ISSCC 2005

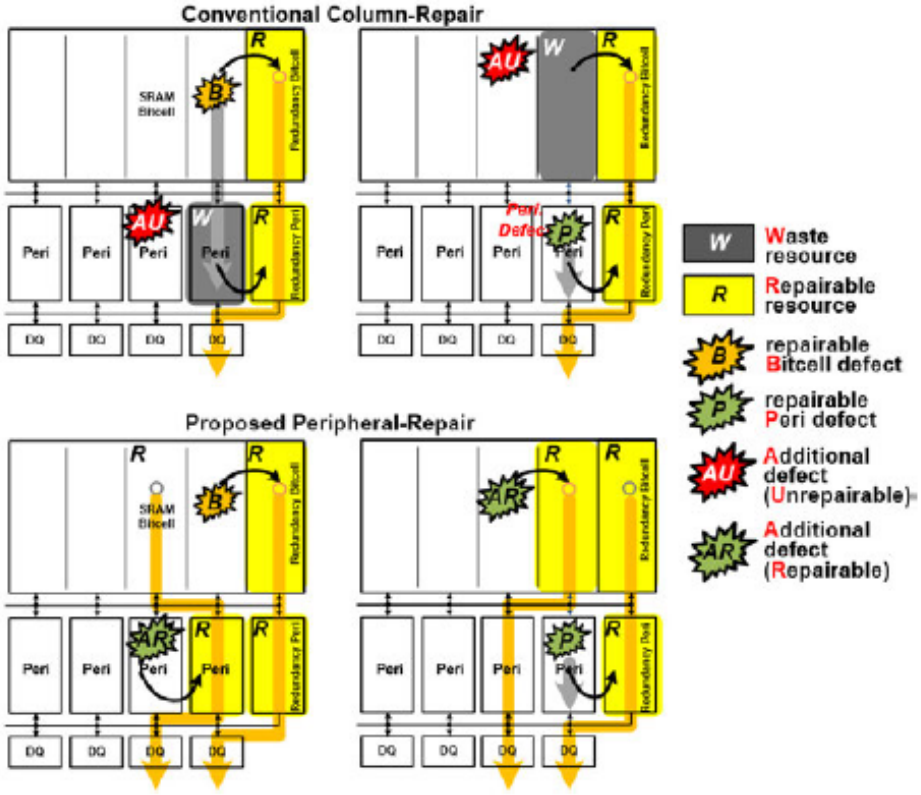
VDD vs VCC (or VDDM)

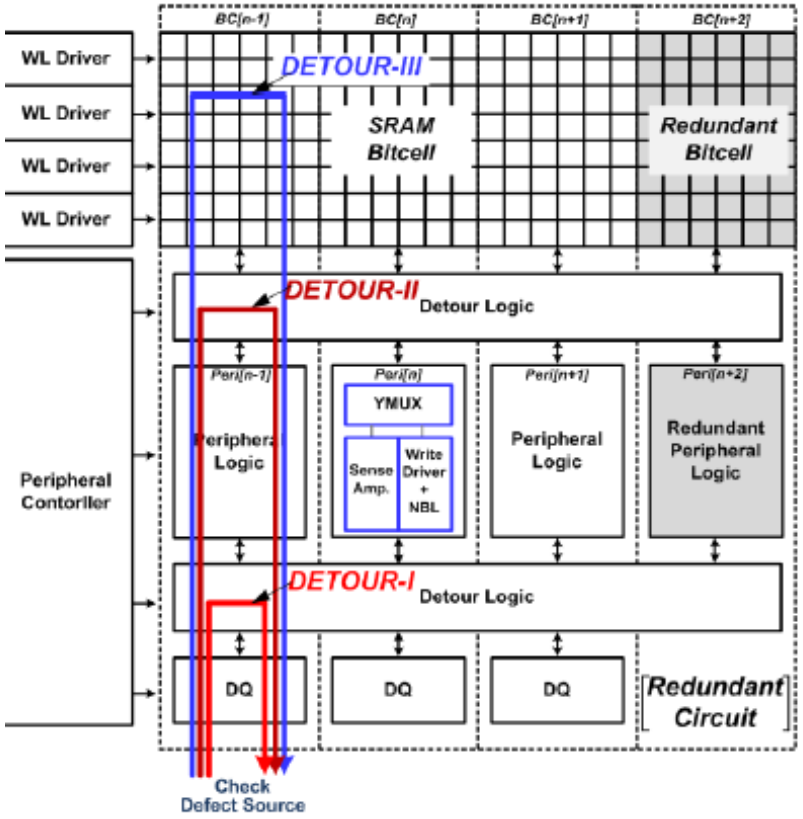


Hybrid Dual Rail Array



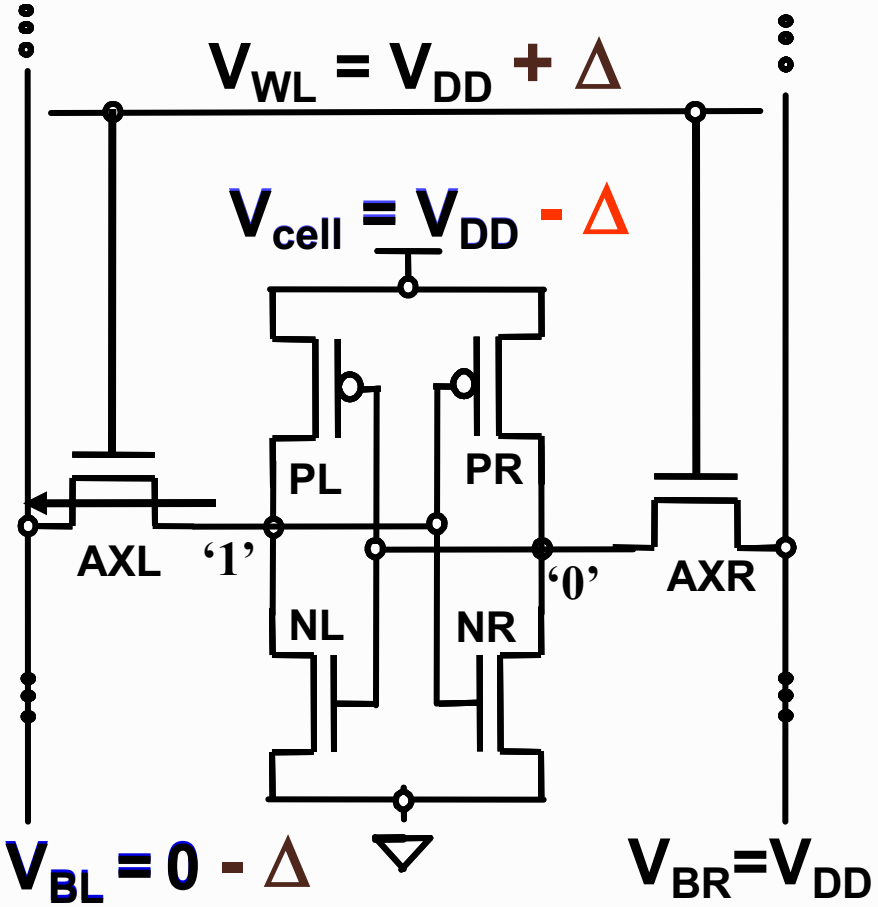
Array Redundancy





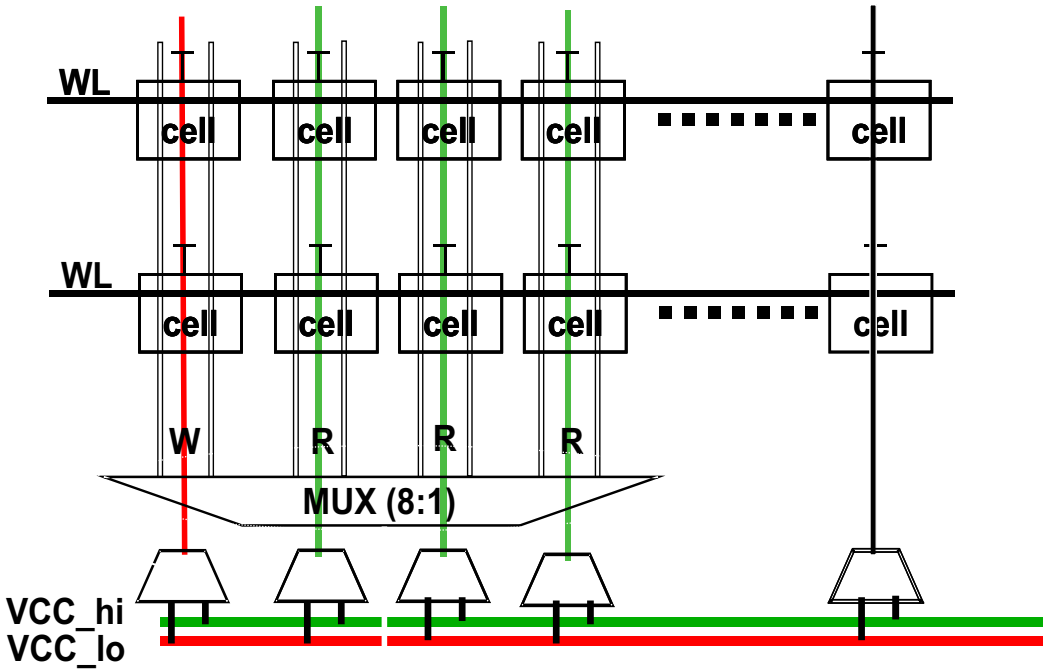
Use Redundancy to reduce Vmin

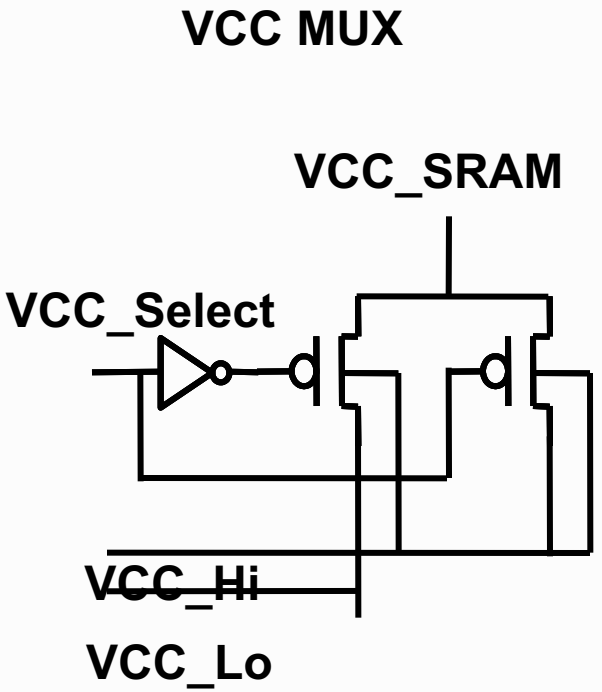
Dynamic Circuit Techniques for Variation Tolerant SRAM



	Read	Write
V_{WL}	Lower V_{WL} => lower V_{read} (weak AX)	Higher V_{WL} => Strong AX helps discharge
V_{cs}	Higher V_{cs} => lower V_{read} (strong PD) Higher V_{trip}	Lower V_{cs} => Weak PUP
V_{BL}	Weak impact	Negative V_{BL} for 0 => strong AX helps discharge

Example: Dual-Vcc based Dynamic Circuit Techniques

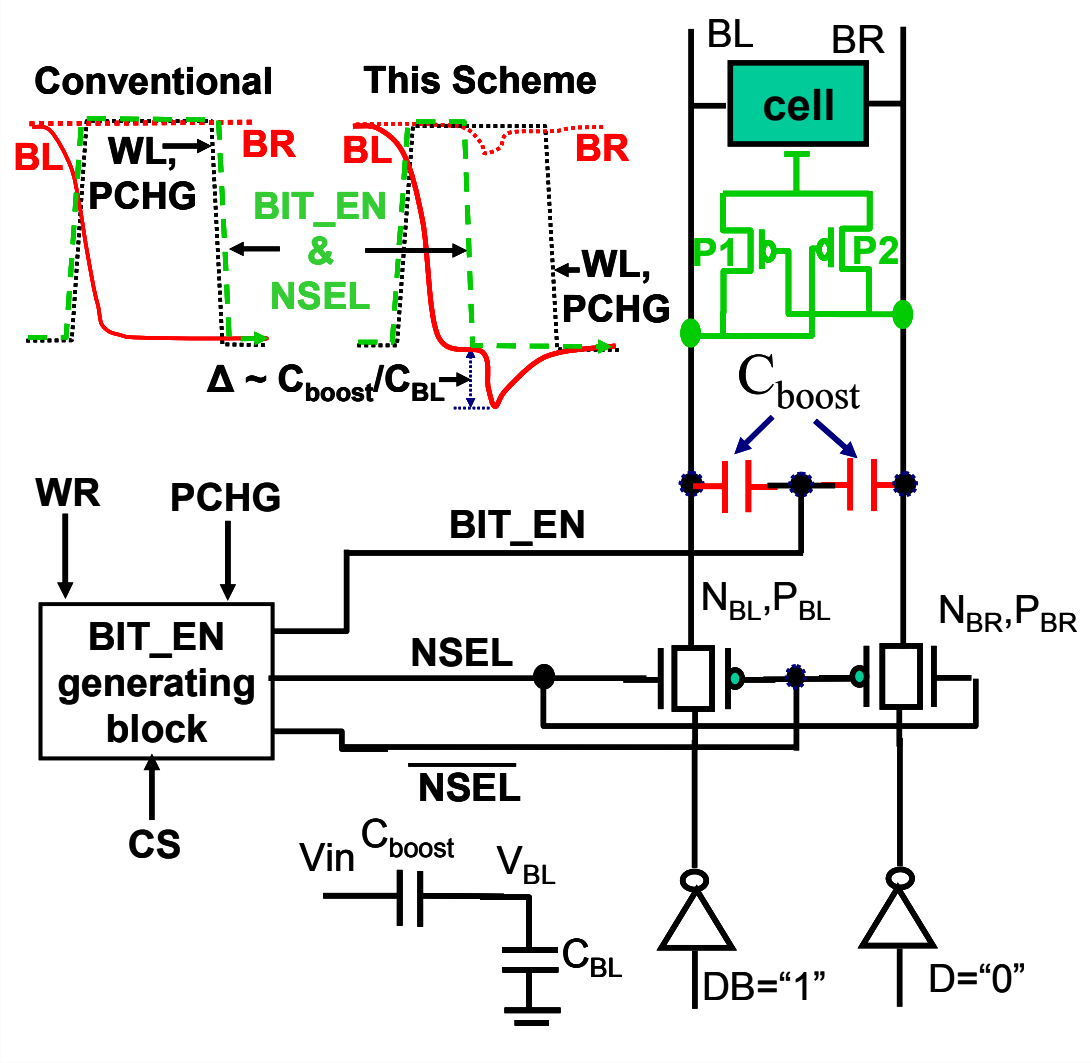




- Dynamic VCC MUX is integrated into subarray
- VCC selection is along column direction to decouple the Read & Write

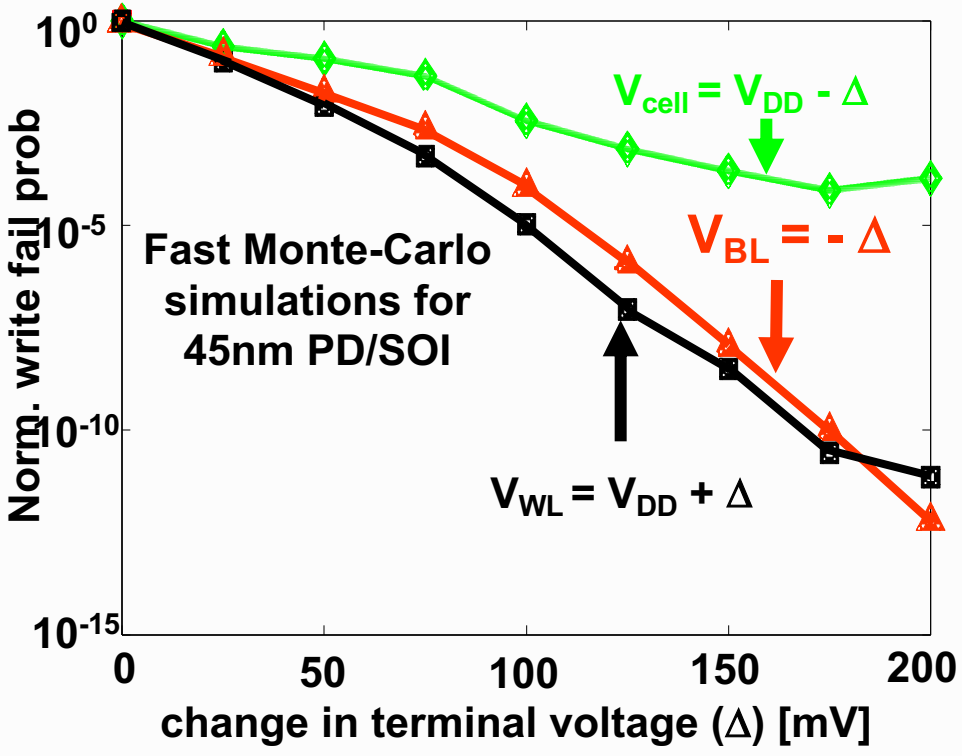
Source: K. Zhang et. al. ISSCC 2005

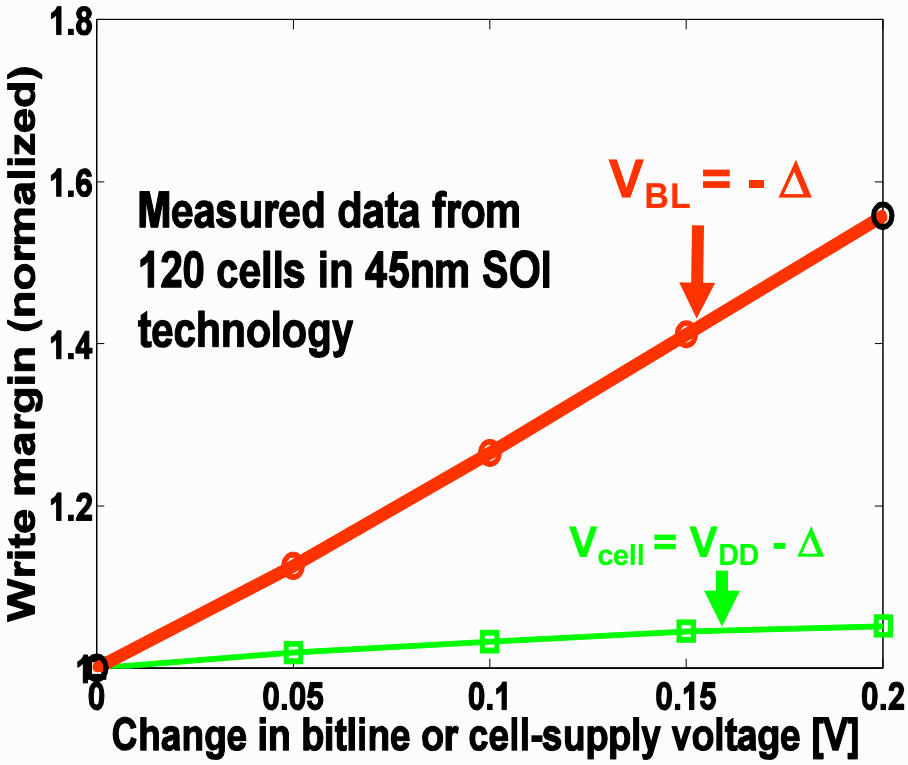
Negative Bit Line Scheme



Source: S. Mukhopadhyay, TVLSI 2009

Effectiveness Considerations: Writability improvement

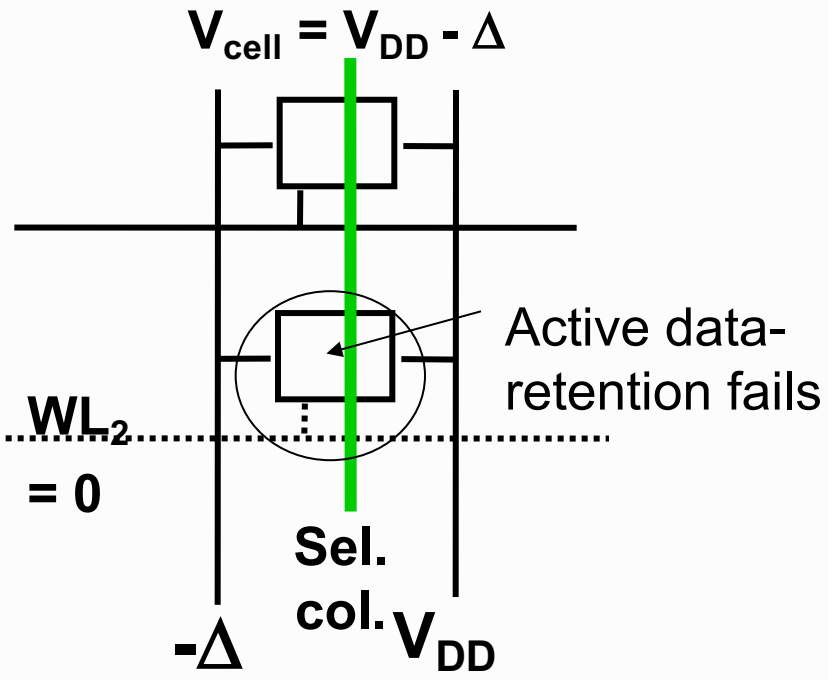


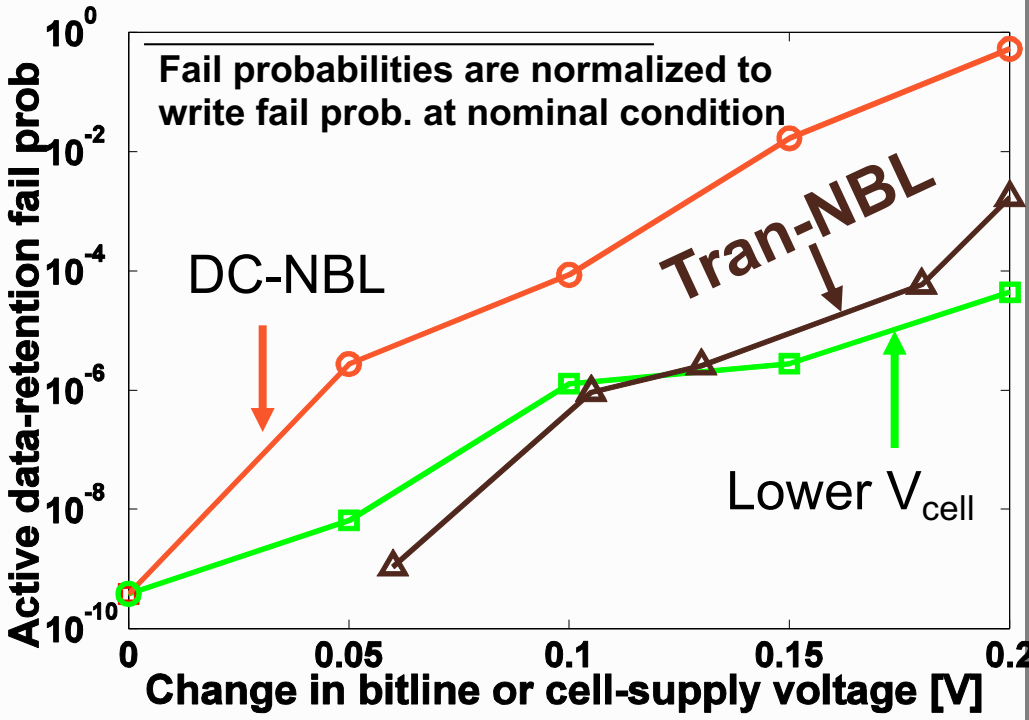


- Various dynamic schemes have different effectiveness in improving writability for similar read stability
  - Higher V_{WL} is most effective

Source: S. Mukhopadhyay, TVLSI 2009

Impact on Active Data-Retention

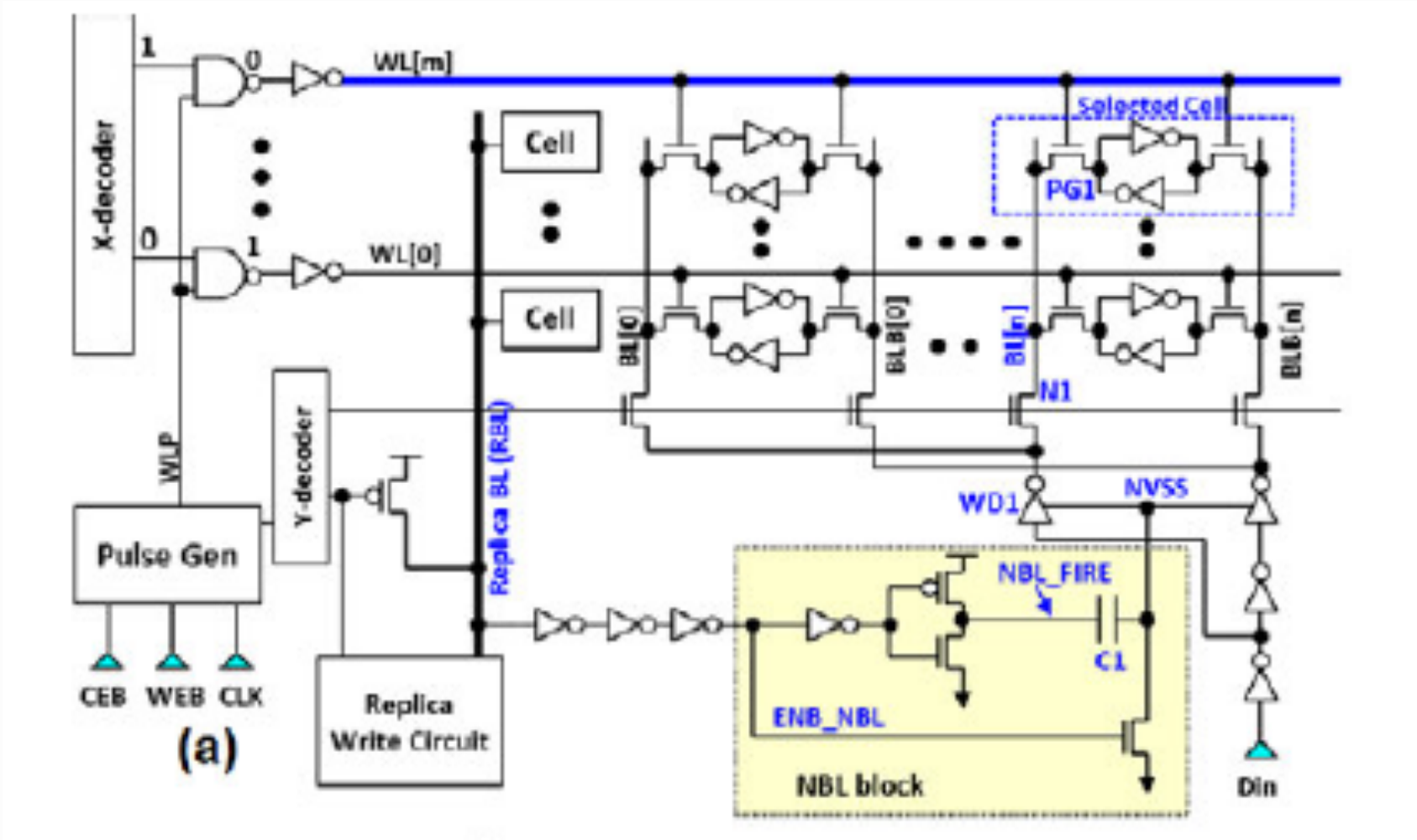




- Column based read-write control adversely impact the active data-retention failures
  - DC negative bitline has higher active data-retention failures
  - Tran-NBL and lower V_{cs} have comparable failure rates

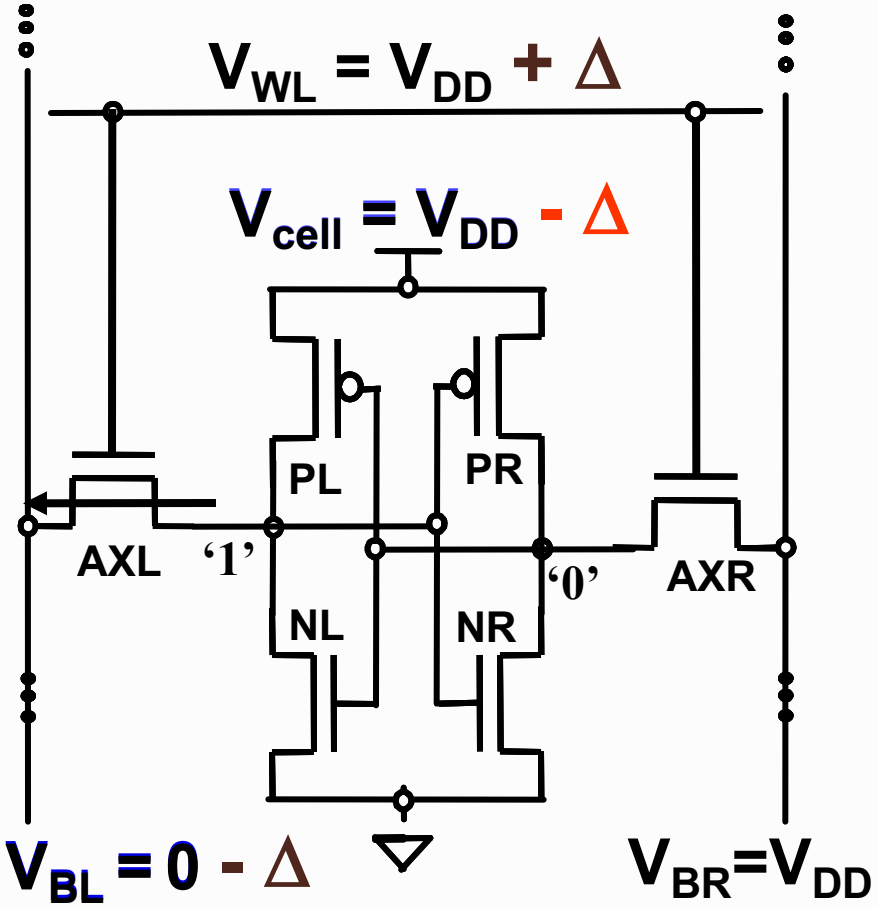
Source: S. Mukhopadhyay,, TVLSI 2009

Tran – NBL: Using Replica Column



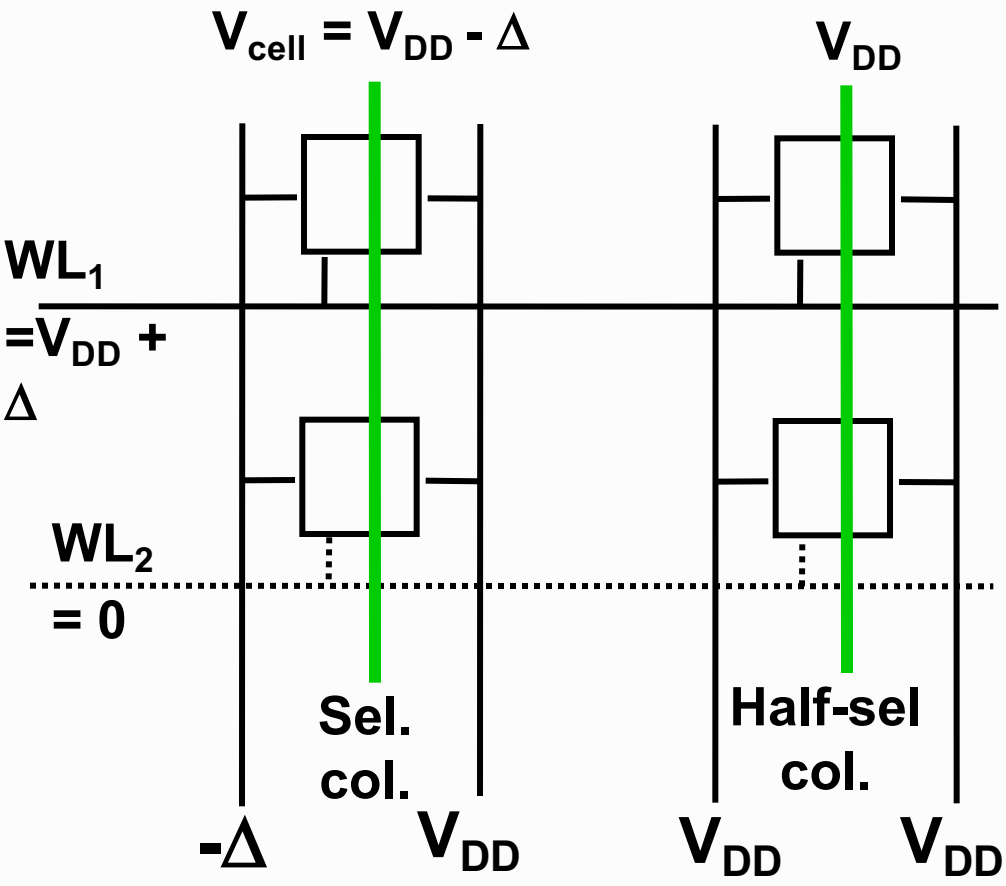
Source: J. Chang, ISSCC 2017

Dynamic Circuit Techniques for Variation Tolerant SRAM



	Read	Write
V_{WL}	Lower V_{WL} => lower V_{read} (weak AX)	Higher V_{WL} => Strong AX helps discharge
V_{cs}	Higher V_{cs} => lower V_{read} (strong PD) Higher V_{trip}	Lower V_{cs} => Weak PUP
V_{BL}	Weak impact	Negative V_{BL} for 0 => strong AX helps discharge

Implementation Consideration: Half-Select Stability

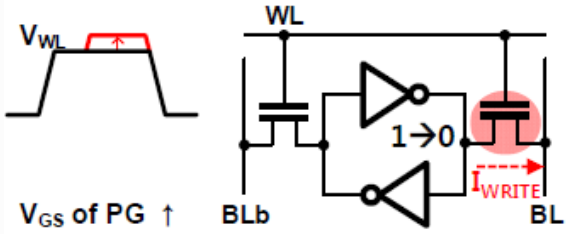


- Higher V_{WL}
  - – Row-based scheme
  - – Degrades half-select read stability of the unselected columns
- Lower V_{cell} or negative bit-line
  - + Column-based scheme
  - + Half-select read stability remains same

Assist Methods

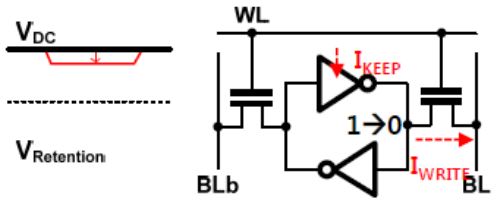
WLOD *(WL Overdrive)*

- Strengthen PG



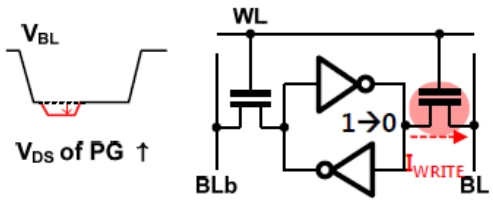
VCDL *($V_{DD,CELL}$ Lowering)*

Weaken PU



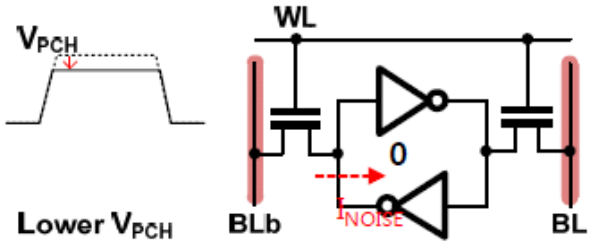
NBL *(Negative BL)*

- Strengthen PG



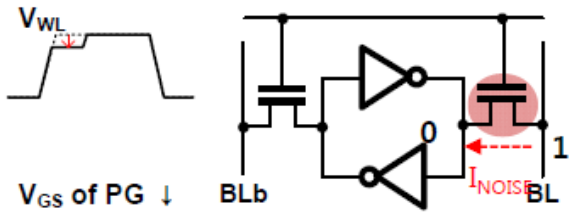
SBL *(Suppressed BL)*

Weaken BL noise



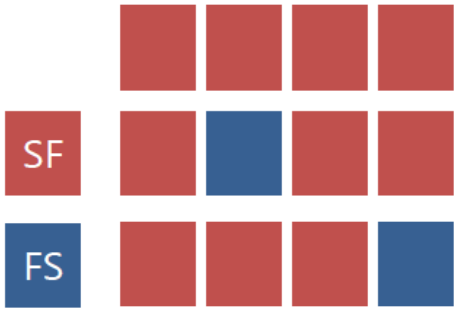
WLUD *(WL Underdrive)*

- Weaken PG

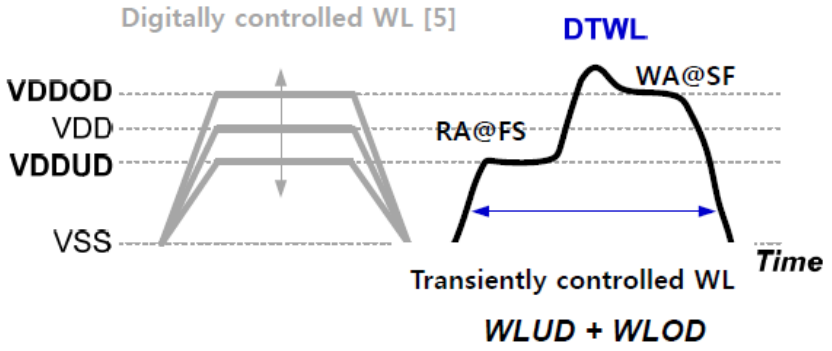


Proposed Dual-Transient WL (DTWL)

- Dual-Transient WL (DTWL) controls WL transiently
- DTWL provides mix-up assist for read and write
  - Covers different process-corner
  - DTWL mitigate the impact of WLOD (WA)

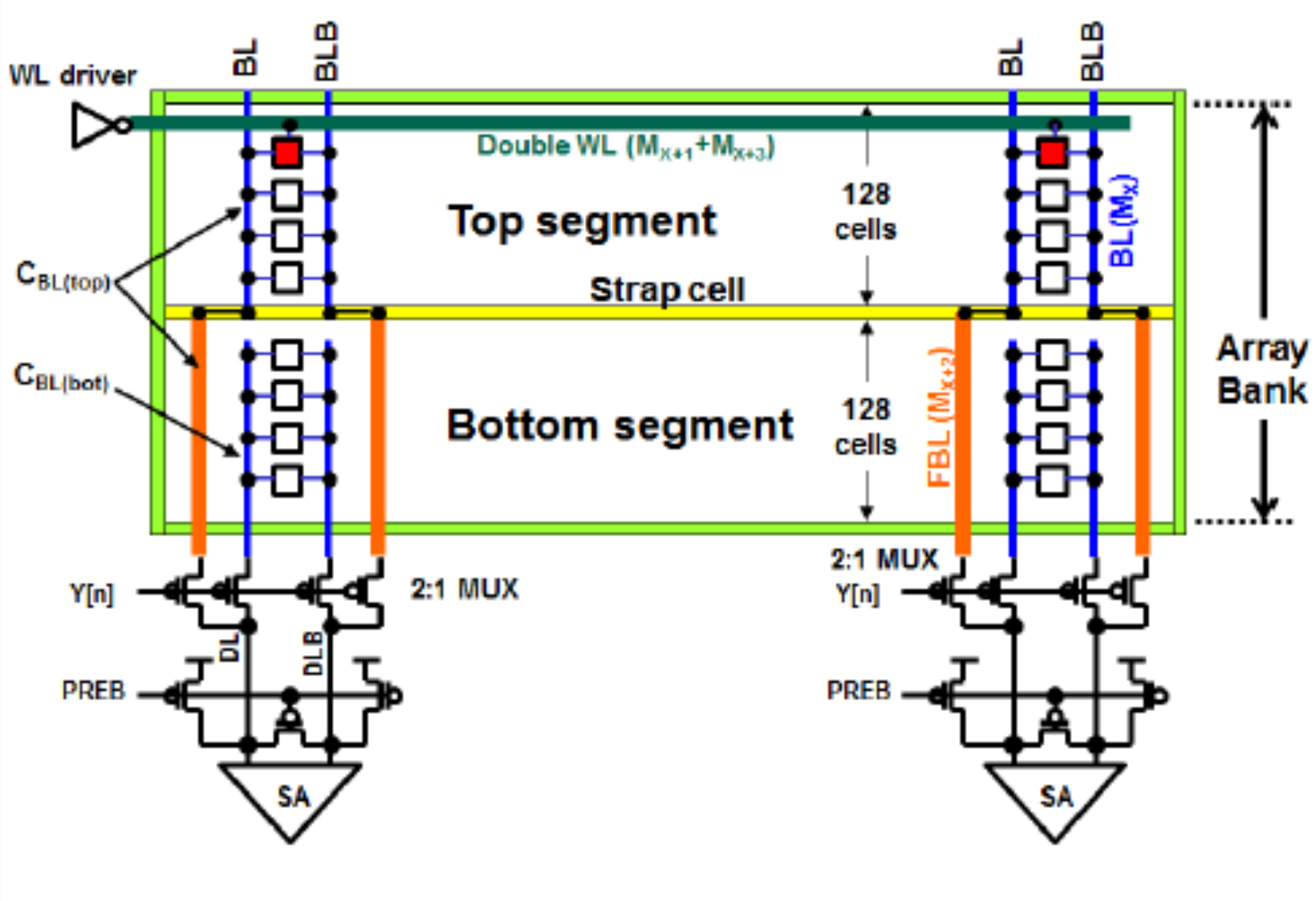


different process-corner



RA and WA

Flying Methods



Question

- Of the various assist methods

a) Negative bit line scheme does not help 8-T sram cell

b) Word line under drive does not help 8-T sram cell

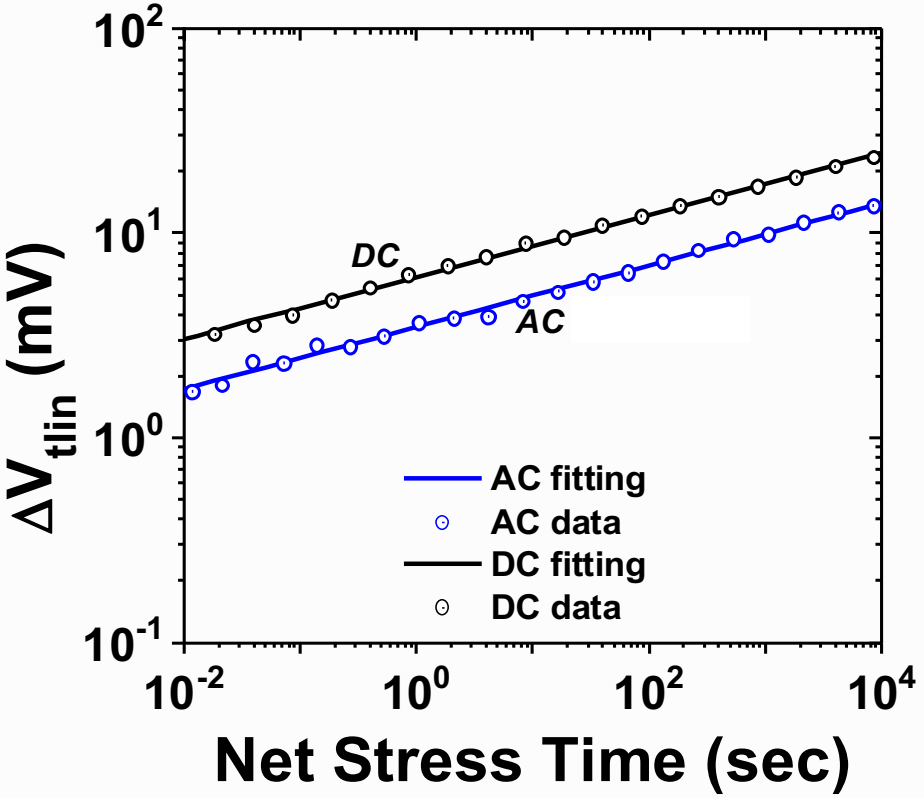
c) Word line over drive does not help 7-T conditionally decoupled sram cell

d) VCDL does not help any kind of assymetric sram cell

Bias Temperature Instability

FET characteristics and BTI

- Threshold voltage (V_T)
- Current degradation approximately corresponds to V_T degradation
- Known sensitivities
  - PBTI is *more* sens. to Voltage
  - NBTI is *more* sens. to temperature
- Semi-empirical model (for both NBTI and PBTI)

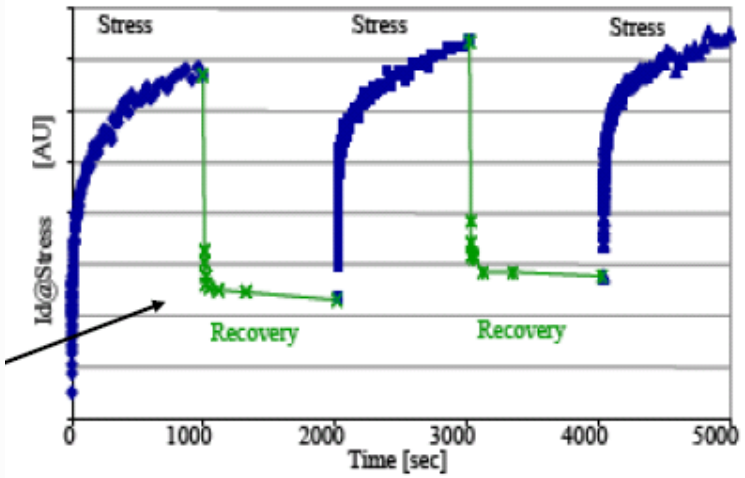


$$\Delta V_T|_{DC\_stress} = A V_{DD}^{a} T^{b} t^{n}$$ *(without including recovery)*

Recovery after stress

Static stress and recovery or "0.001 Hz waveform"

*Ramey et. al., Intel, IRPS 2009



- **Recovery happens when FET is OFF**

$$\Delta V_T\,|_{after\_relax} = FR \mathrm{x} \Delta V_T\,|_{DC\_stress}$$

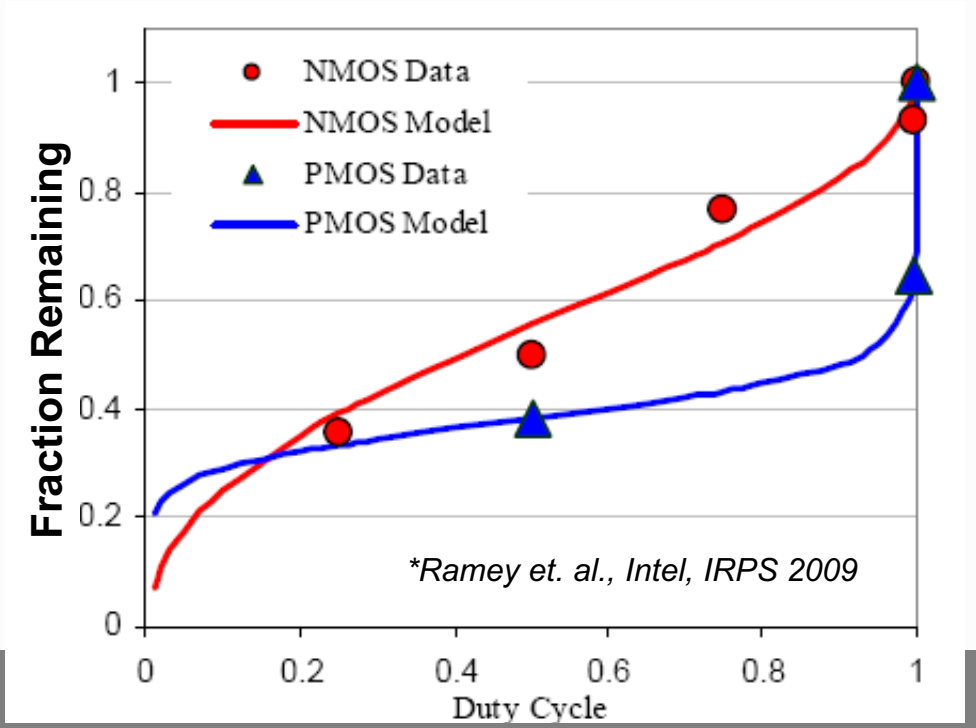
Fraction Remaining

$$FR = \left[1 + \alpha \left(\frac{t_{relax}}{t_{stress}}\right)^n\right]^{-1}$$

- In other words, if probability of '1' at the gate of an NFET is say P_1, then,

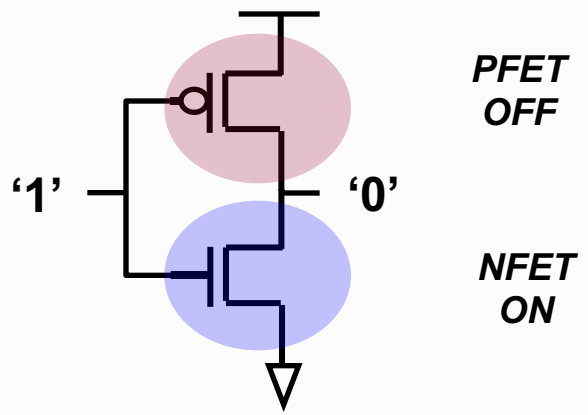
$$\text{duty\_cycle} = \frac{t_{\text{stress}}}{t_{\text{stress}} + t_{\text{relax}}} = P_1$$

- **Biggest benefits of recovery when duty_cycle < 95%**



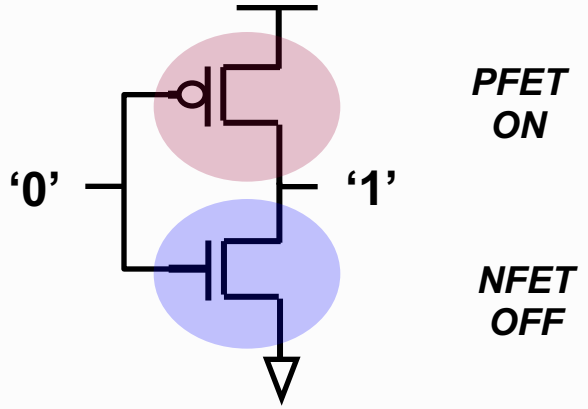
FET stress-recovery

Let’s take an example of simple CMOS inverter



PFET is relaxing: Gate-source HIGH and drain LOW

NFET is stressed: Gate is HIGH and source-drain LOW



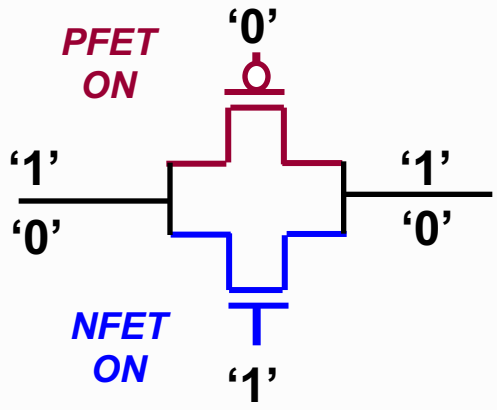
PFET is stressed: Gate is LOW and source-drain HIGH

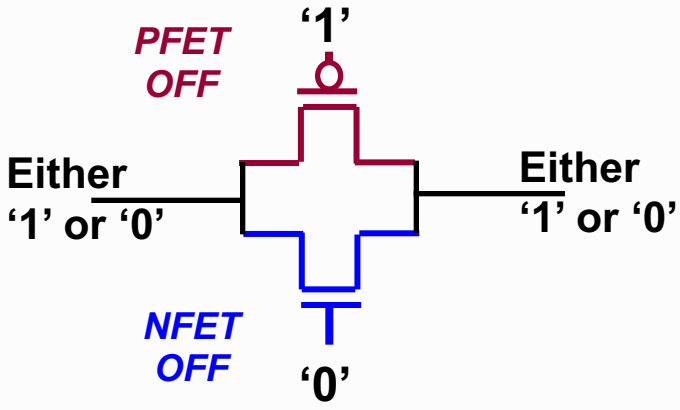
NFET is relaxing: Gate-source LOW and drain HIGH

- If a FET is ON, it’s stressed (for both NFET and PFET)
- If a FET is OFF, it’s relaxed (for both NFET and PFET)

FET stress-recovery

For other circuit types say transmission gate



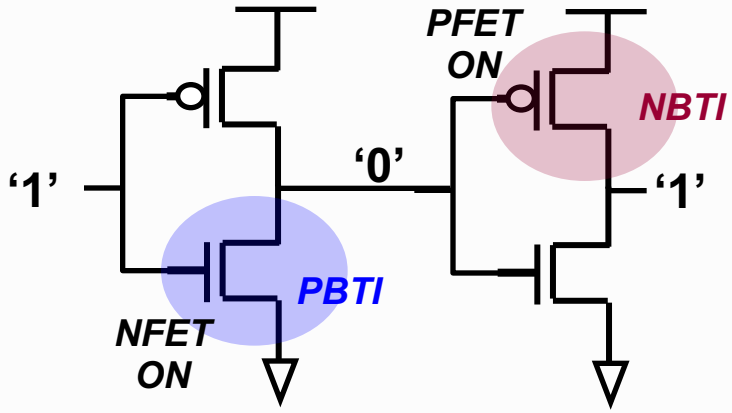


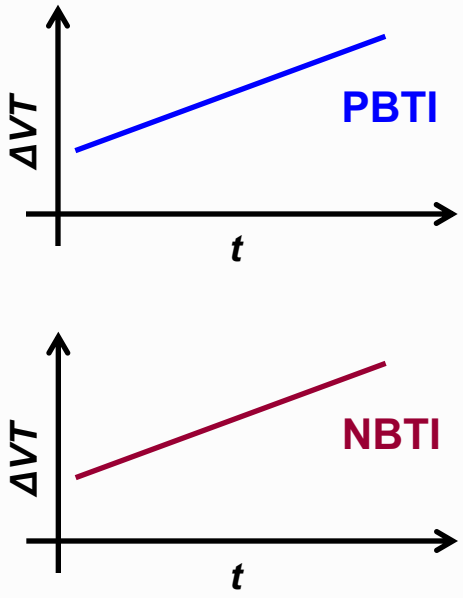
- **Both the FETs are either ON or OFF together**
- **Source-drain voltages during relaxation depends on other circuit blocks on left and right**
  - **e.g., negative gate-drain or gate-source voltage in NFET may speed up recovery (also true for inverter on previous slide)**

Nature of Stresses/recovery

Static or DC stress

– FETs are in the same voltage bias condition during the USAGE





Examples:

–SRAM cells storing the same data for long time

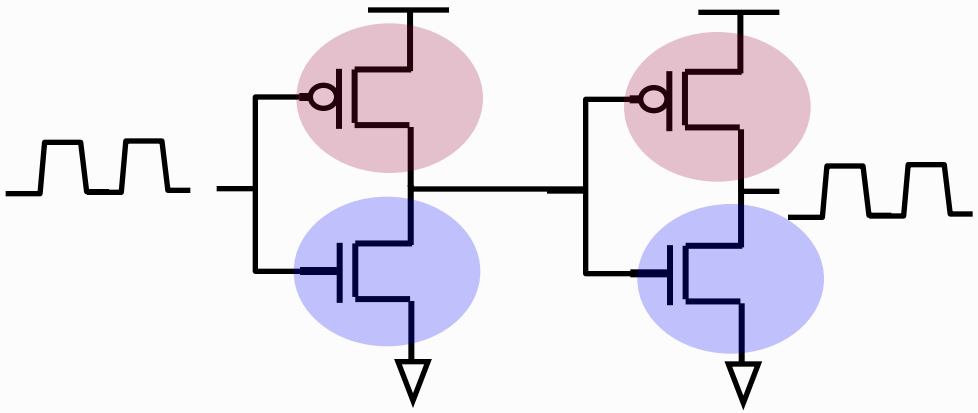
–Circuit paths not used for long time but powered on

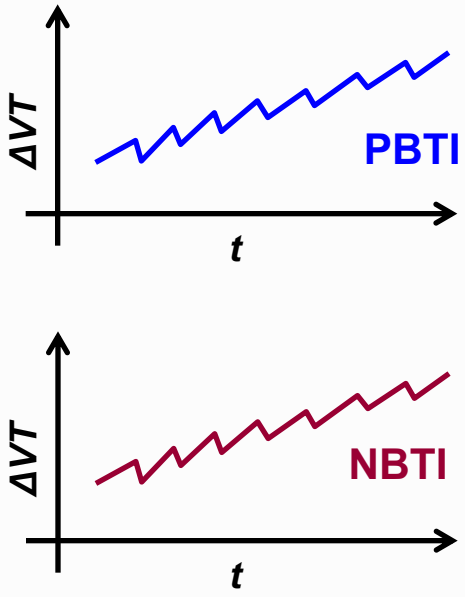
– Word line drivers, local and global eval circuits

Nature of Stresses/recovery

Alternating or AC stress

- FETs turn ON (stress) and OFF (recover) during the USAGE
- It's composed of several DC stress and recovery conditions
- Durations of stress and recovery depend on nature of program running and typically can not be estimated





Examples:

–SRAM cells frequently changing the stored data

–Logic circuit paths doing computations

Question

- The bias temperature instability device degradation in a circuit can be reduced by

a) Using assymmetric transistors since they will degrade at different rates
b) Avoiding pass gates in the design and always using transmission gates
c) Increasing the supply voltage of the circuit
d) Ensuring that all nodes in a circuit switch every N cycles

Timing Failure due to BTI