Advanced Topics in VLSI

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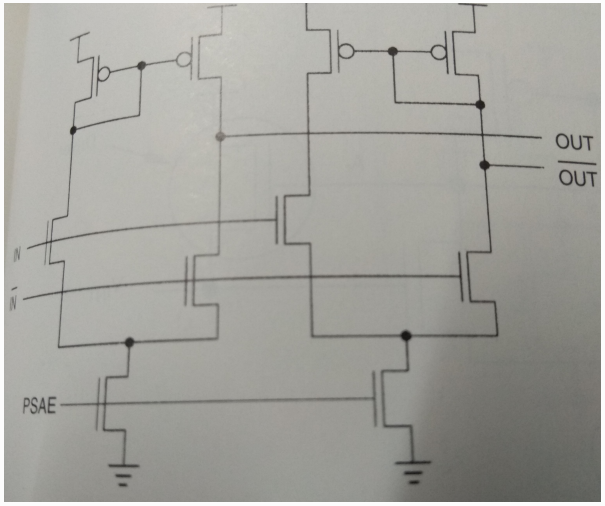
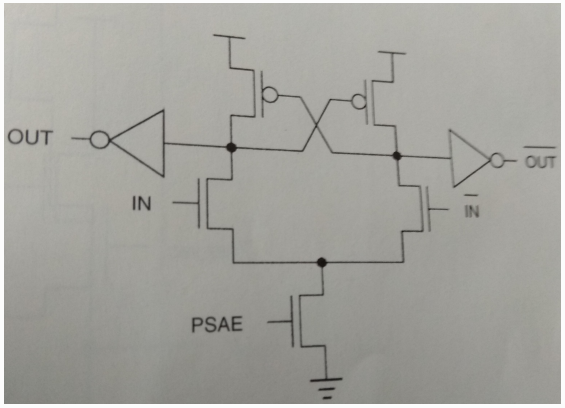
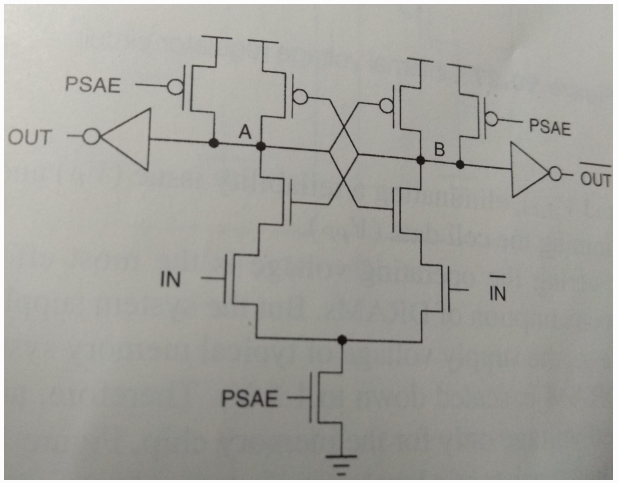
Sense Amplifiers (Alternate)



Current Mirror Based



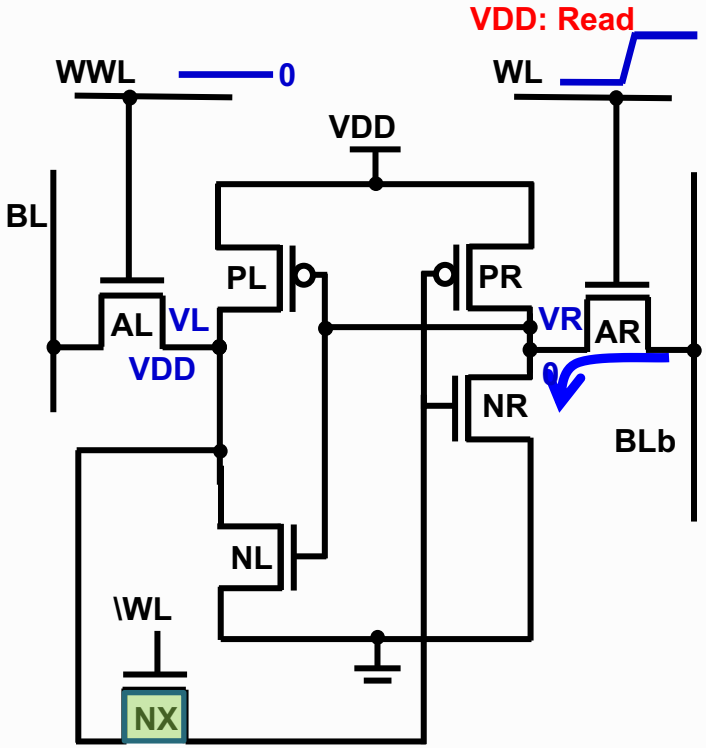
Half Latch Based

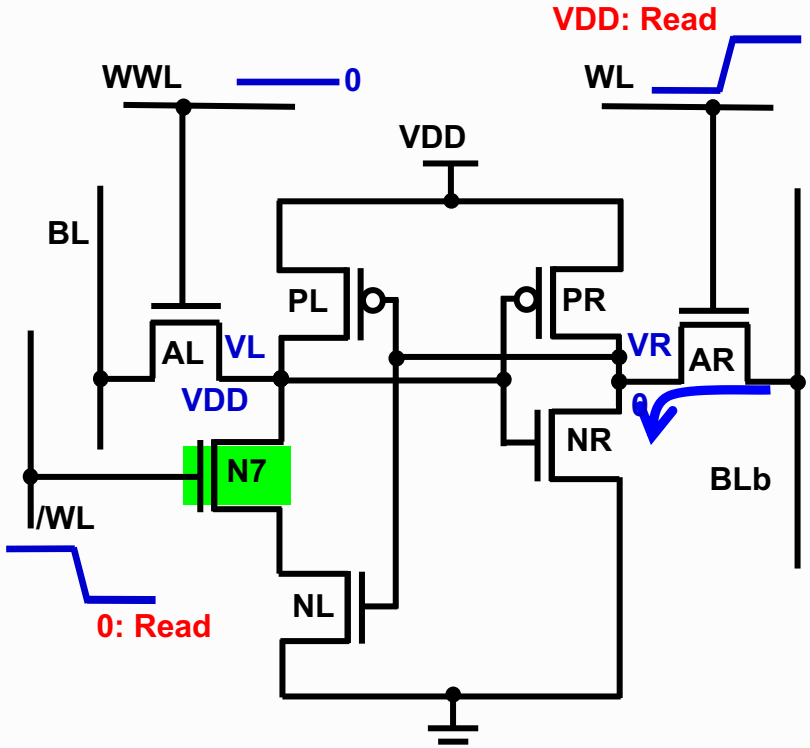


Full Differential

Discuss in class next week

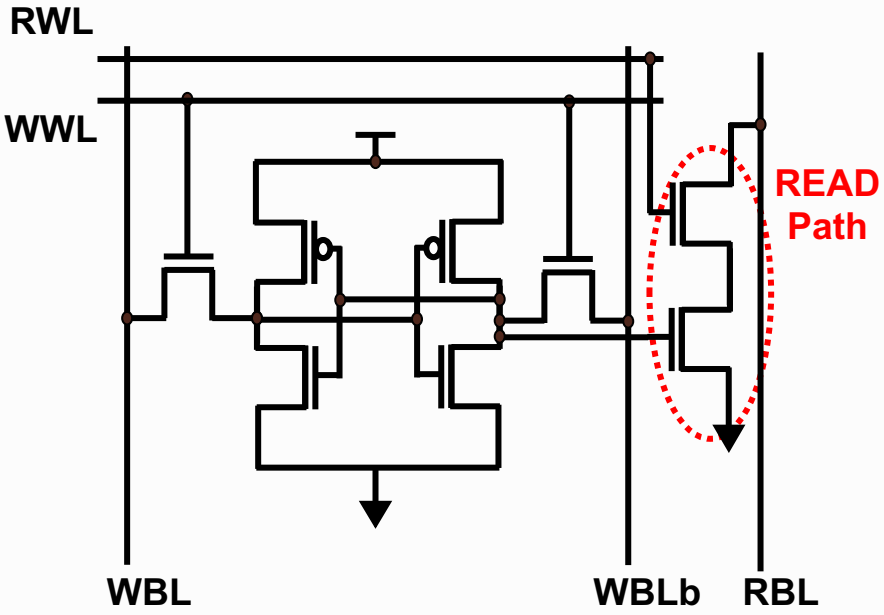
Conditionally decoupling regeneration

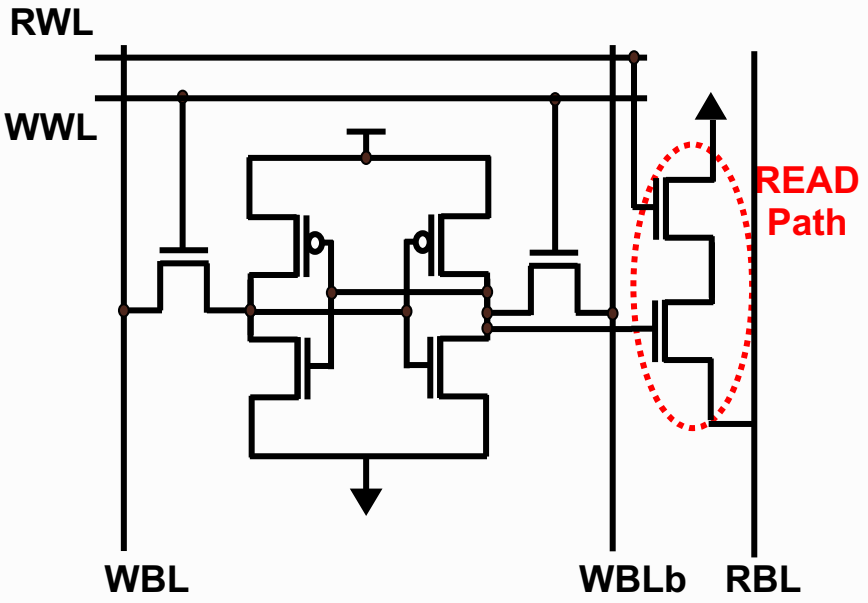




Why use /WL ...?

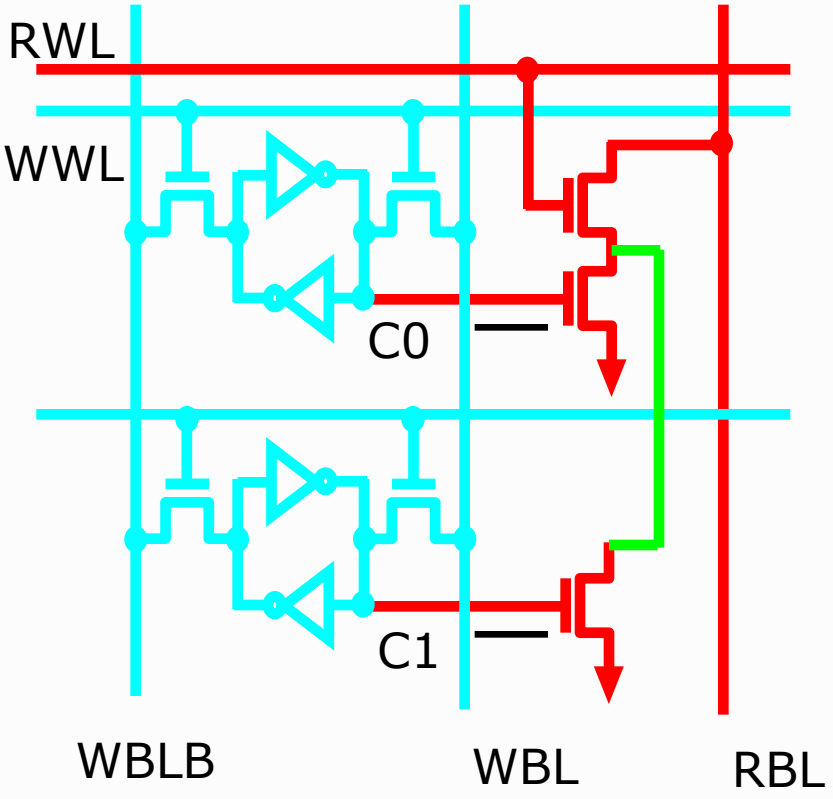
Thought exercise





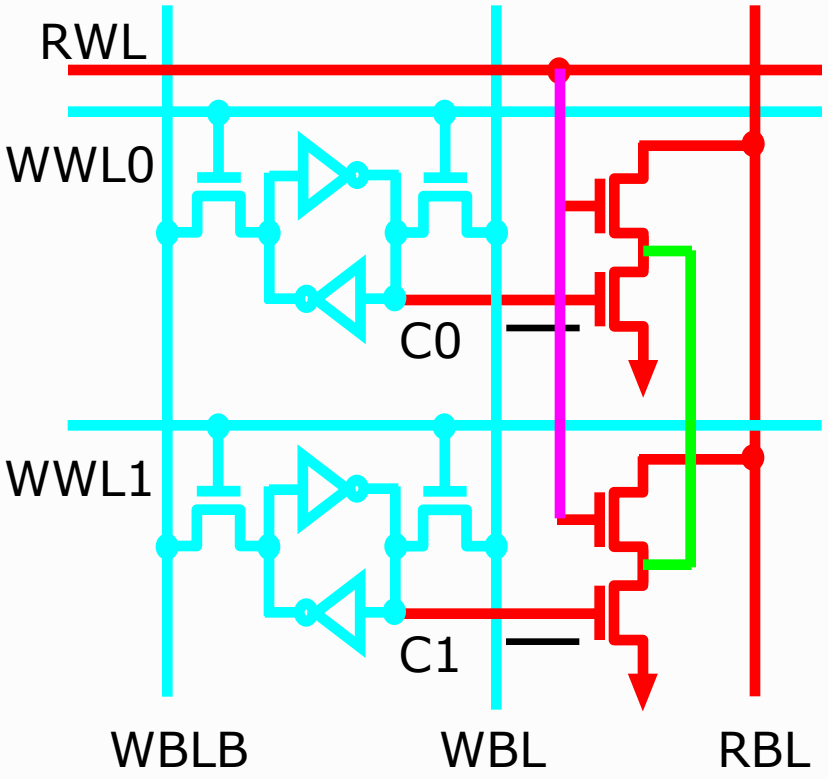
Implement logic function via 8T merge

- Concept: Use the 8-T portion of the cell for implementing logic functions
  - Possible due to decoupling of read and write paths
- RBL discharges when either C0 or C1 is high
  - Read stack remains 2-high
- And function: switch definition of WBL and WBLB
- An OR2 embodiment is shown on right
  - Can be complex OR4, OR8, etc.

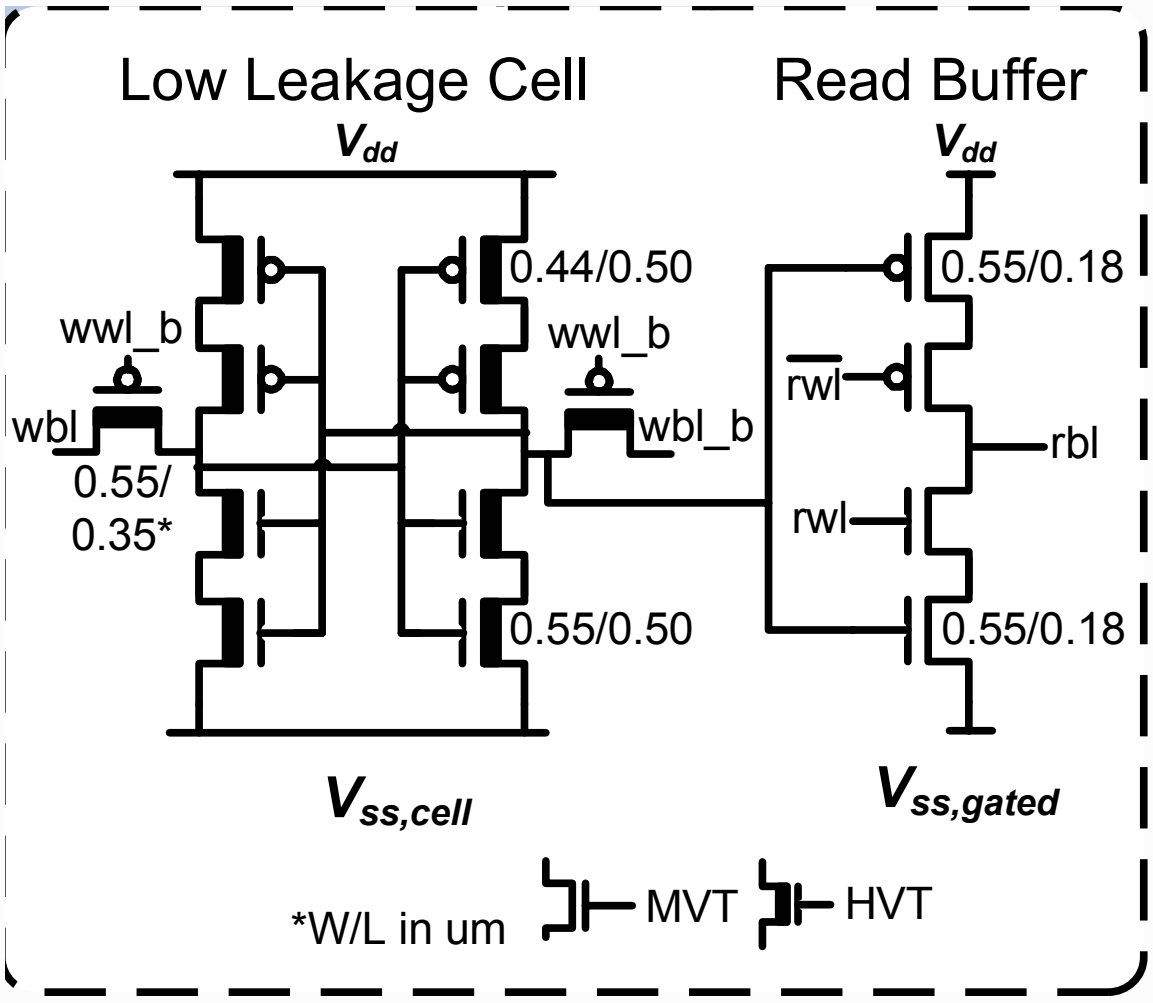


A More Practical Implementation

+ Share RWL between adjacent cells
  => 3 word-lines in 4 metal tracks
  - Reduces coupling capacitance (+ performance and power)
+ All FEOL features identical to conventional 8T cell
  - OR
  - upper device in stack can be made smaller, reducing cell size



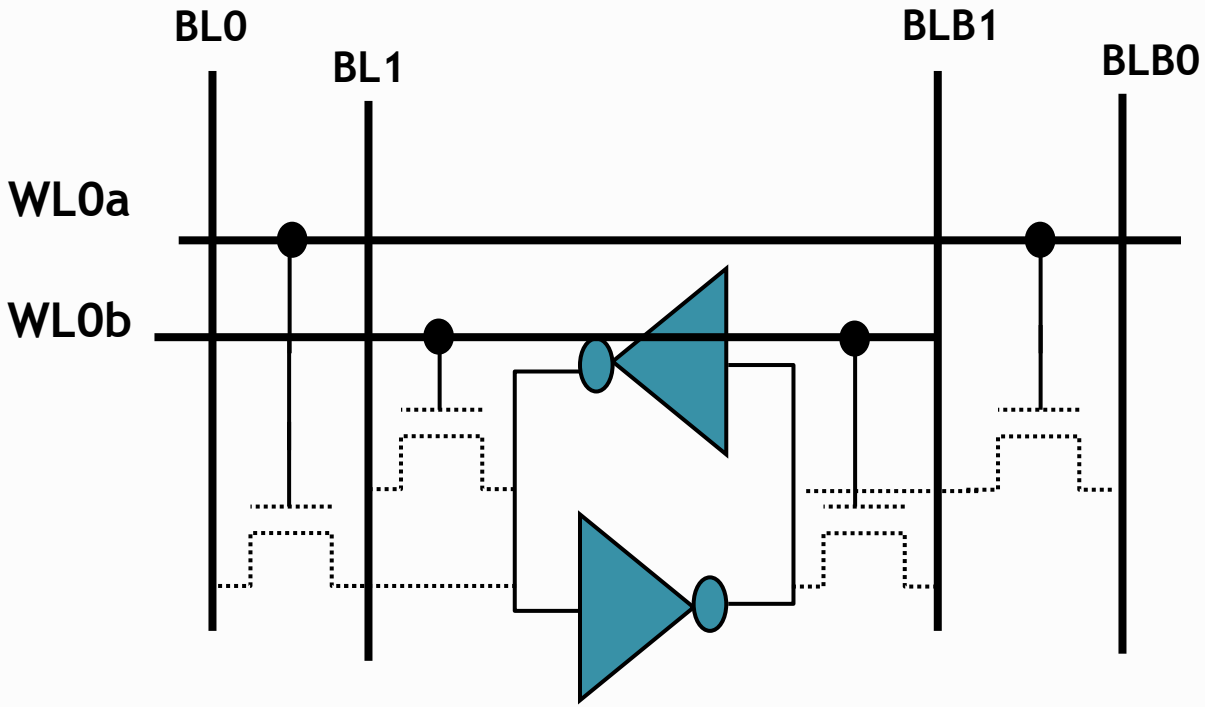
Low leakage SRAM



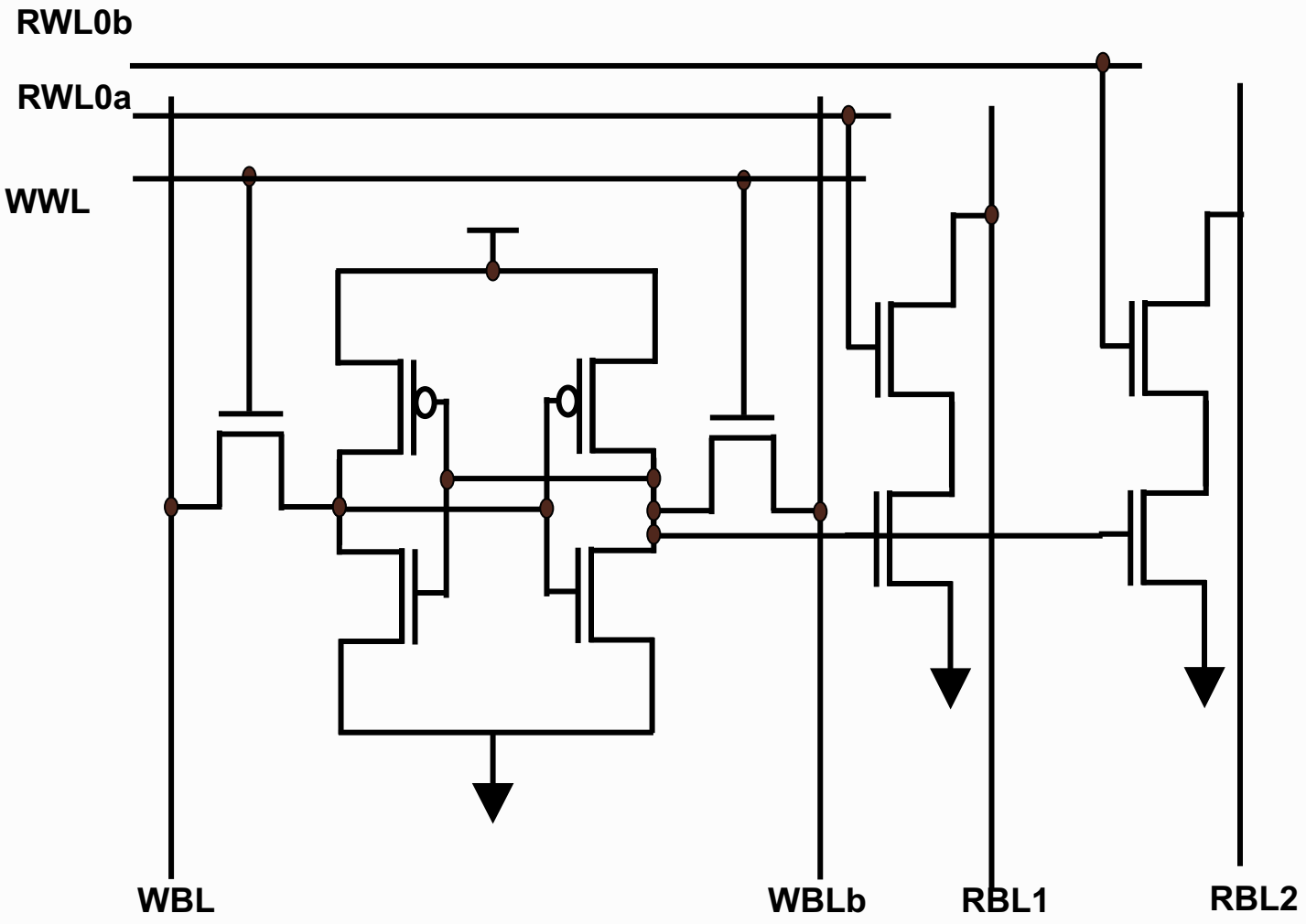
The Phoenix Processor: A 30pW Platform for Sensor Applications

(S. Hanson , VLSI Symp '08)

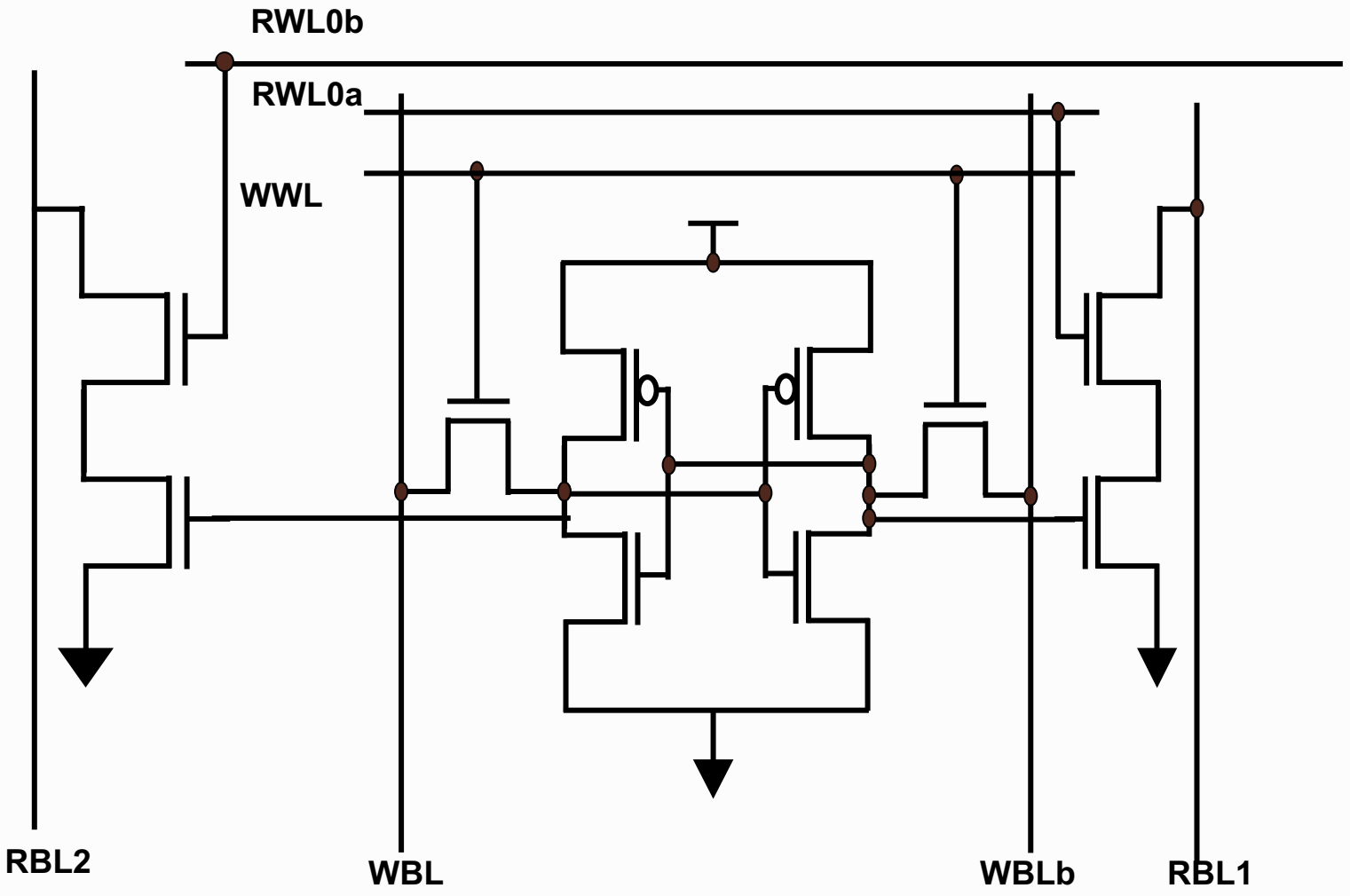
Multi-porting SRAM Cell



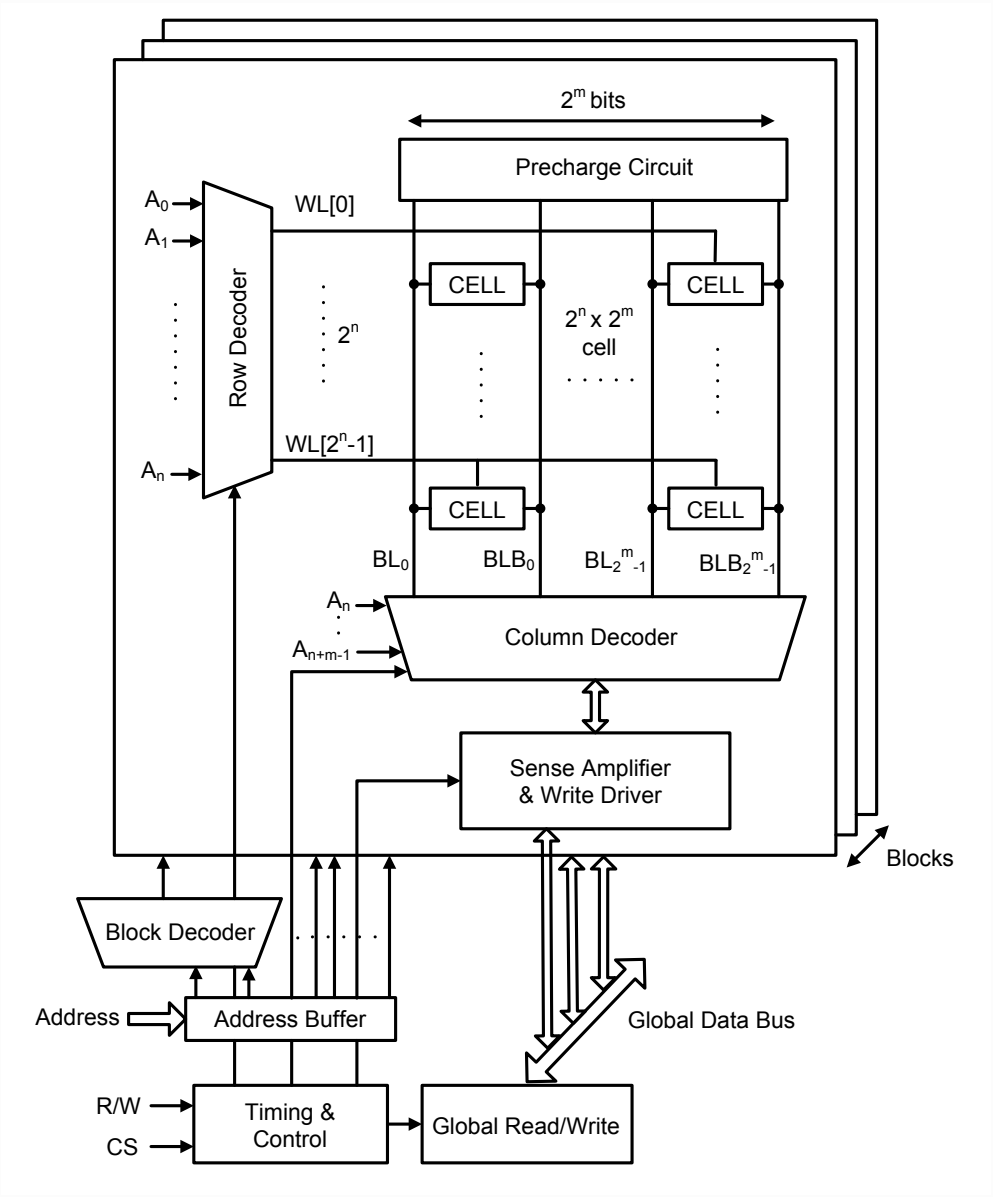
Multi read ports



Multi read ports

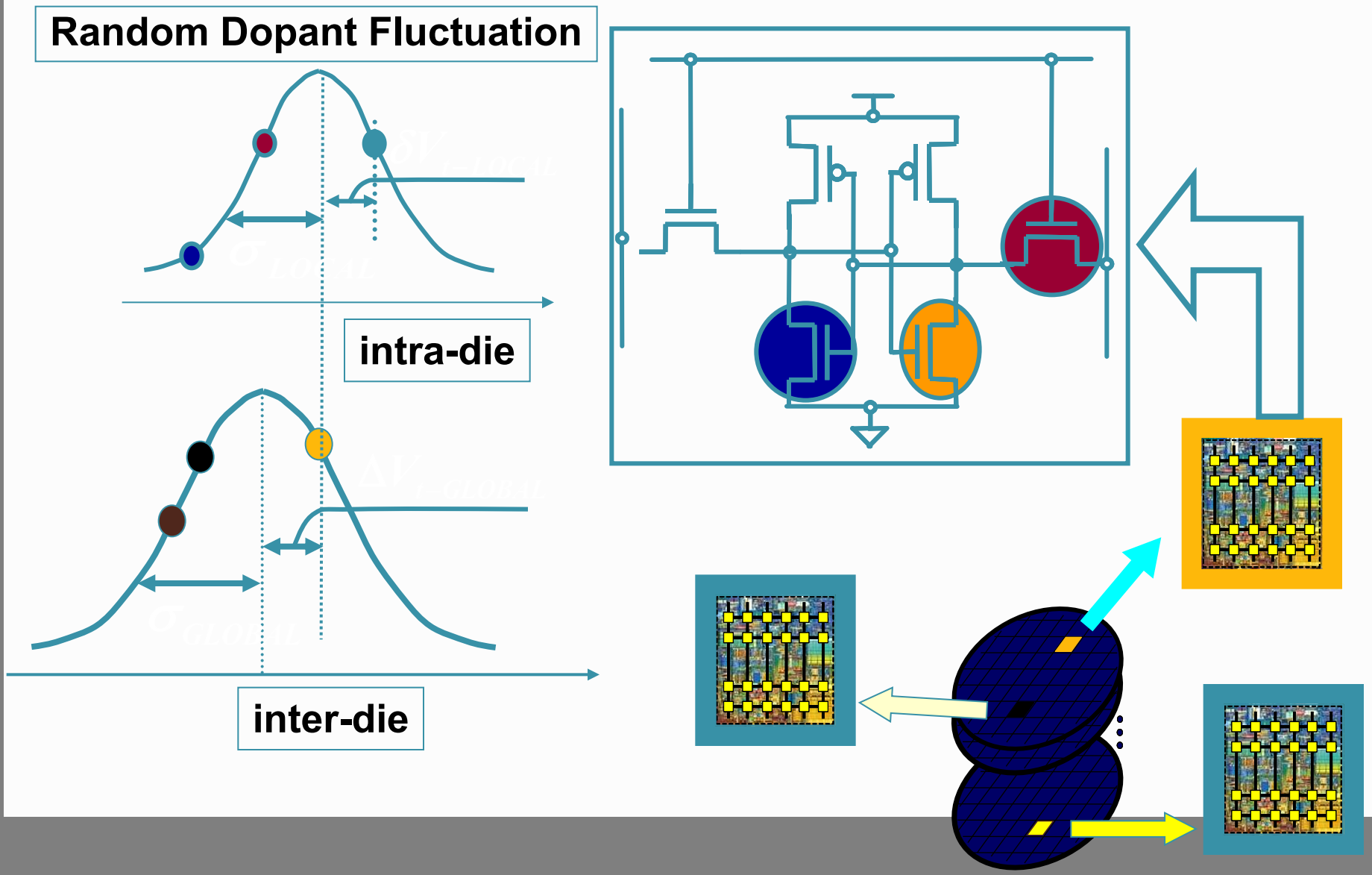


Block Diagram

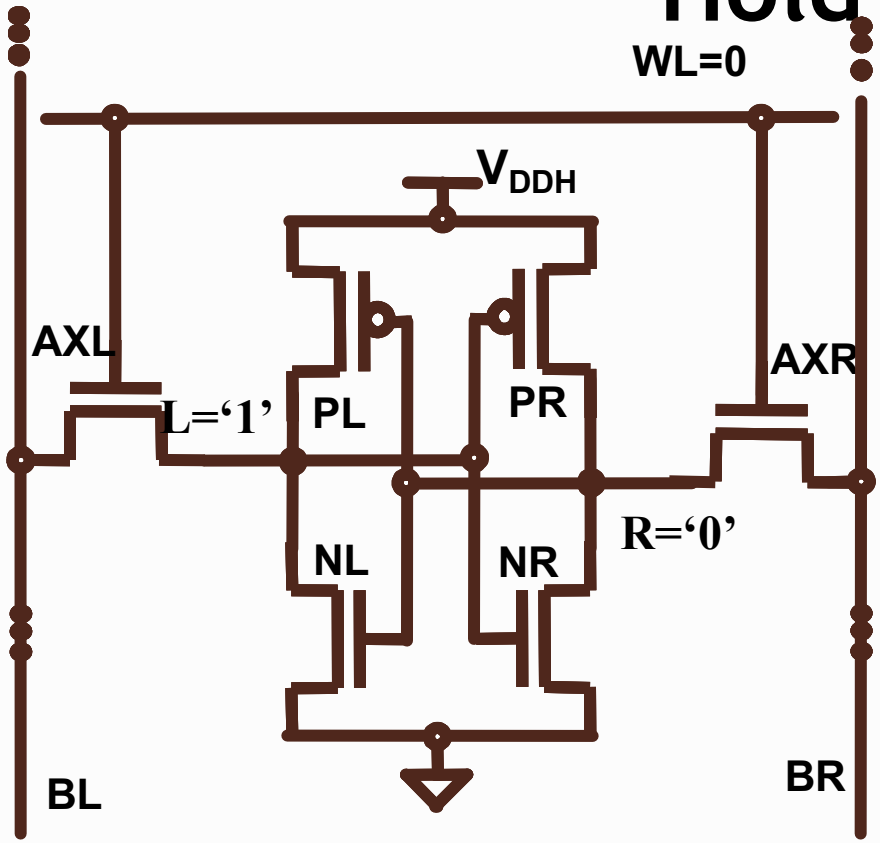


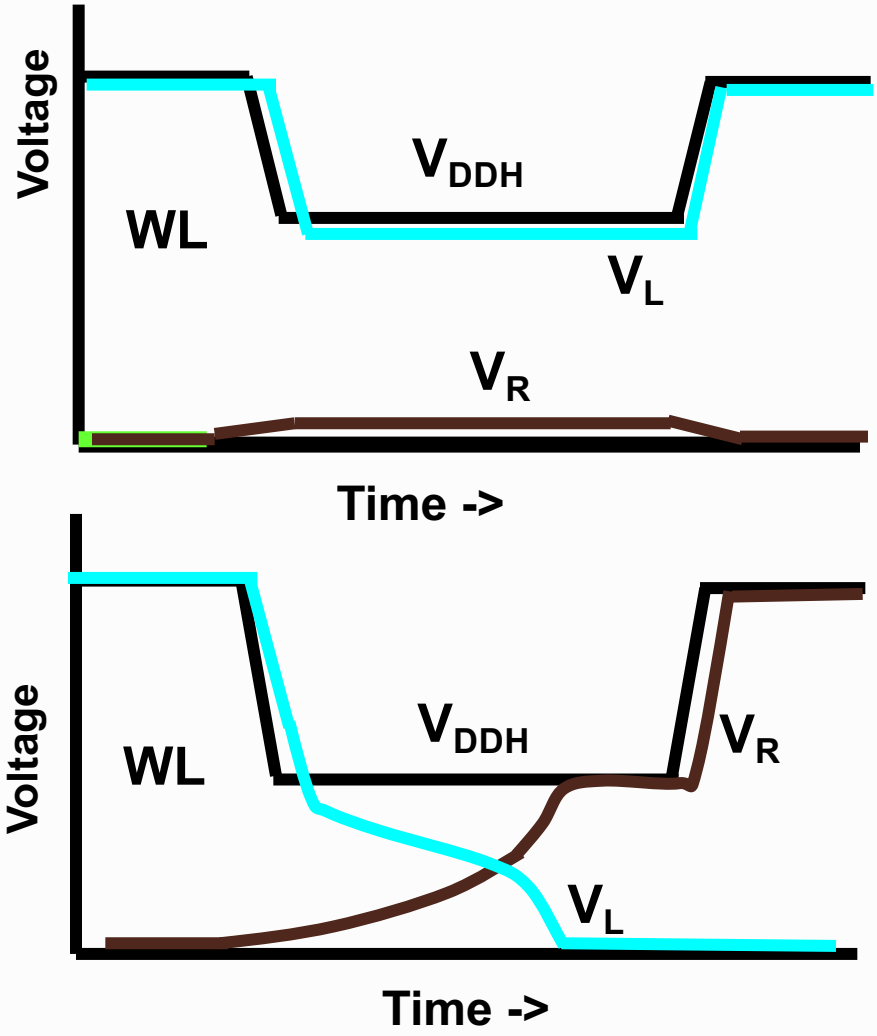
Bank and Bank Conflicts

Global and Local Variations

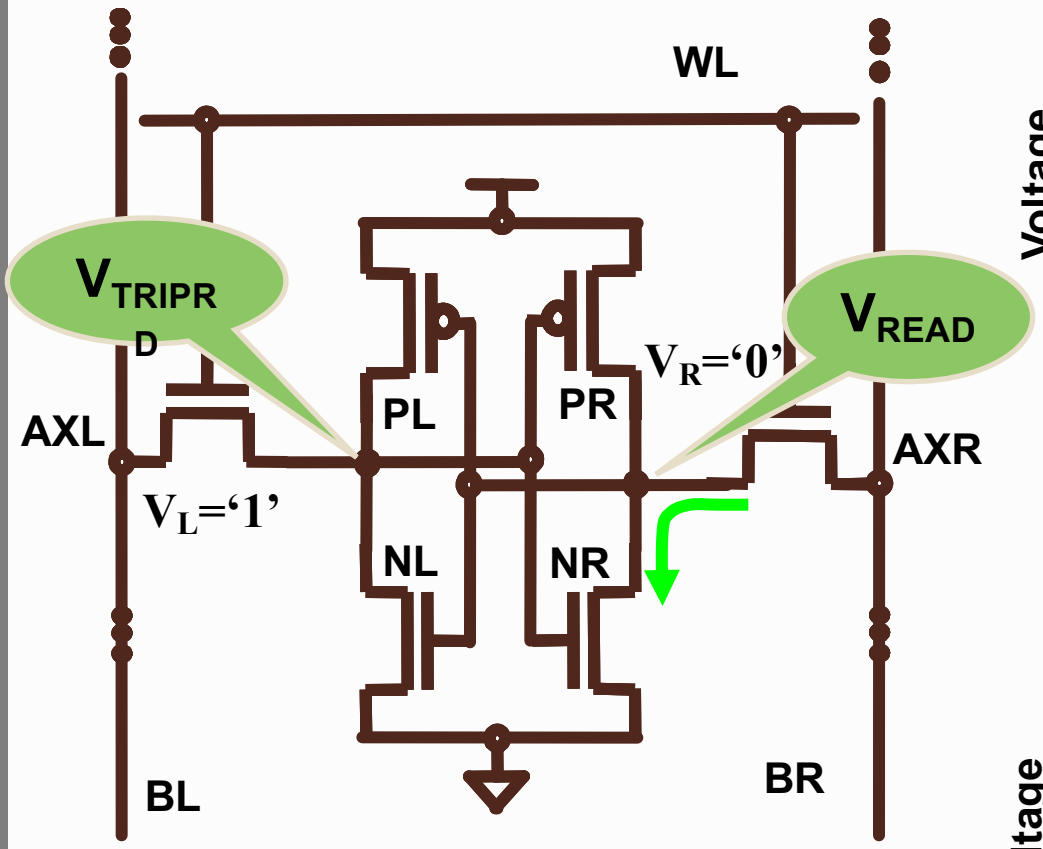


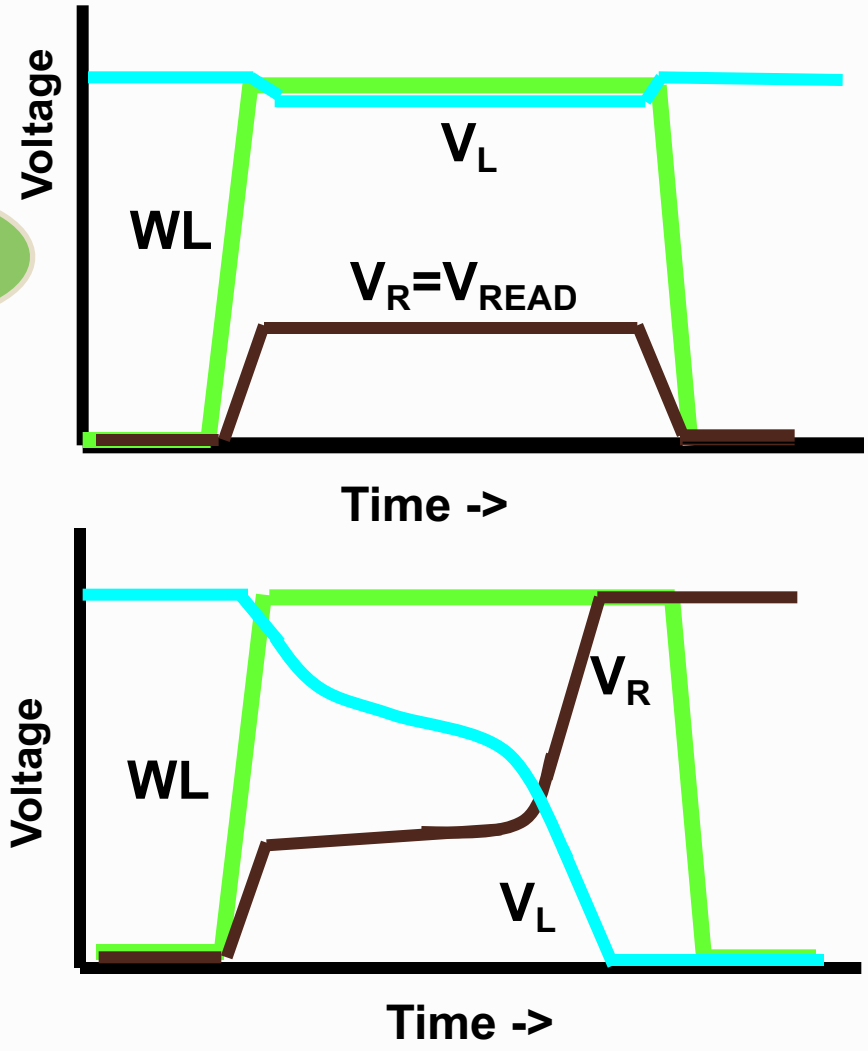
Hold Failure



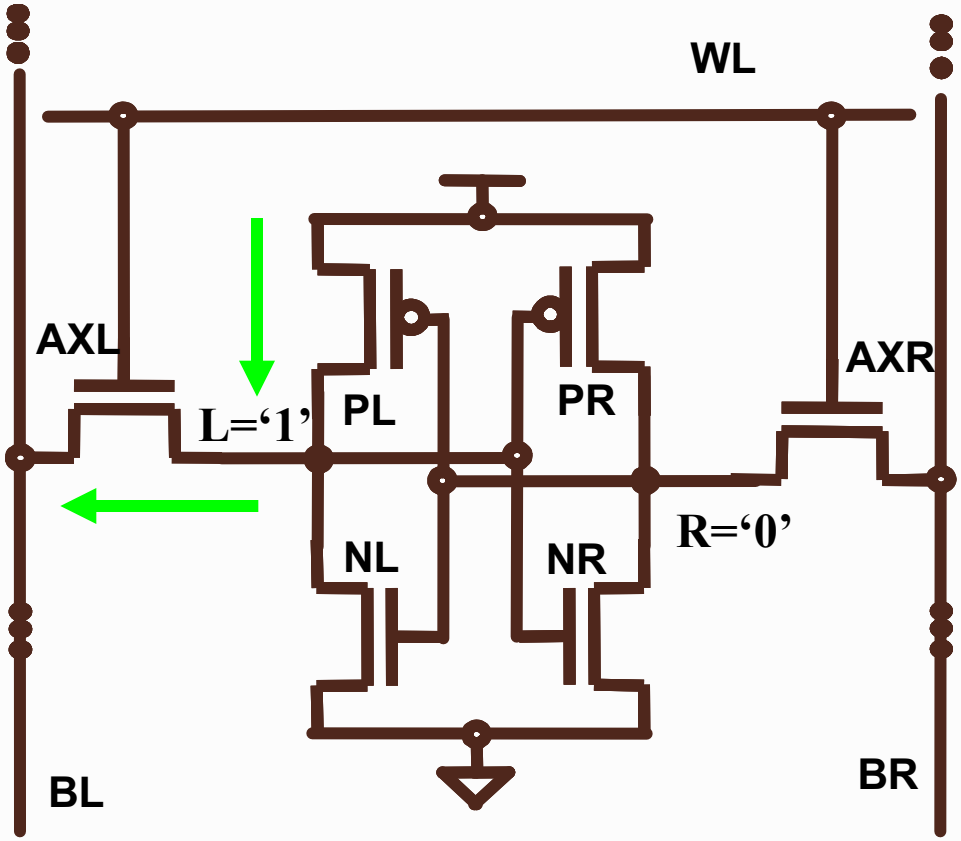


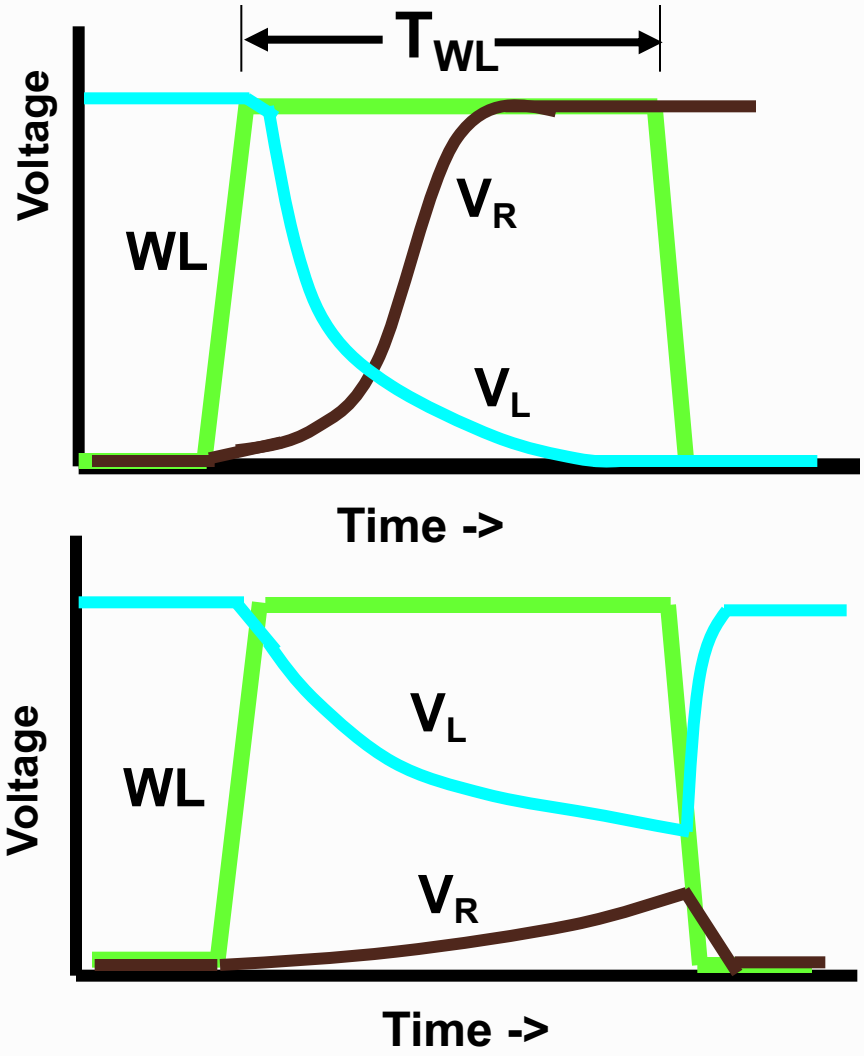
Read Failure



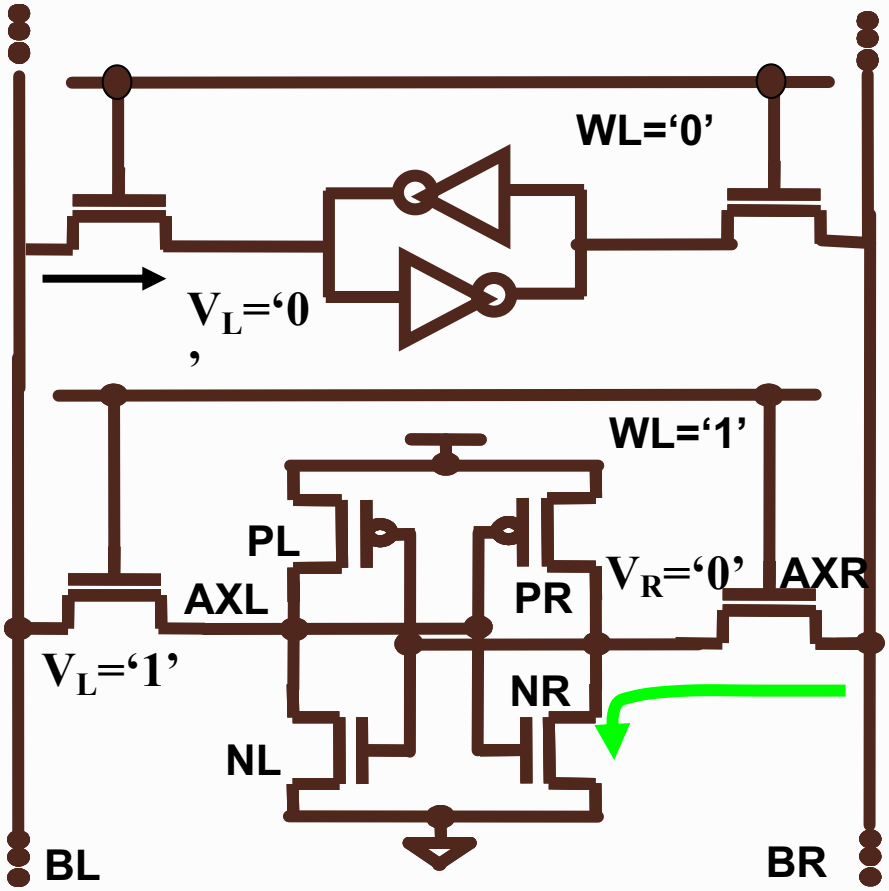


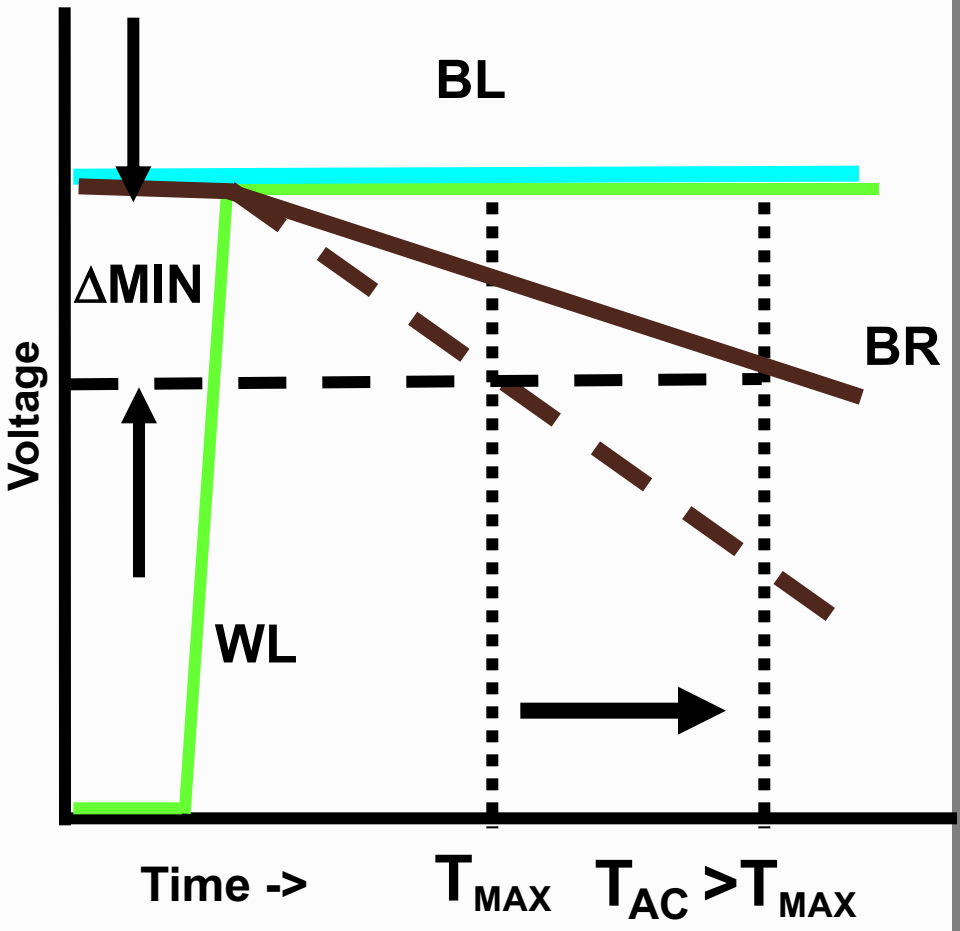
Write Failure



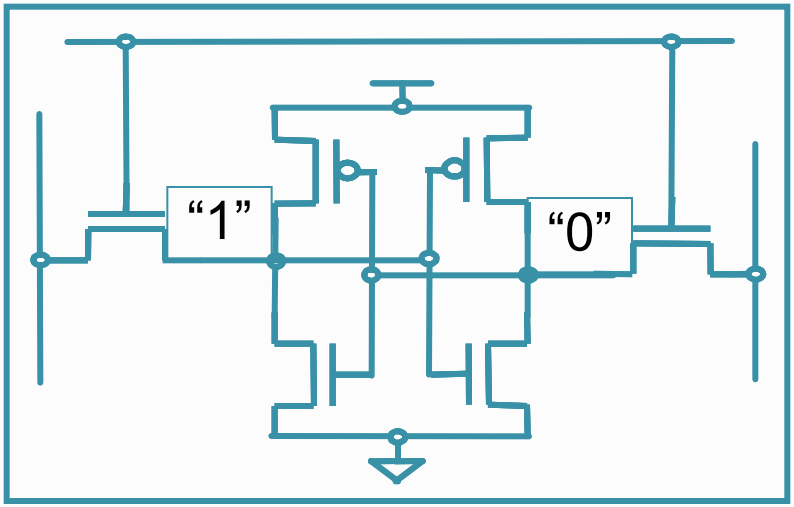


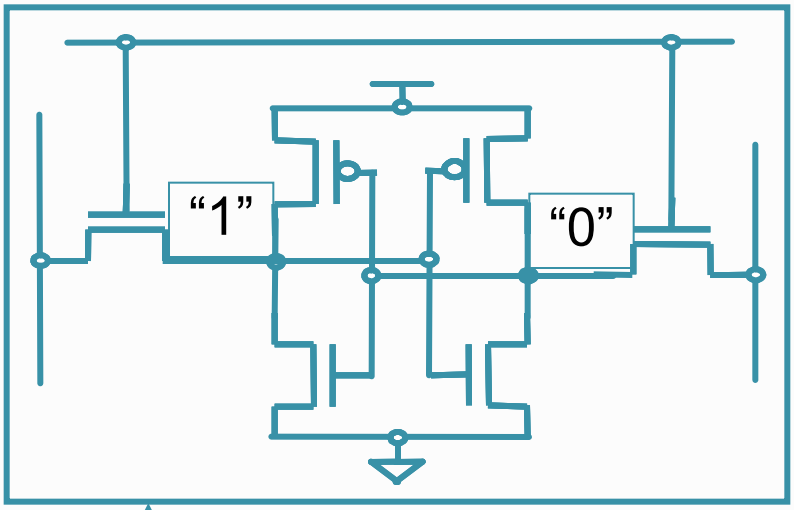
Access Failure

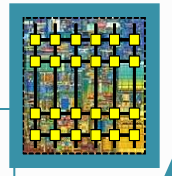


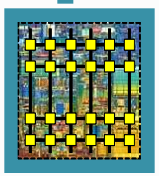


Inter-die Variation & Cell Failures









Low–Vt Corners
- Read failure ↑
- Hold failure ↑

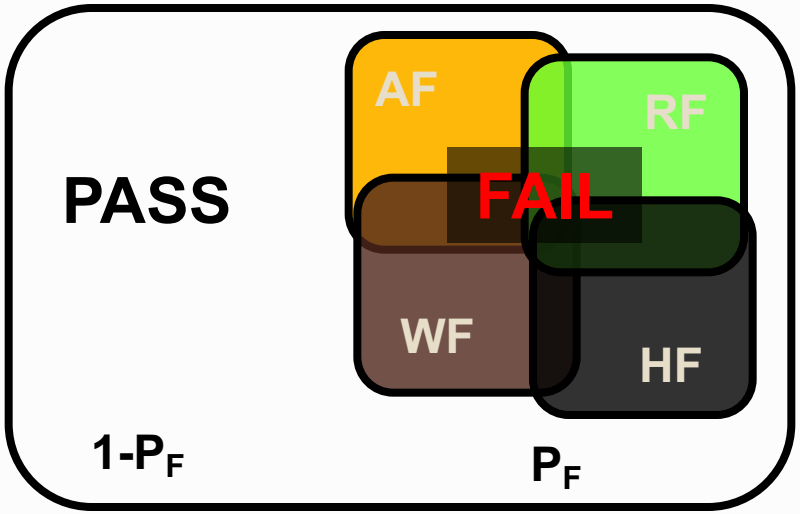
High–Vt Corners
- Access failure ↑
- Write failure ↑

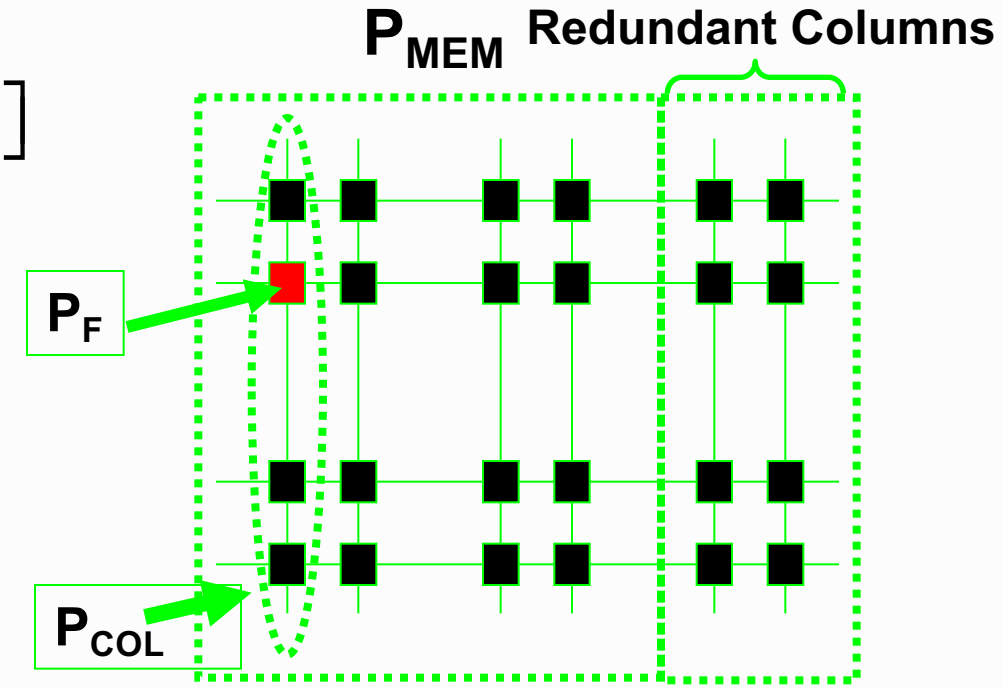
S. Mukhopadhyay et. al, ITC2005, VLSI2006, JSSC2007, TCAD2008

Failures in SRAM Array

Overall Cell Failure:

$$P_F = P[Fail] = P[A_F \cup R_F \cup W_F \cup H_F]$$

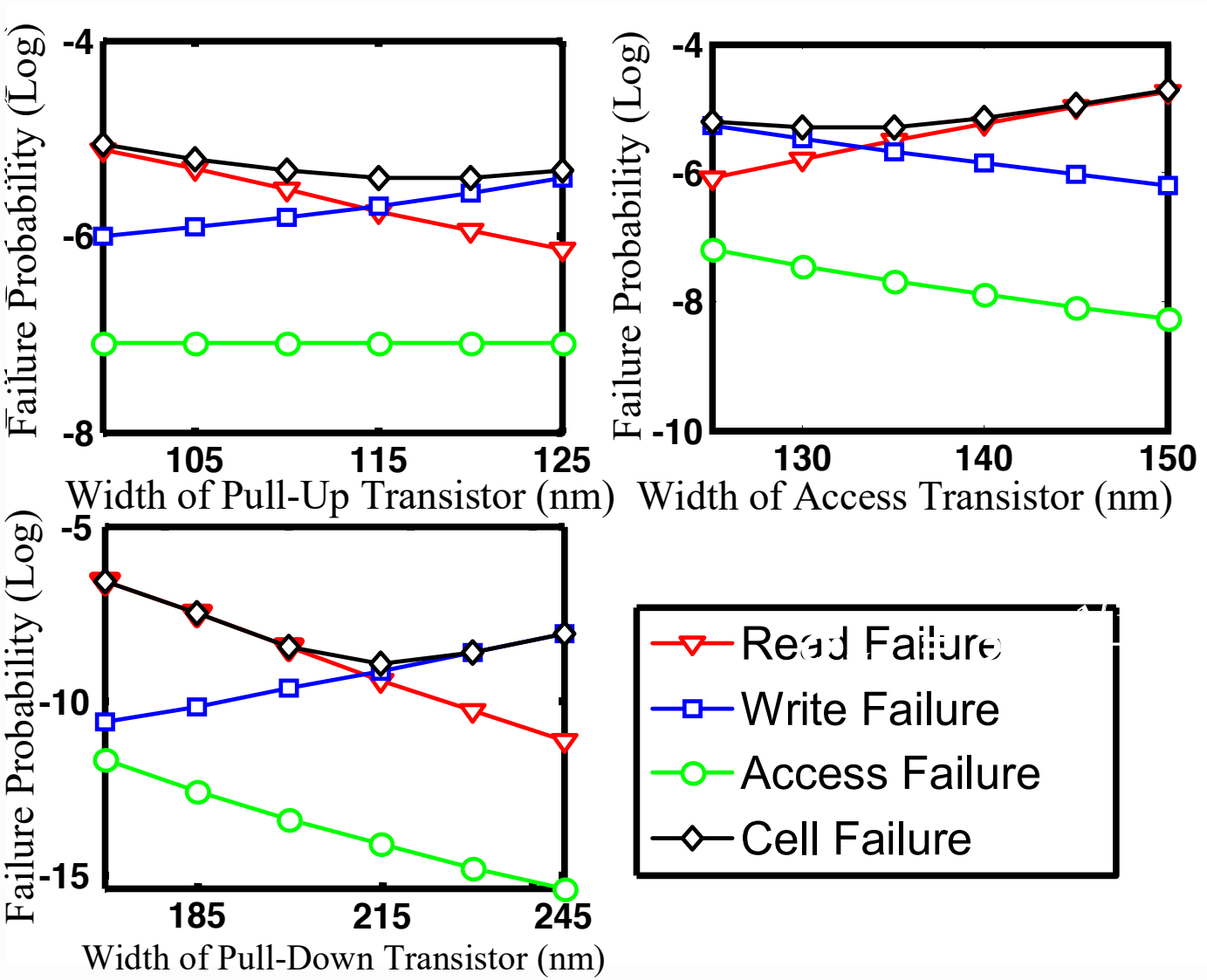




- P_{COL}: Probability that any of the cells in a column fail

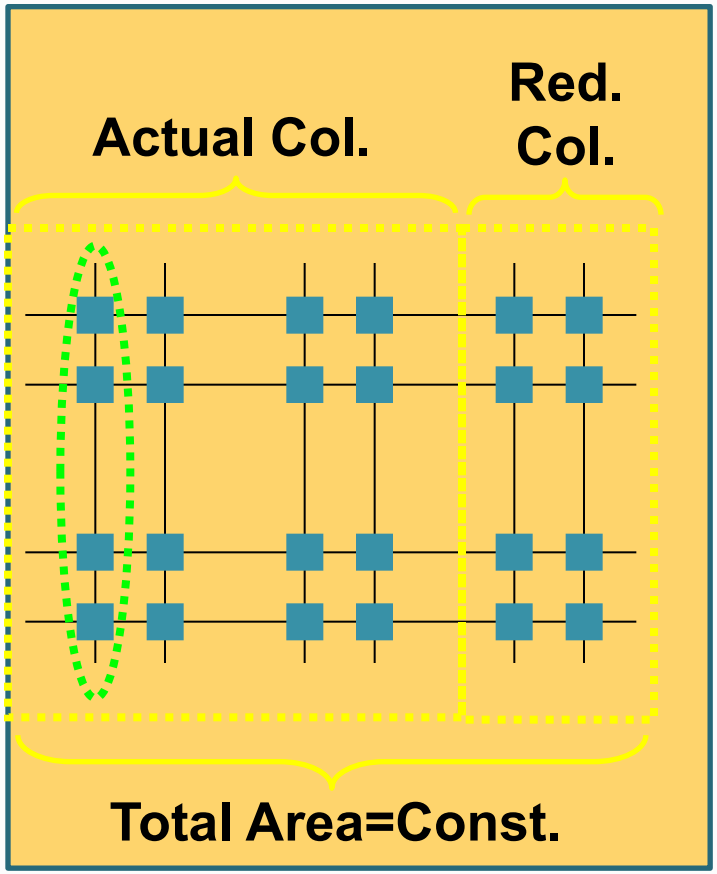
$$P_{COL} = 1 - (1 - P_F)^{N_{ROW}}$$

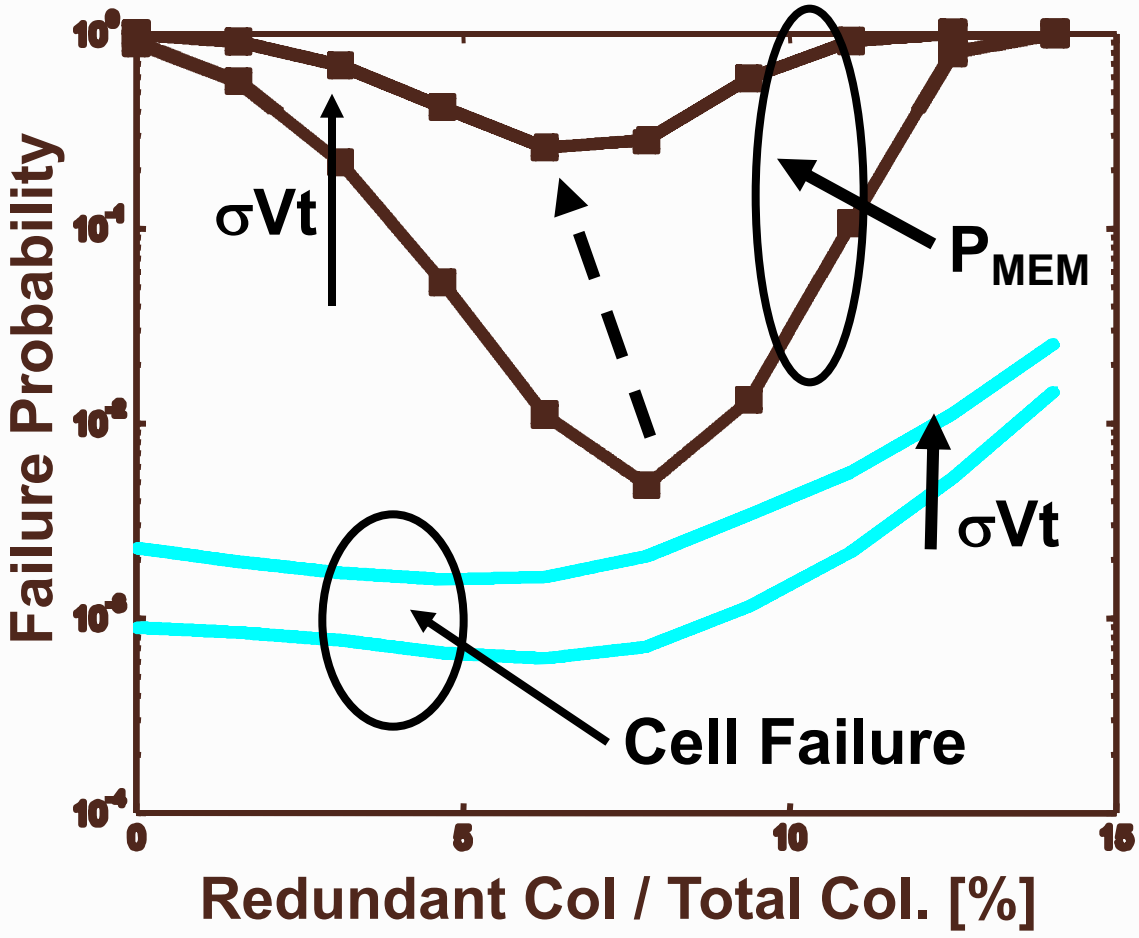
Transistor Sizing



- Slide contributed by K. Roy, Purdue

Impact of Redundancy on Memory Failure





Larger redundancy

(1) more column to replace (less memory failure).

(2) smaller cell area (larger cell failure).

Question

- Array redundancy

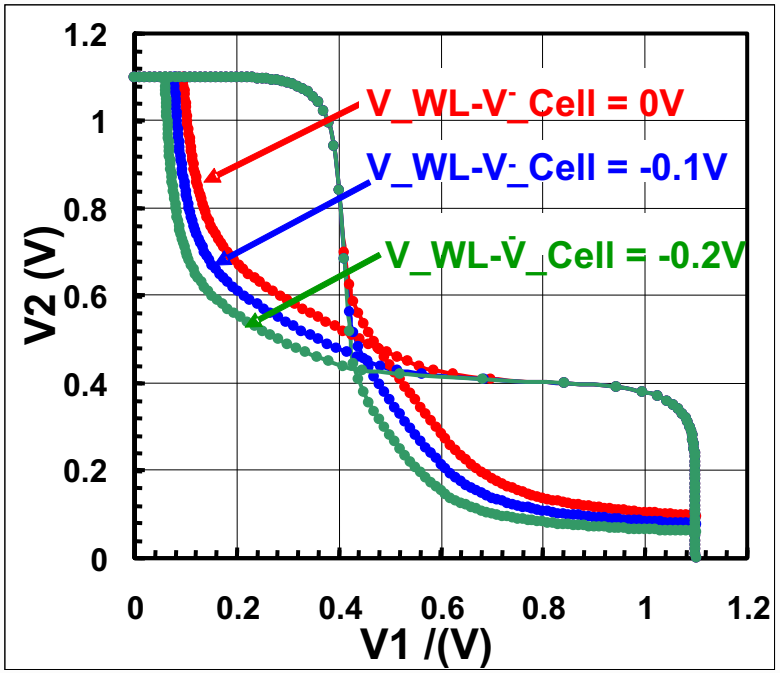
a) Improves cell stability

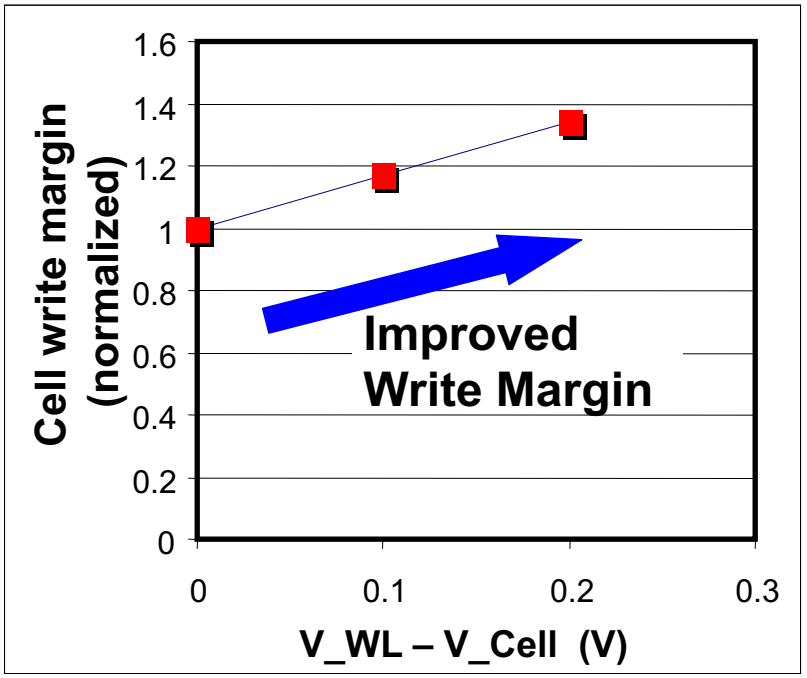
b) Degrades cell performance (i.e increases read and write times)

c) Does not require any change to cell peripheral circuits

d) Row redundancy is better than column redundancy

Example: Multi-VCC for SRAM Cell





- Create differential voltage between WL and Cell to decouple the Read & Write
  - Write: V_WL > V_Cell
  - Read: V_WL < V_Cell

Source: K. Zhang et. al. ISSCC 2005