Advanced Topics in VLSI

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Queries

- Sense Amplifier and Hierarchical Bit-Lines

BL = VDD

BR = VDD- ΔV

Sense

Q

ϕ

word 0

SRAM Cell

lbl 0

Keeper

word b – 1

Q0

Q1

H

lbl 1

More Local Bitlines

Q2

Q3

H

Keeper

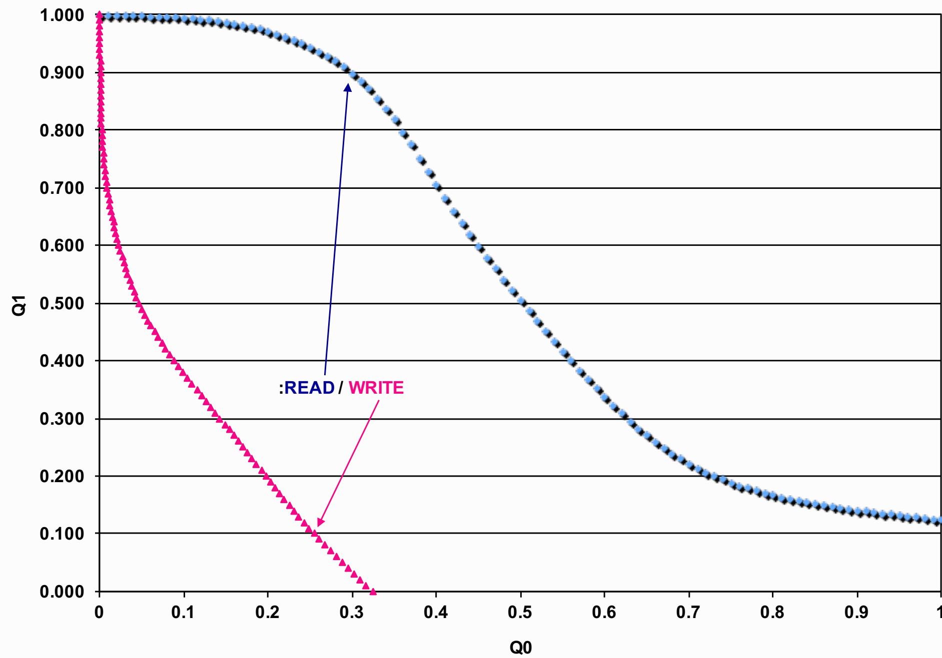
gbl

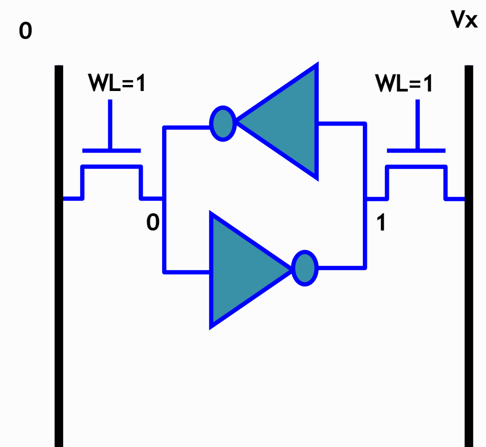
H

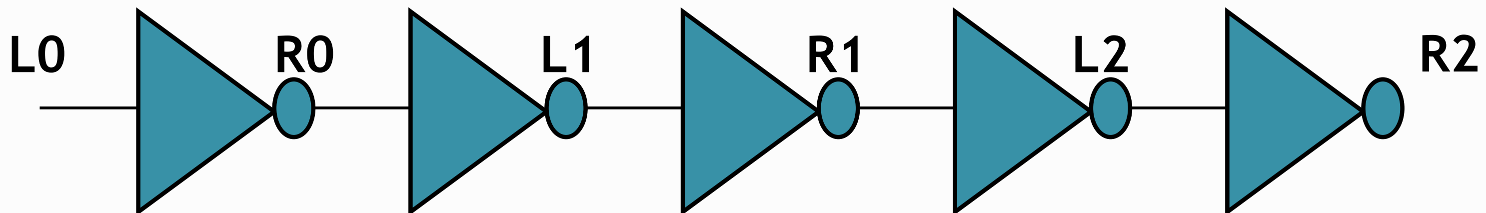
out

Queries

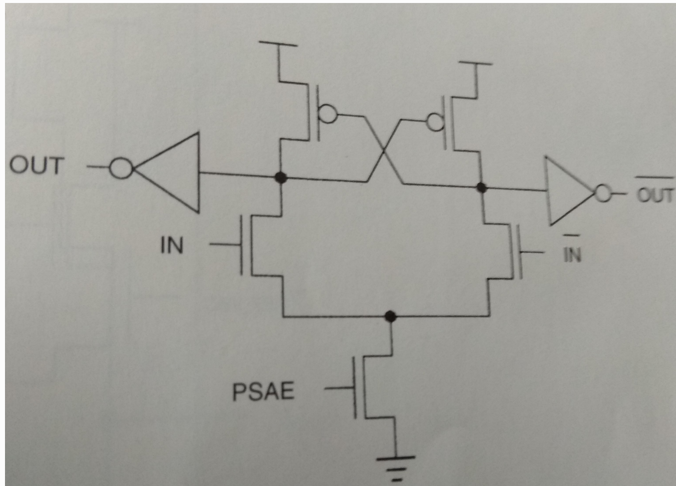
- Write Margin (and alternate definition)



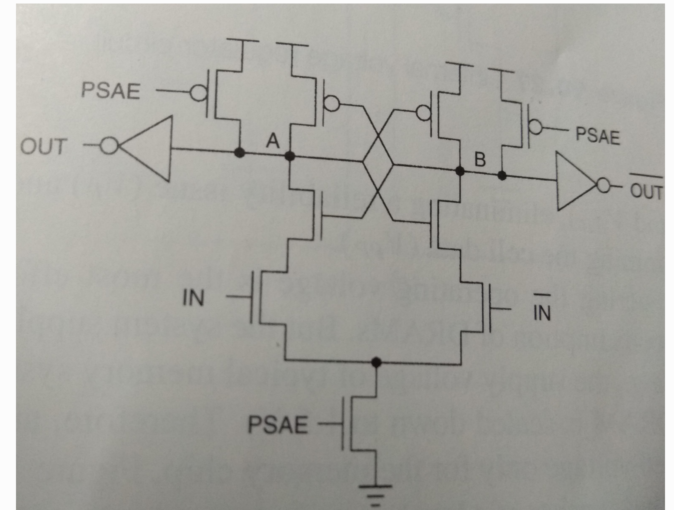




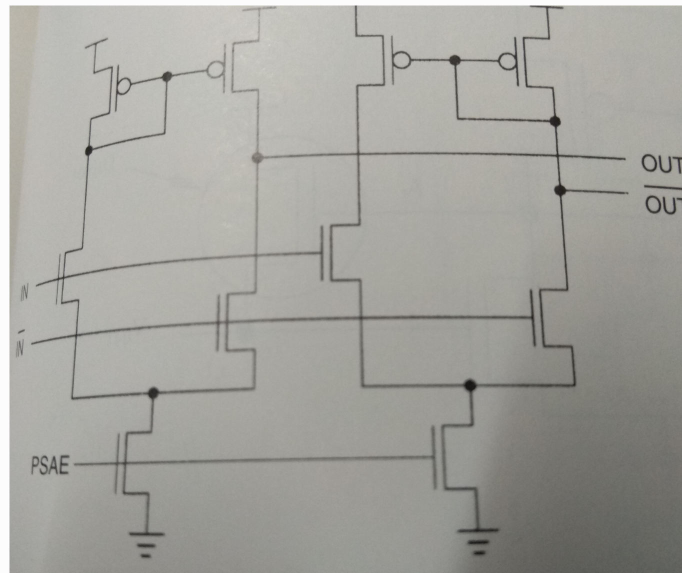
Sense Amplifiers (Alternate)



Half Latch Based



Full Differential



Current Mirror Based

This Class

- Memory Arrangement & Timing Diagrams
- Alternative Cell Types (6 to 10T)

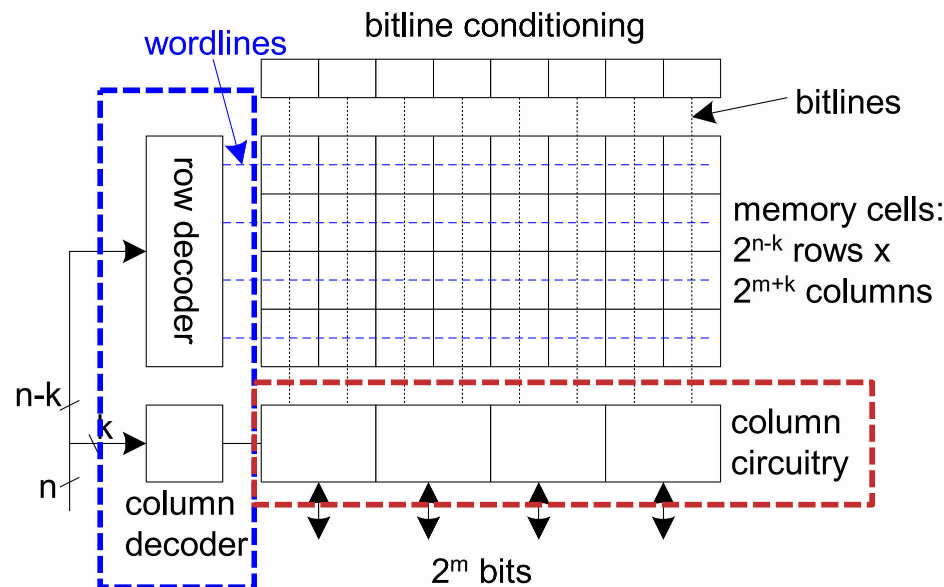
Memory Architecture

- Array of 2^k bits => K address bits?

	0	1	2	3	4	5	6	7
0	0	1	2	3	4	5	6	7
1	8	9	10	11	12	13	14	15
2	16	17	18	19	20	21	22	23
3	24	25	26	27	28	29	30	31
4	32	33	34	35	36	37	38	39
5	40	41	42	43	44	45	46	47
6	48	49	50	51	52	53	54	55
7	56	57	58	59	60	61	62	63
8	64	65	66	67	68	69	70	71
9	72	73	74	75	76	77	78	79
10	80	81	82	83	84	85	86	87
11	88	89	90	91	92	93	94	95
12	96	97	98	99	100	101	102	103
13	104	105	106	107	108	109	110	111
14	112	113	114	115	116	117	118	119
15	120	121	122	123	124	125	126	127
16	128	129	130	131	132	133	134	135
17	136	137	138	139	140	141	142	143
18	144	145	146	147	148	149	150	151
19	152	153	154	155	156	157	158	159
20	160	161	162	163	164	165	166	167
21	168	169	170	171	172	173	174	175
22	176	177	178	179	180	181	182	183
23	184	185	186	187	188	189	190	191
24	192	193	194	195	196	197	198	199
25	200	201	202	203	204	205	206	207
26	208	209	210	211	212	213	214	215
27	216	217	218	219	220	221	222	223
28	224	225	226	227	228	229	230	231
29	232	233	234	235	236	237	238	239
30	240	241	242	243	244	245	246	247
31	248	249	250	251	252	253	254	255
	SA	SA	SA	SA	SA	SA	SA	SA

Memory Architecture

- 2^n *words* of 2^m *bits* each, If n >> m, fold by 2^k into fewer *rows* of more *columns*



For read & write: NFET only based ?

- Good regularity – easy to design
- Utilization = Cell Area / (Cell + Periphery Area)

Memory Folding

	0	1	2	3	4	5	6	7
0	0	1	2	3	4	5	6	7
1	8	9	10	11	12	13	14	15
2	16	17	18	19	20	21	22	23
3	24	25	26	27	28	29	30	31
4	32	33	34	35	36	37	38	39
5	40	41	42	43	44	45	46	47
6	48	49	50	51	52	53	54	55
7	56	57	58	59	60	61	62	63
8	64	65	66	67	68	69	70	71
9	72	73	74	75	76	77	78	79
10	80	81	82	83	84	85	86	87
11	88	89	90	91	92	93	94	95
12	96	97	98	99	100	101	102	103
13	104	105	106	107	108	109	110	111
14	112	113	114	115	116	117	118	119
15	120	121	122	123	124	125	126	127
16	128	129	130	131	132	133	134	135
17	136	137	138	139	140	141	142	143
18	144	145	146	147	148	149	150	151
19	152	153	154	155	156	157	158	159
20	160	161	162	163	164	165	166	167
21	168	169	170	171	172	173	174	175
22	176	177	178	179	180	181	182	183
23	184	185	186	187	188	189	190	191
24	192	193	194	195	196	197	198	199
25	200	201	202	203	204	205	206	207
26	208	209	210	211	212	213	214	215
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28	224	225	226	227	228	229	230	231
29	232	233	234	235	236	237	238	239
30	240	241	242	243	244	245	246	247
31	248	249	250	251	252	253	254	255
	SA	SA	SA	SA	SA	SA	SA	SA

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
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240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
2:1 Mux		2:1 Mux		2:1 Mux		2:1 Mux		2:1 Mux		2:1 Mux		2:1 Mux		2:1 Mux	
SA		SA		SA		SA		SA		SA		SA		SA	

Hierarchical Word Line

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
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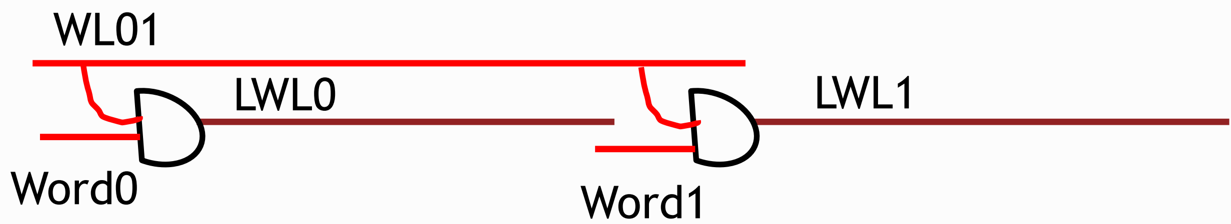
2:1 Mux		2:1 Mux		2:1 Mux		2:1 Mux		2:1 Mux		2:1 Mux		2:1 Mux		2:1 Mux	
SA		SA		SA		SA		SA		SA		SA		SA	



Why memory is folded?

- To improve aspect ratio by column multiplexing
  - E.g.: 2Kword x 16 can be arranged as 256 rows and 128 columns
  - 8:1 MUX are used to read 16 desired columns out of 128
- To improve soft-error immunity
  - bits of a word are not placed next to each other
    - Single-bit soft-error can be corrected by ECC

Bit Interleaving

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
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2:1 Mux		2:1 Mux		2:1 Mux		2:1 Mux		2:1 Mux		2:1 Mux		2:1 Mux		2:1 Mux	
SA		SA		SA		SA		SA		SA		SA		SA	

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	8	1	9	2	10	3	11	4	12	5	13	6	14	7	15
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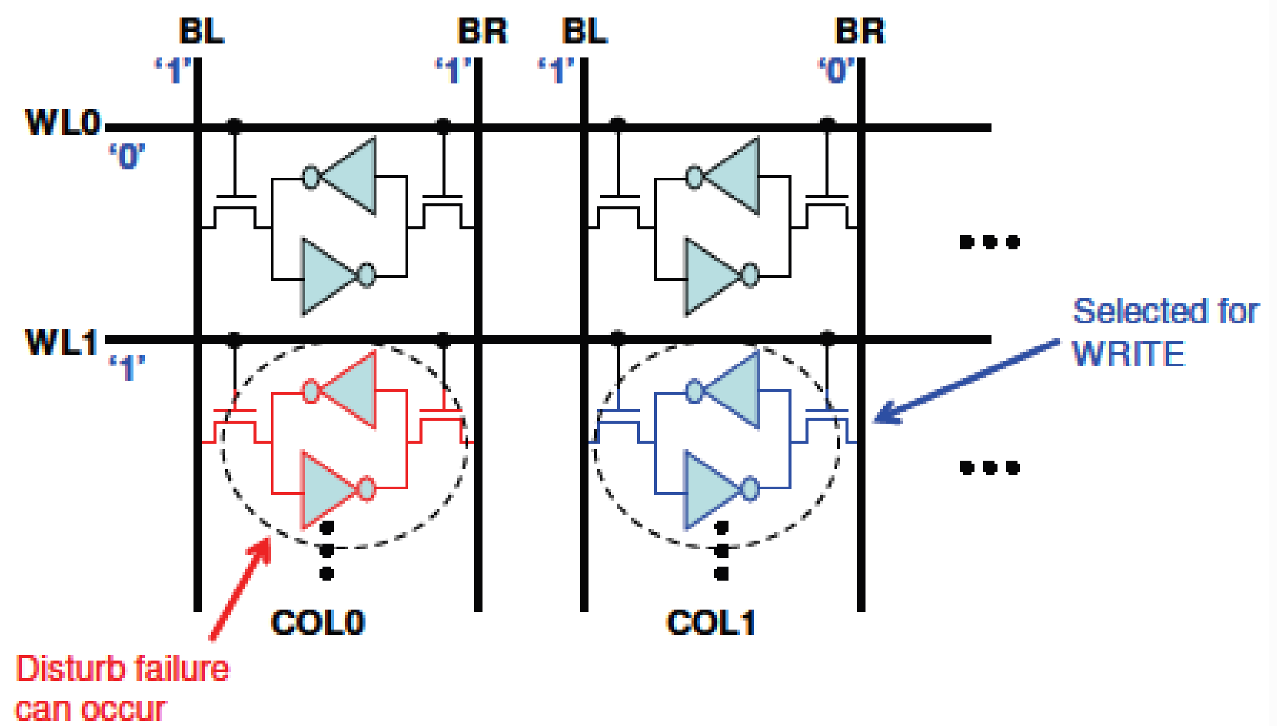
240	248	241	249	242	250	243	251	244	252	245	253	246	254	247	255
2:1 Mux		2:1 Mux		2:1 Mux		2:1 Mux		2:1 Mux		2:1 Mux		2:1 Mux		2:1 Mux	
SA		SA		SA		SA		SA		SA		SA		SA	

- Easier to fit SA in the width of 'N' bit cells, rather than 1 (as in the case of unfolded memory)

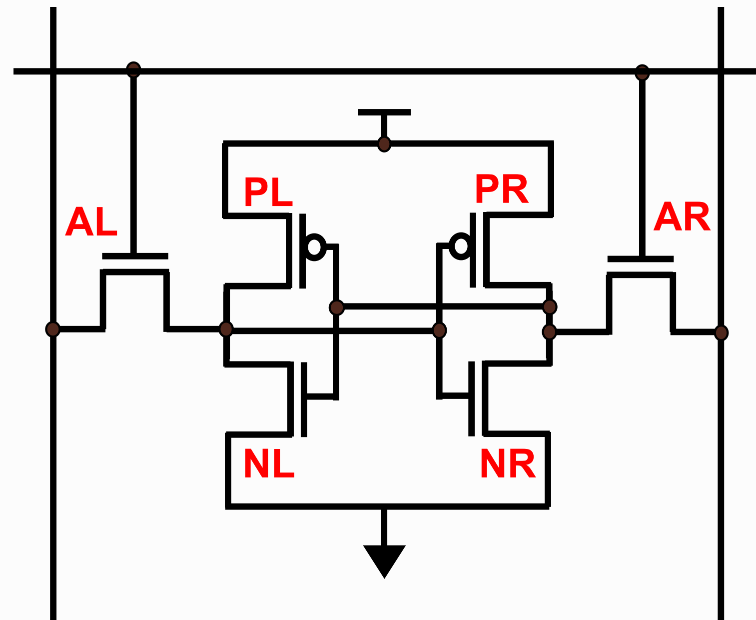
Column Select and Half-Select Issue

Prevents multiple-bit soft error

Better aspect ratio



The Balancing Act

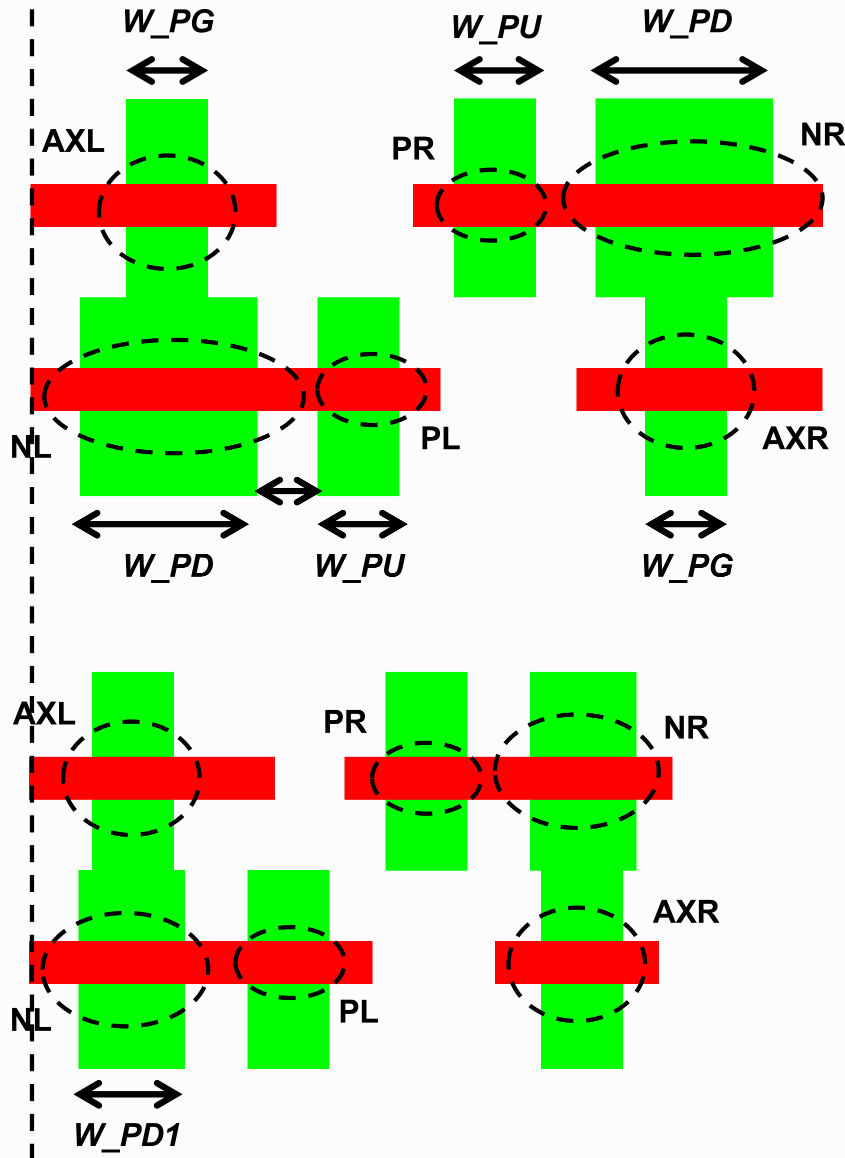


Large N: Better READ performance. If too large, trip voltage of inverter becomes so low that cell becomes unstable.

Large A: Better Performance. If too large, storage node voltage goes high during READ, causing cell flip

Large P: Increase stability. If too large, hard to WRITE

High Performance vs Dense Cells



High-Performance and READ stable

- $W_{PD} >> W_{PG}$ for READ stability
- Low READ access time
- Large cell footprint
- Less RDF induced V_T fluctuation in PD
- Microprocessors etc.

Dense and WRITE stable

- $W_{PD} \sim W_{PG}$ for WRITE stability
- Large READ access time
- Small cell footprint
- Large RDF induced V_T fluctuation in PD
- Dense applications – PDA etc.
- Maintain read stability by preventing increasing Vmin_cell (dual supply arrays)

(A. Bansal, IRPS 2009)

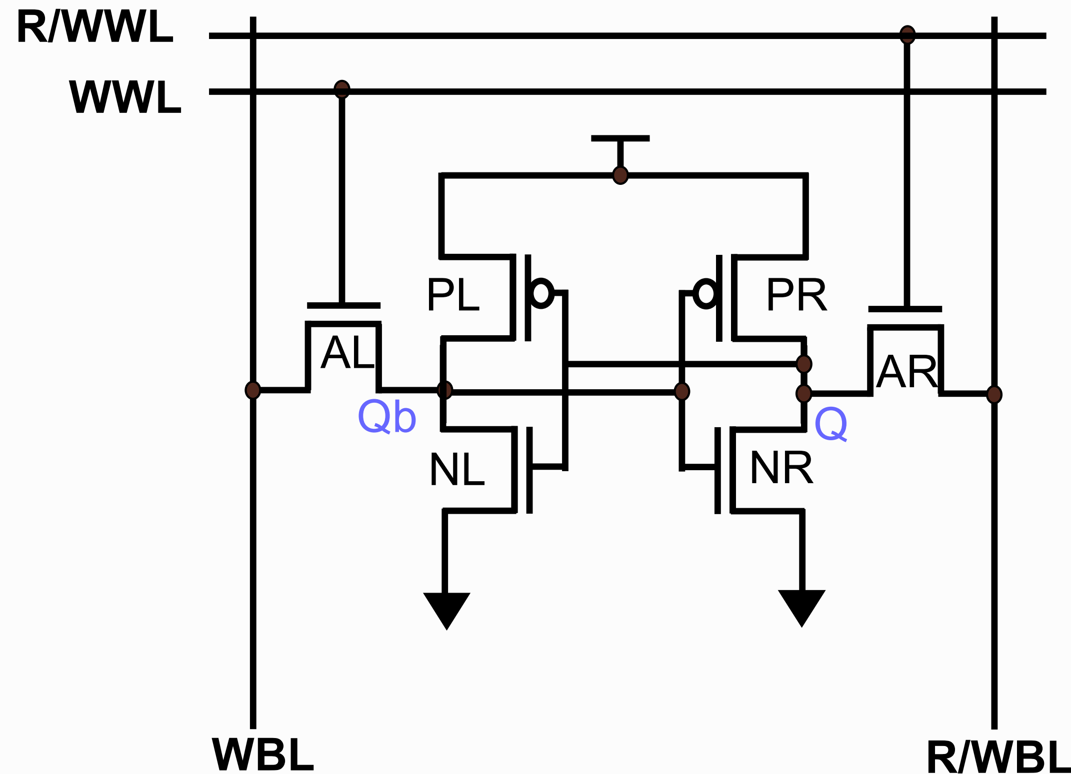
Topics

- ❑ Alternative Cell Types (6 to 10T), Asymmetric Cells, Sub-threshold Cells, Low – leakage cells

Modified to

- ❑ Alternative Cell Types
  - ❑Split word line with single ended read
  - ❑Assymetric cells
  - ❑Decouple Read/Write Cells (8T Cells)
  - ❑Regenerative Feedback
- ❑Impact of Variation

6-T Single Ended Read



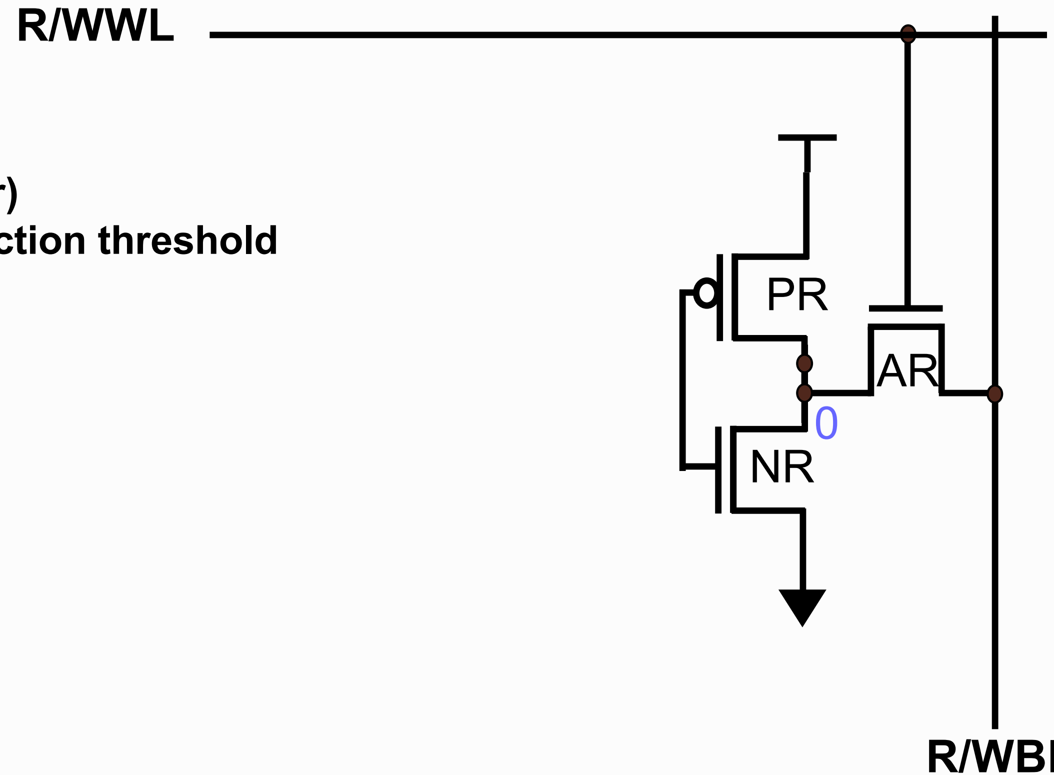
- Split word line for Read and Write
- Single-ended Read / Differential Write
- Full swing domino Read with short bit line

READ : R/WWL = VDD and WWL = GND

WRITE: R/WWL = VDD and WWL = VDD

Reduced bit-line swing

- **Duration of word-line being 'ON'**
  - **Sufficient for bit-line differential (or)**
  - **Sufficient for bit-line droop to detection threshold**



Refresher Question

- Decreasing the size of only one side of NFET transistors will improve the cell

a) **Cell density**

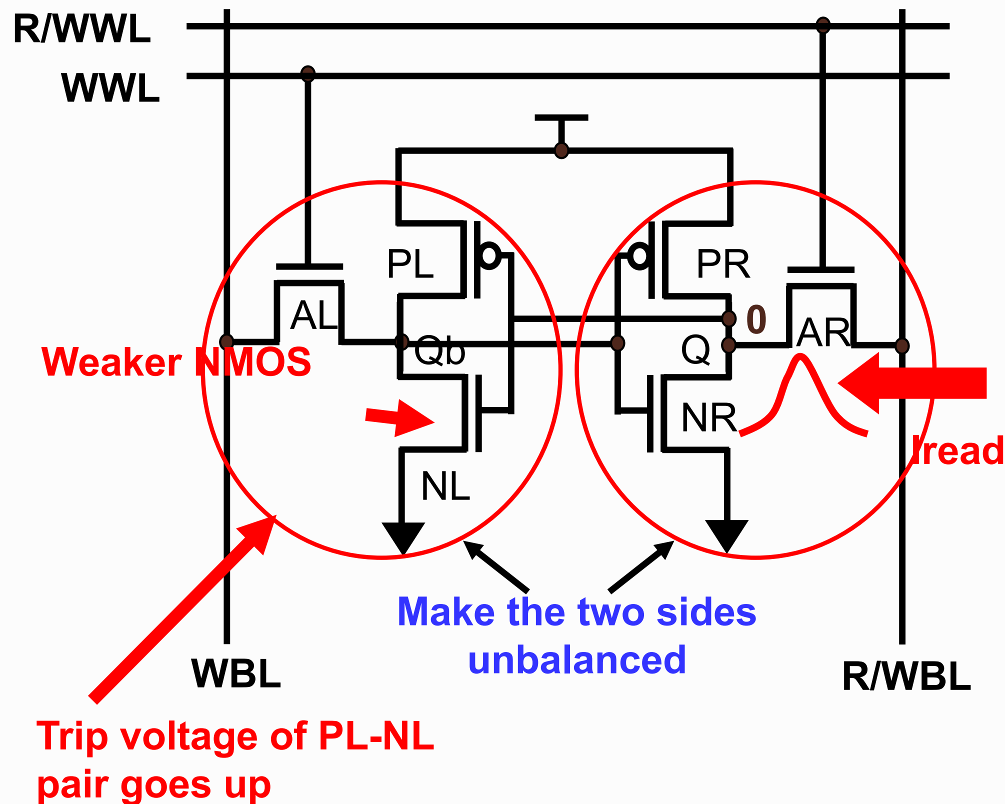
b) Read margin

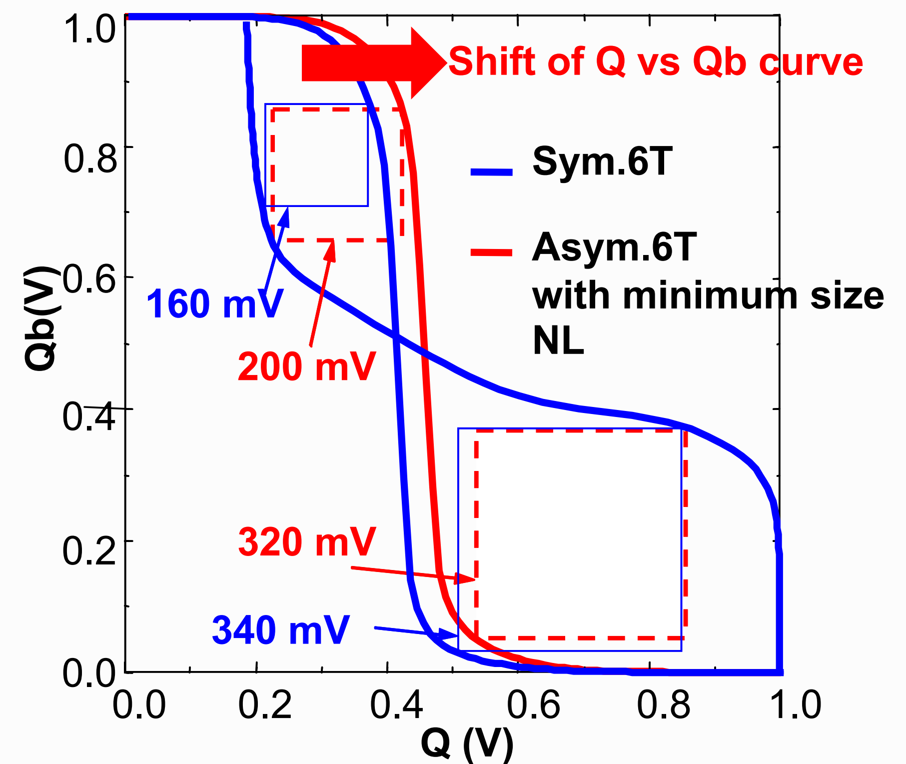
c) Write margin

d) Hold margin

Asymmetrical 6T SRAM: Device Sizing

- Read word-line separated from Write word-line
- Single-ended Read, differential Write





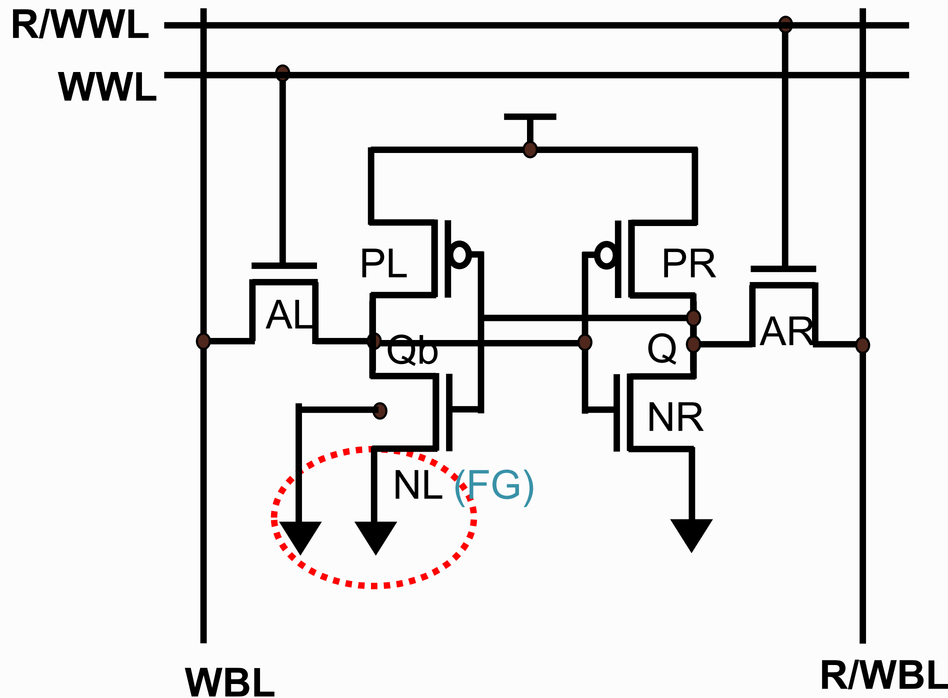
Asymmetry could be achieved through VT selection as well

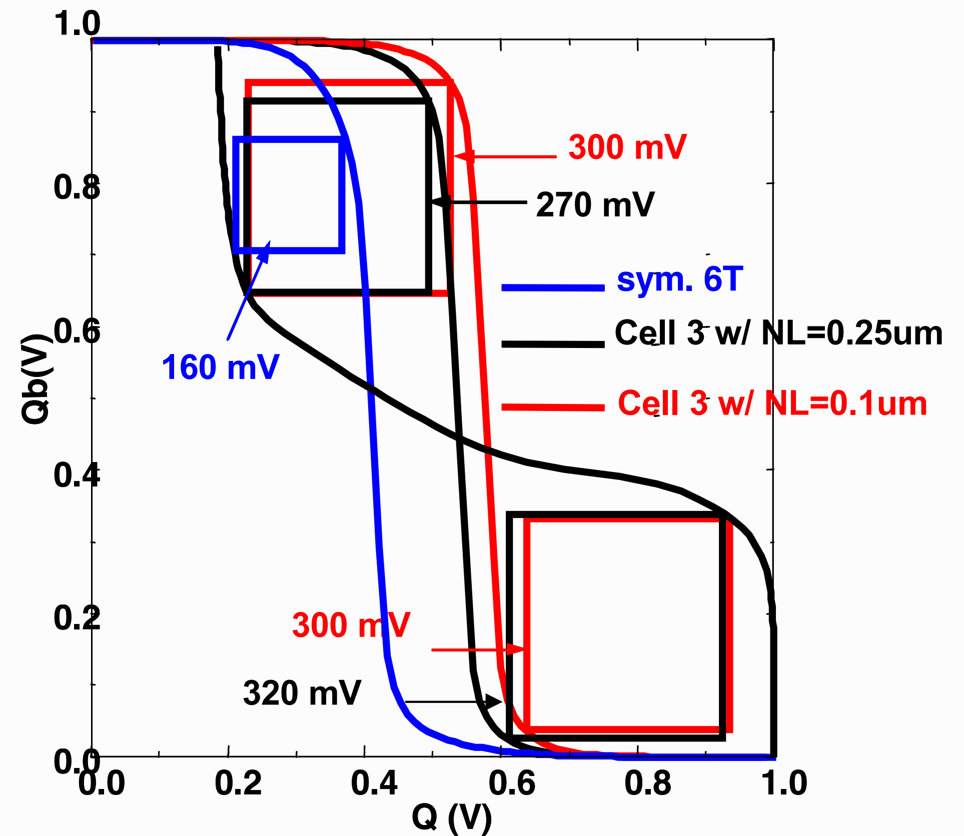
(J. Kim, ESSCIRC, 2006)

6T Asym SRAM in Double Gate Technologies

- Bias back-gate of NL to GND. Front-gate as cell device & sizing down NL
- Left and Right SNM become comparable

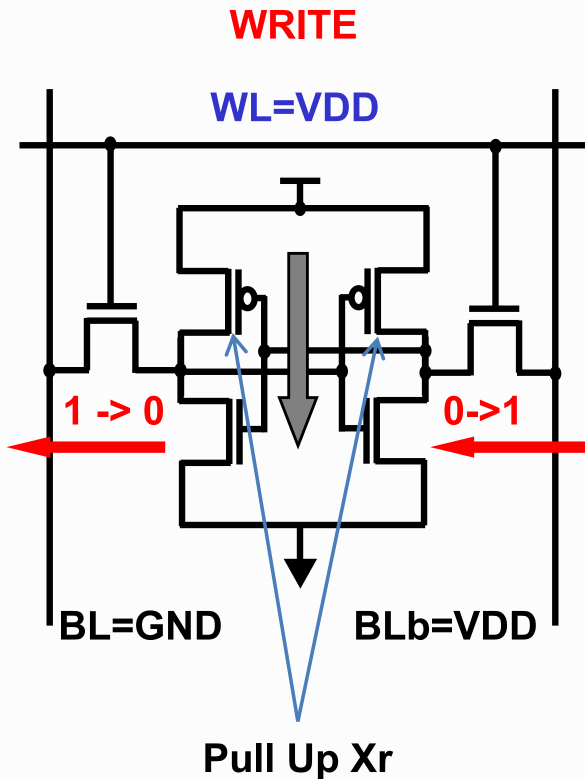
  Optimal SNM of asymmetrical cell

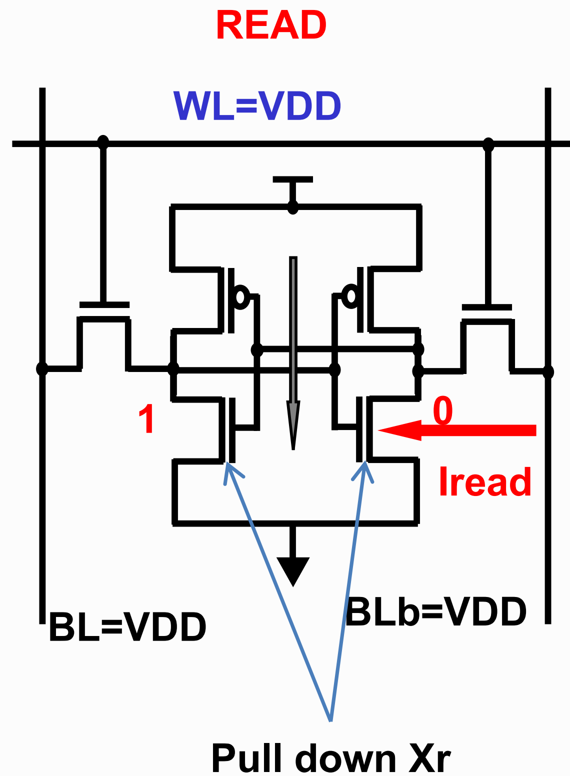


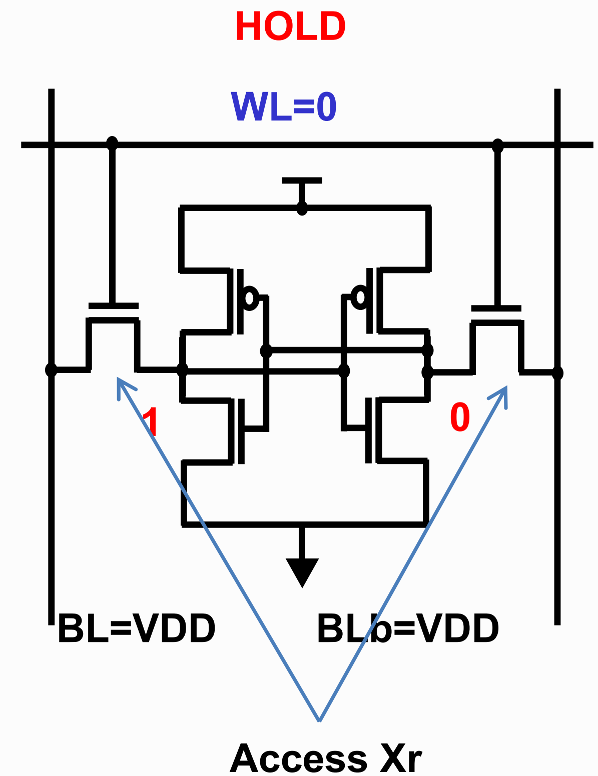


(J. J. Kim et al., ESSCIRC, 2006)

Workhorse 6T-Cell





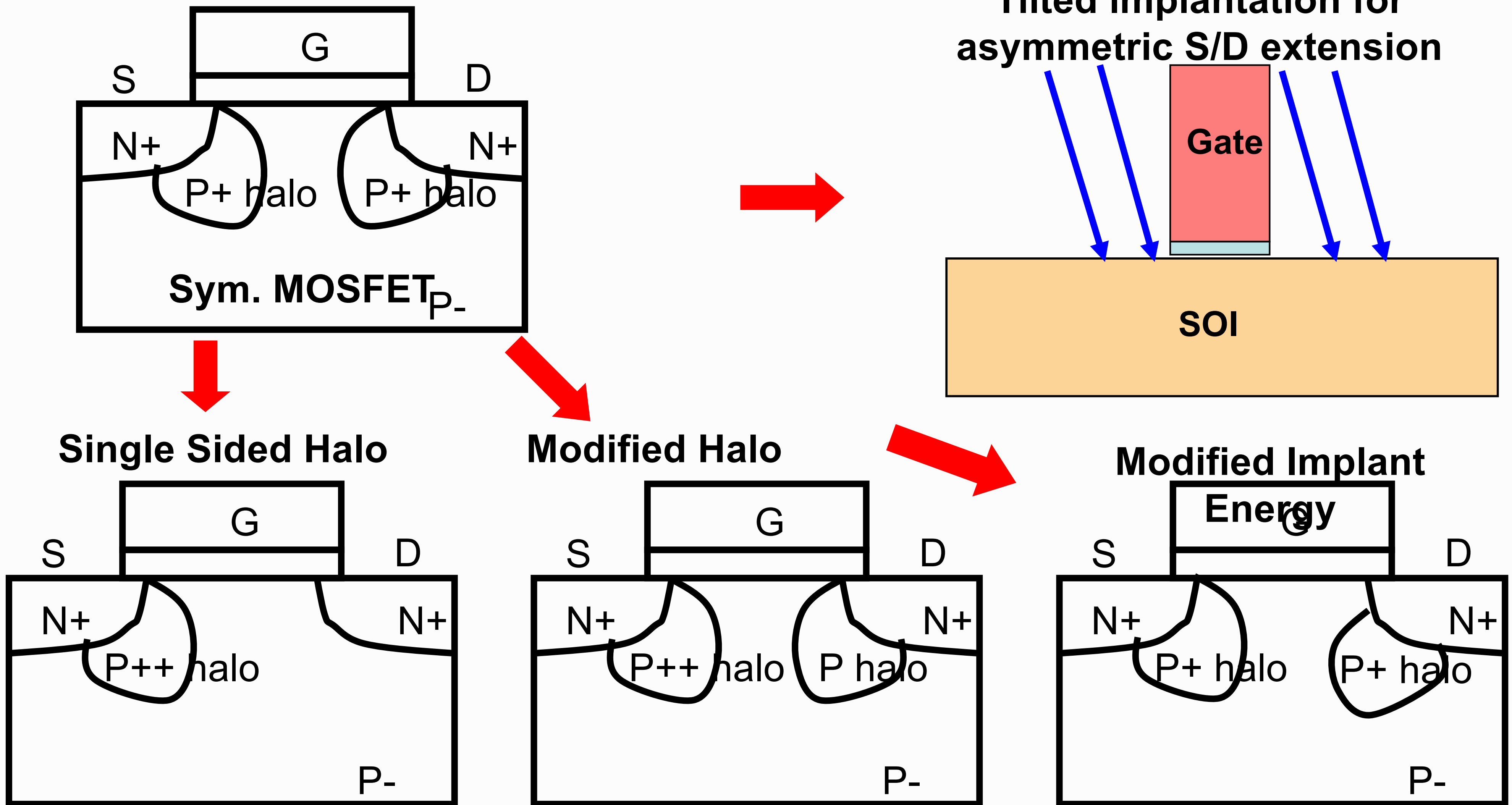


Access Xr: On
Data driven on bit - lines
Data Flipped by over-coming pull-up / pull – down Xrs

Acess Xr: On
BL, Blb pre-conditioned, and then floated, one line discharges thru the cell (Iread), voltage sensed, Data Retained

Access Xr : Off
Data Retained, due to back-to-back inverters

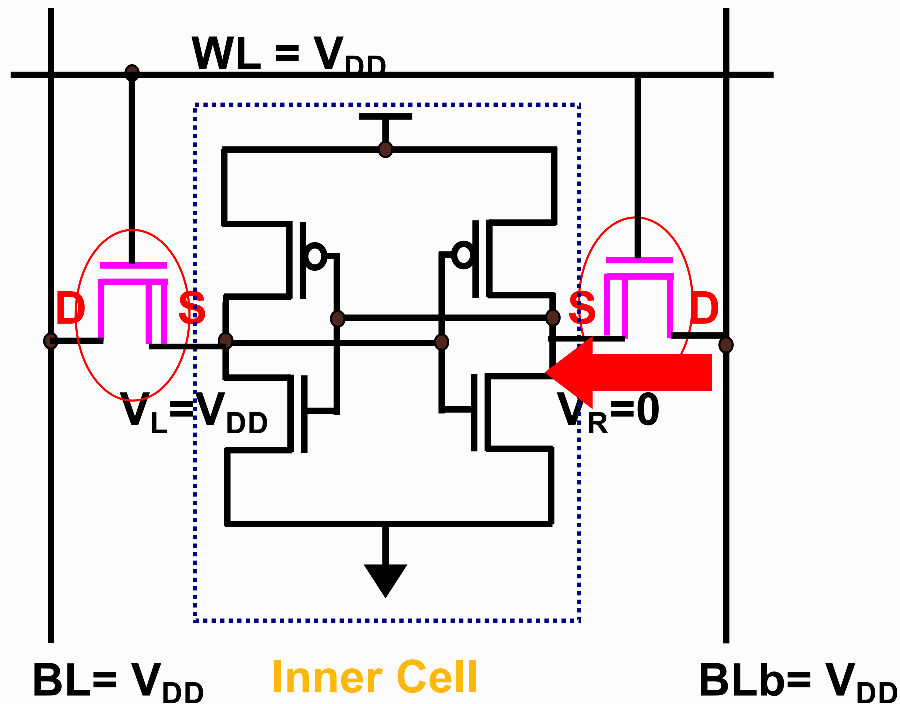
Asymmetric MOSFET

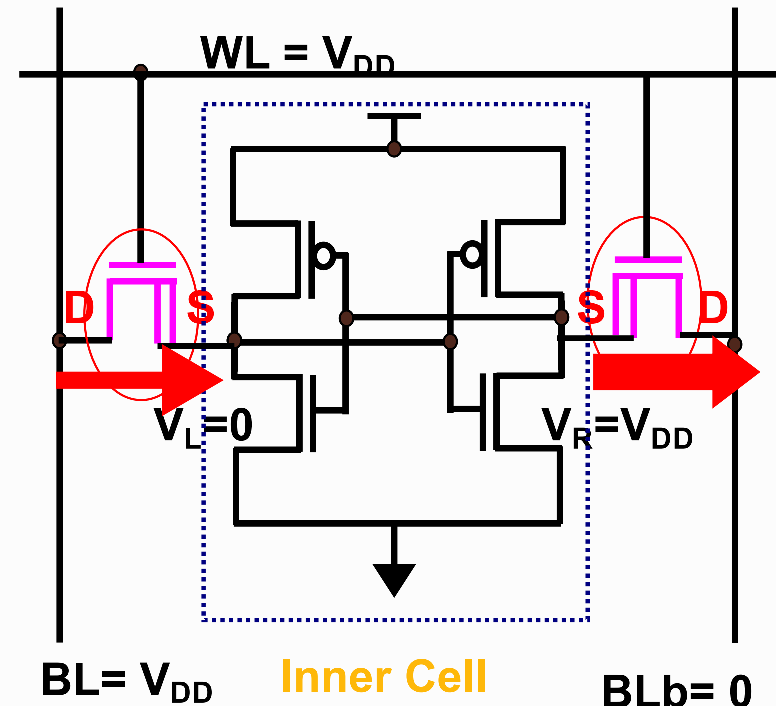


Asymmetric MOSFET can be realized in multiple ways

Net Effect: I (drain – source) ≠ I (source – drain)

Asymmetric Access Transistors





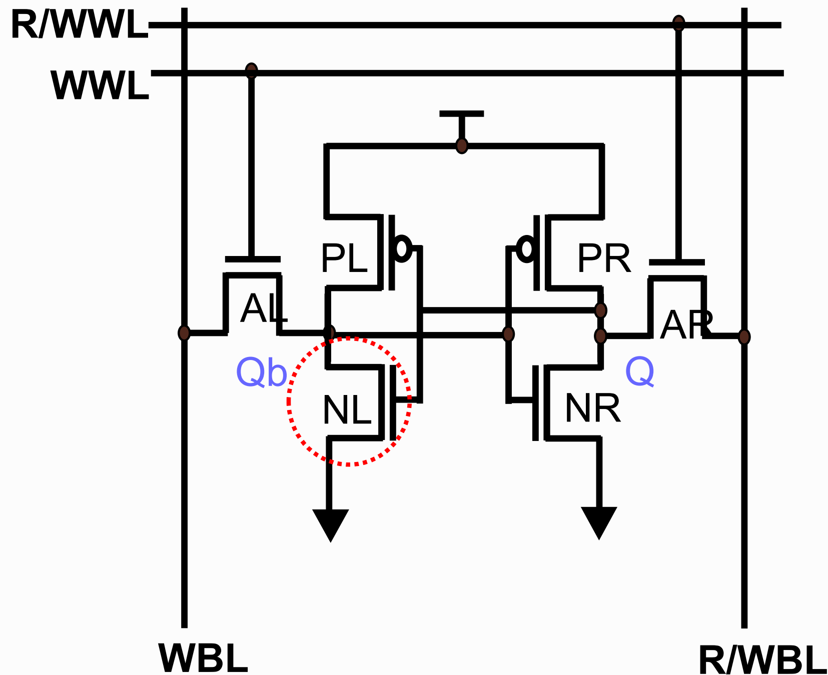
Read Operation

- Access Transistor in Fwd Mode
- Weaker than in Sym. Case
- Read Disturb Noise Reduced

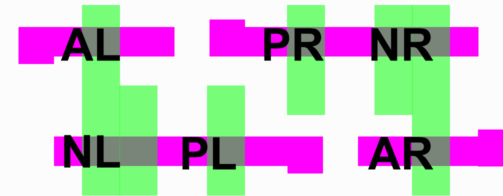
Write Operation

- L and R Access Transistor in Fwd and Rev Mode respectively

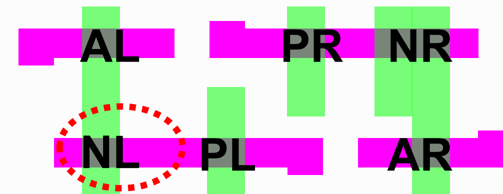
Asymmetric 6-T Cells



Sym

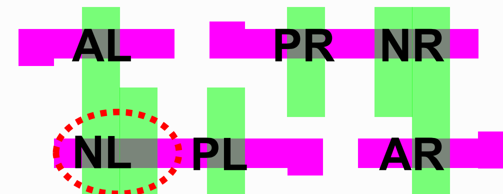


Asym Size



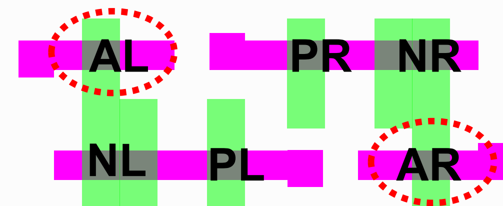
Straight Active region

Asym Vt



Higher Vt doping

Asym Device



S-D are distinct

(J. Kim, CICC 2010, J. Kim EDL 2011)

Question

- Which of the following is not true wrt asymmetric 6-T sram cell

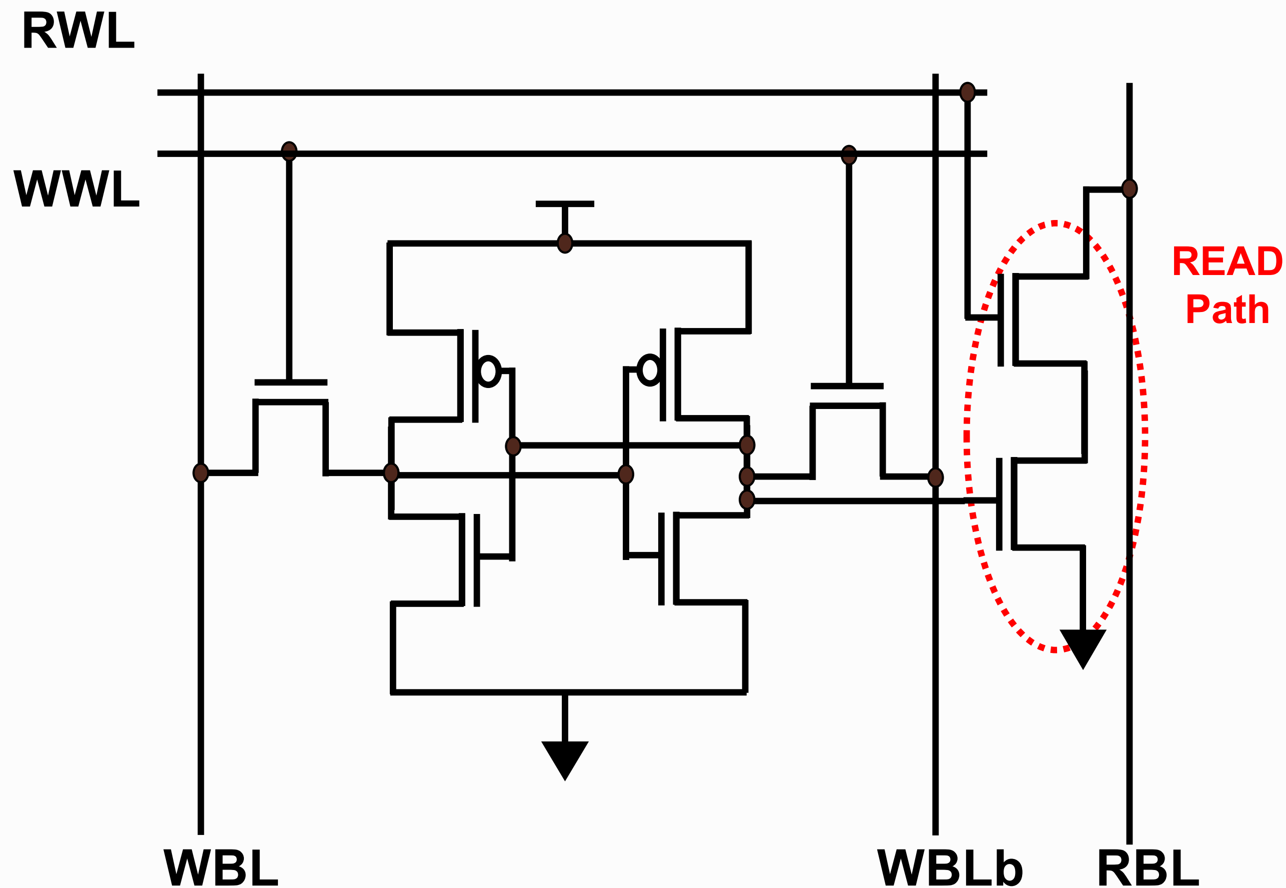
a) Assymetric transistors can be used for pull down and access transistors

b) Assymetric sizing based sram cell has reduced pull down width on the side opposite to the read bit-line

c) Assymetric VT based sram cell does not provide any area benefit

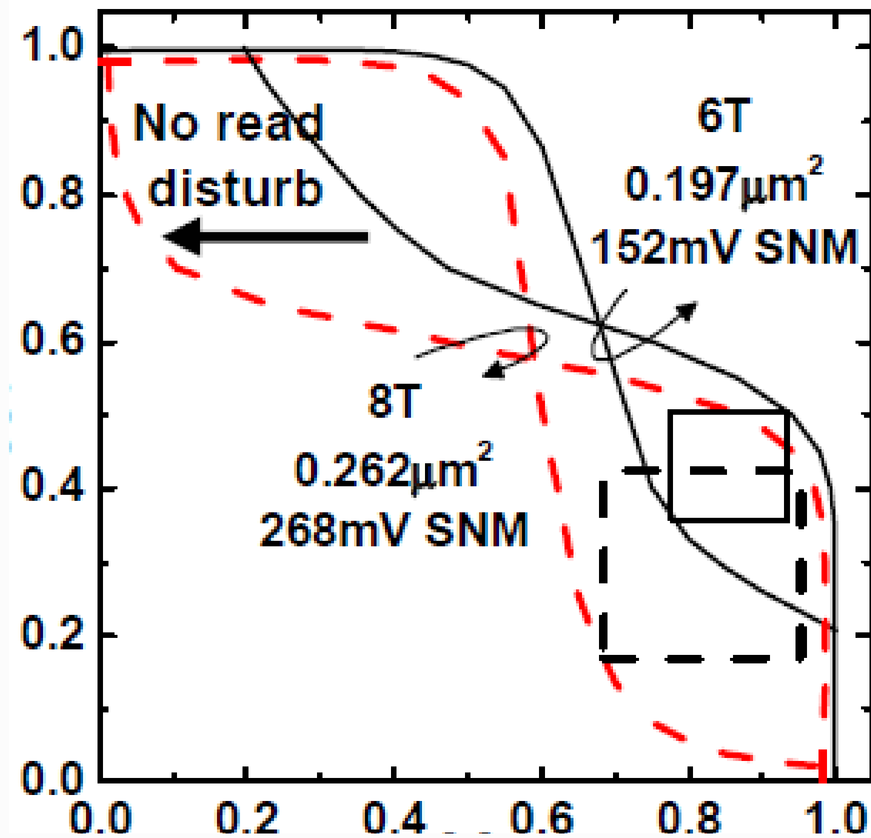
d) All asymmetric transistor sram cells need single ended read

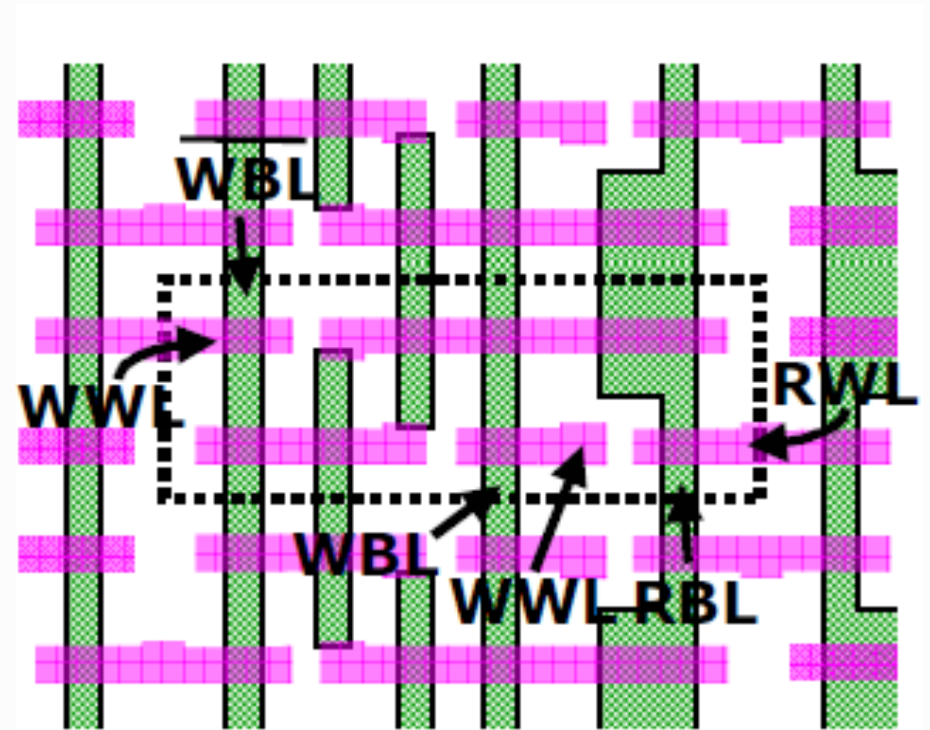
Decoupled Read – Write Bitlines



(L. Chang et al, VLSI Symp 05)

Decoupled Read – Write Bitlines

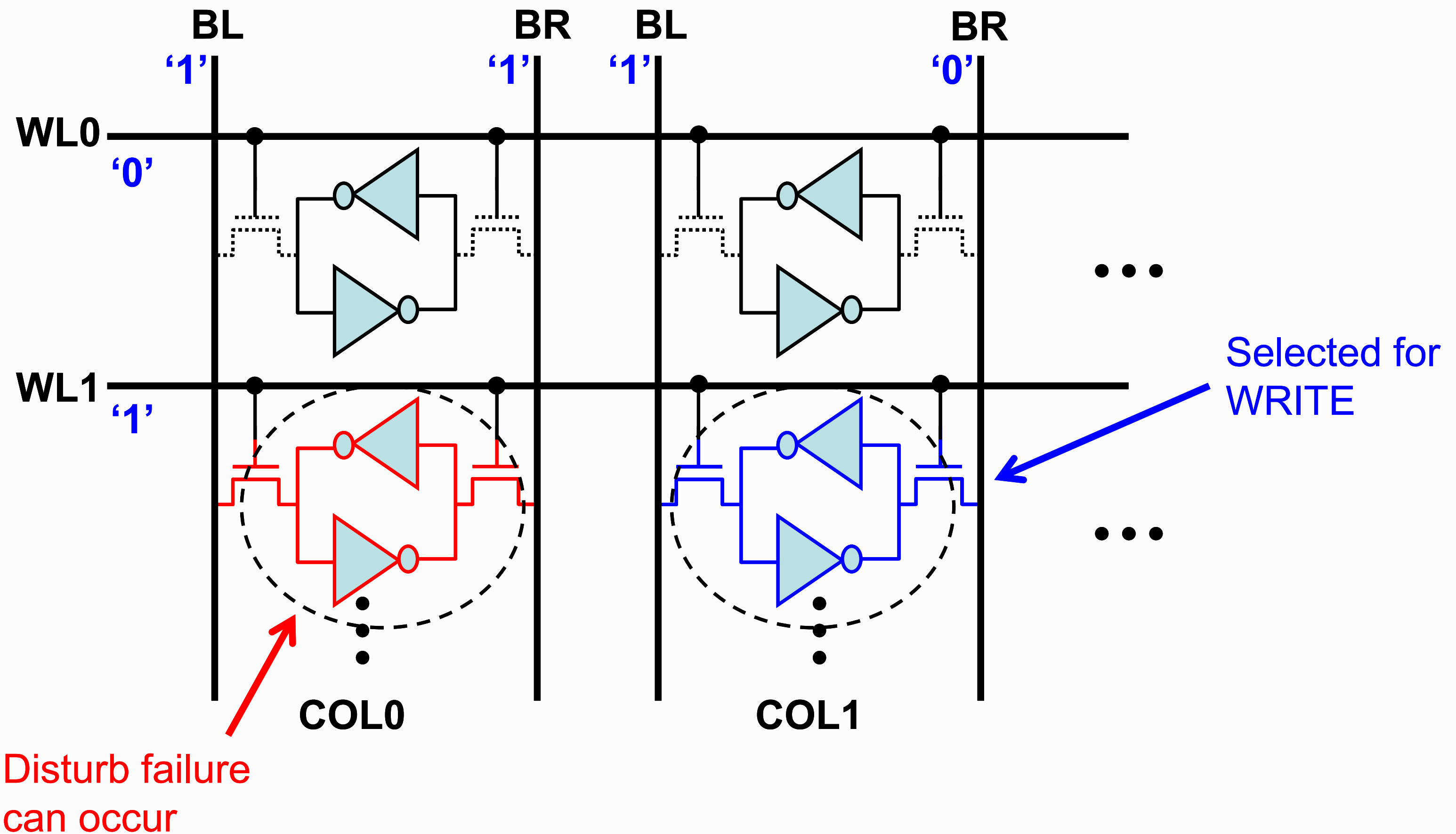




(L. Chang et al, VLSI Symp 05)

Half-Select Disturb

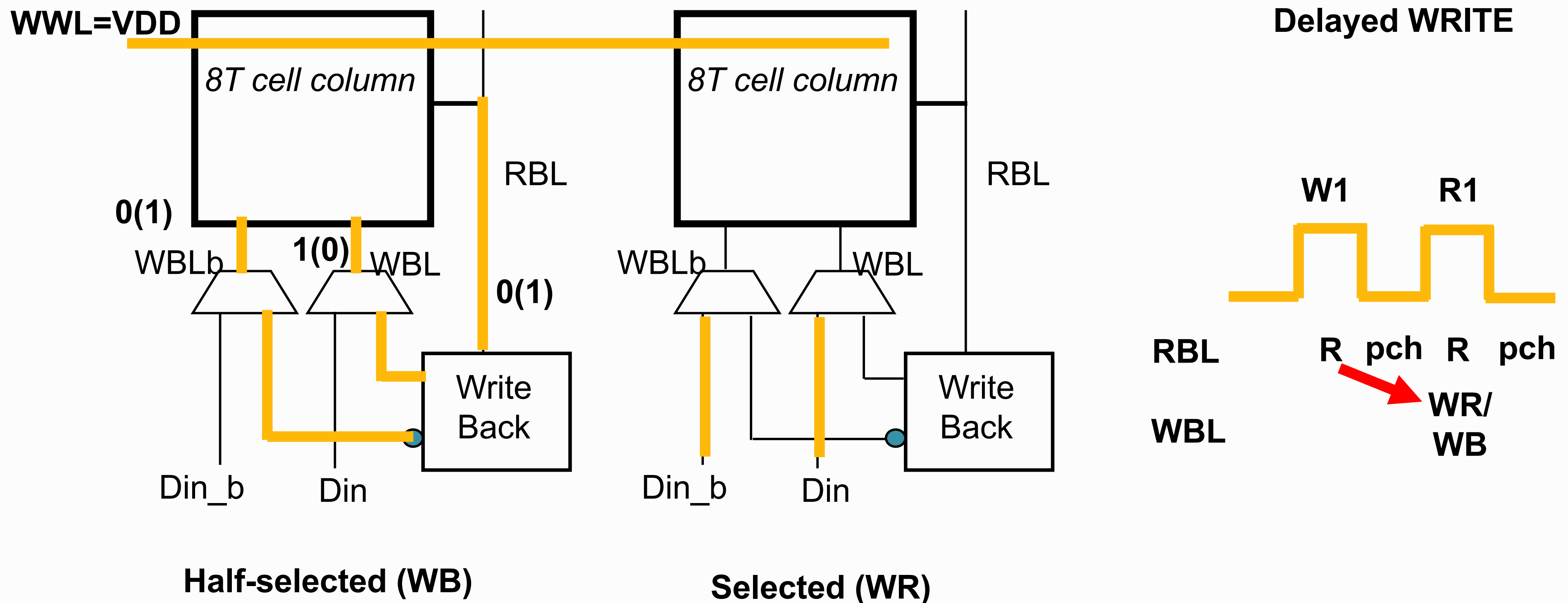
- During a Read or Write operation, half-selected cells on the selected word-line are actually experiencing "Read" operation
  - Disturb similar to Read-disturb



Half-Select in 8T

- Array architecture approach
  - No column select. Floorplan such that all bits in a word are spatial adjacent
- Gated Write wordline signal (Byte Write)
  - Local Write wordline “on” only for the selected block
- Write-back scheme
  - RWL activated even during Write, all cell data in selected WL read out to D-latches
  - Dataout is then written back to half-selected cells

Delayed Read-Modify-Write



- Allow the column-select in 8T cell array by replacing “WRITE” with “READ-MODIFY-WRITE”
- One cycle delayed WRITE: Relaxed timing, No bandwidth loss

Question

❑ Which of the following is true wrt decoupled Read-Write 8T SRAM Cell

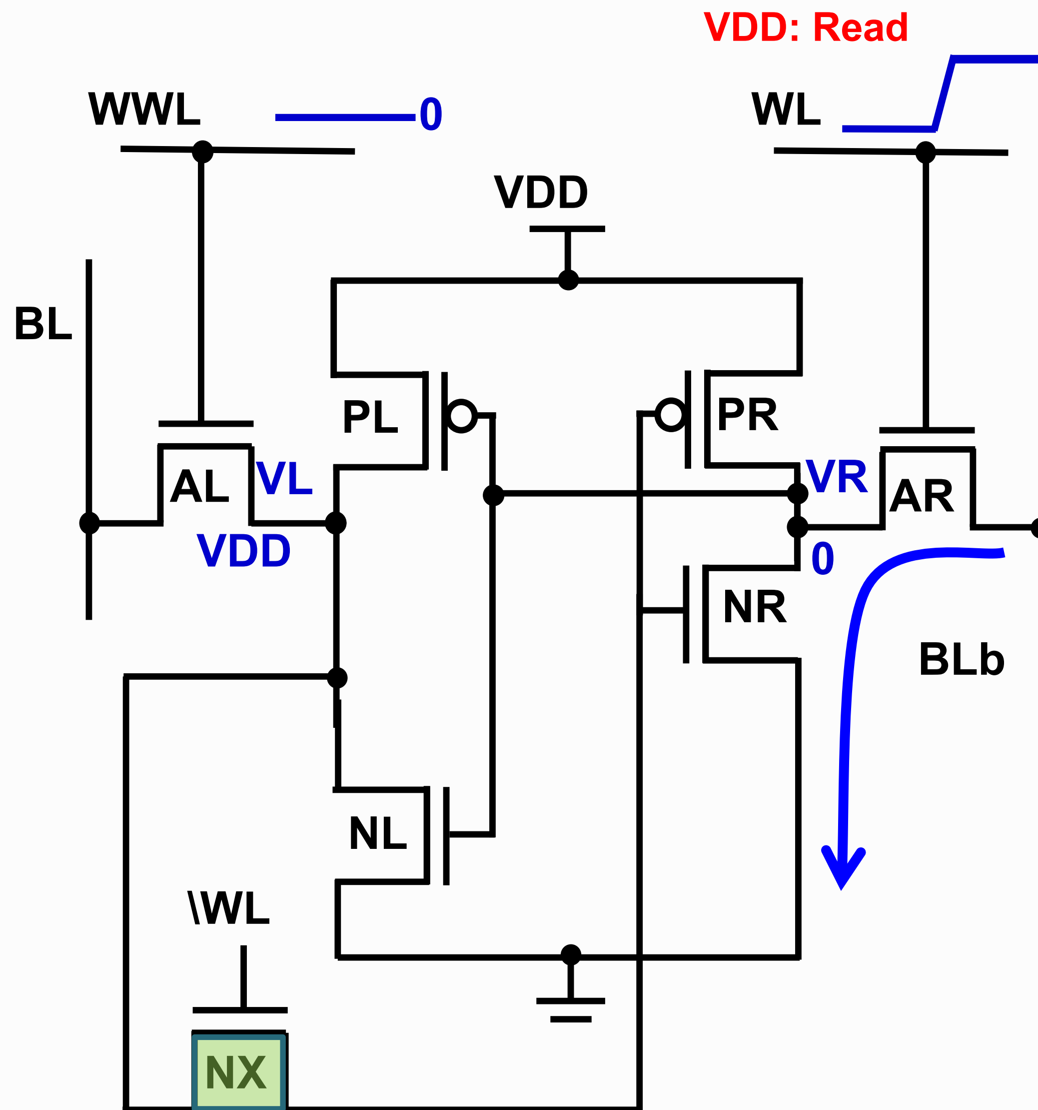
a) The RBL needs to be on the side of the BL-bar

b) It is possible to be read and write to the different cell in the same column

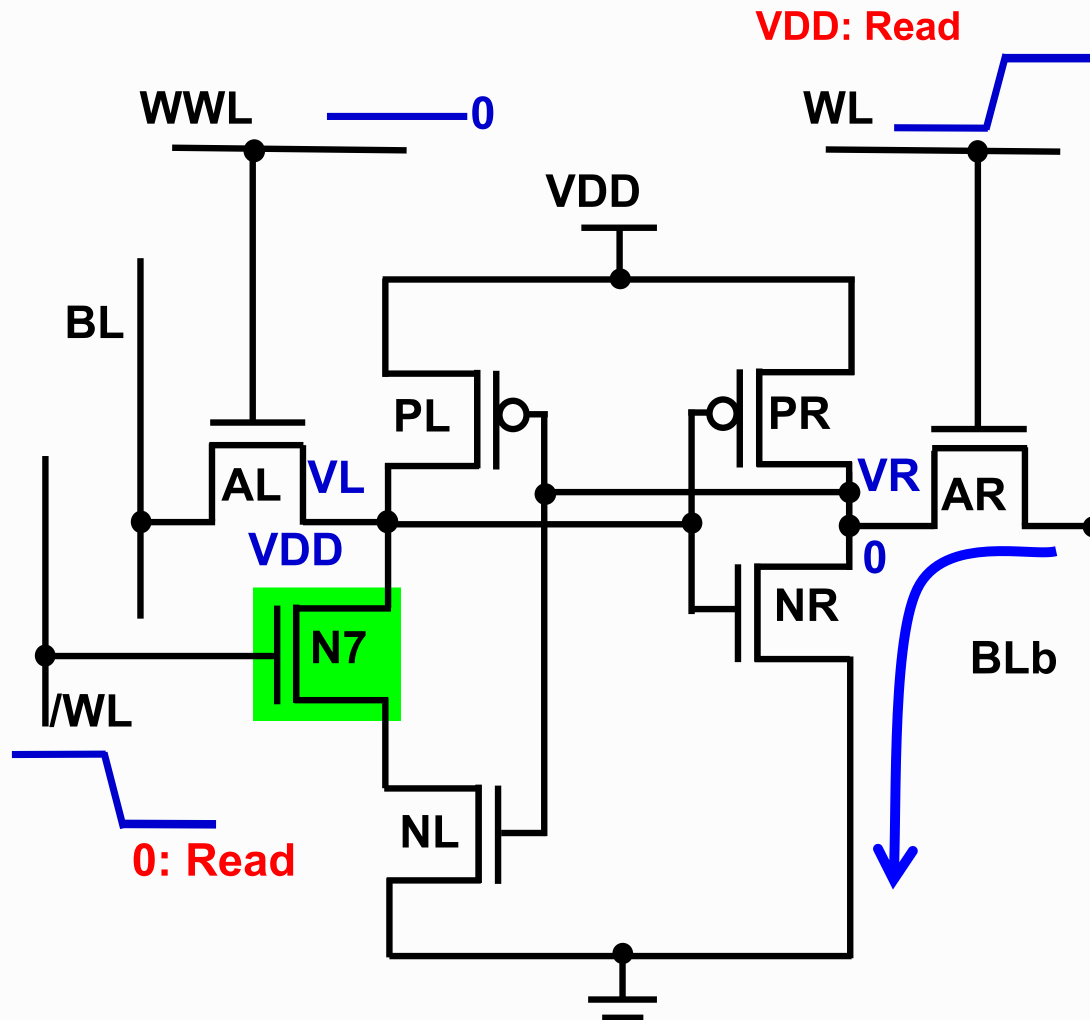
c) The 6-T portion of the SRAM cell is optimized for ‘hold’ operation

d) Memory folding cannot be done with 8-T cells

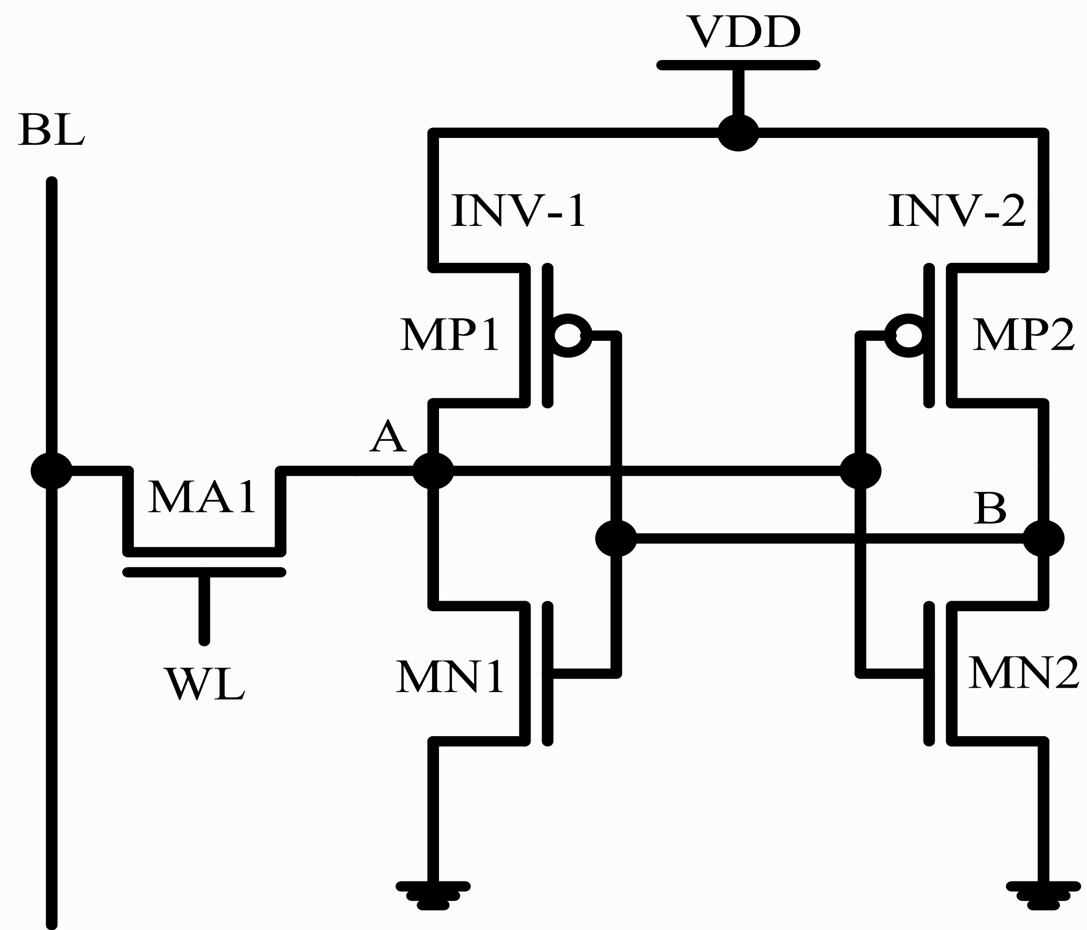
Conditionally decoupling regeneration



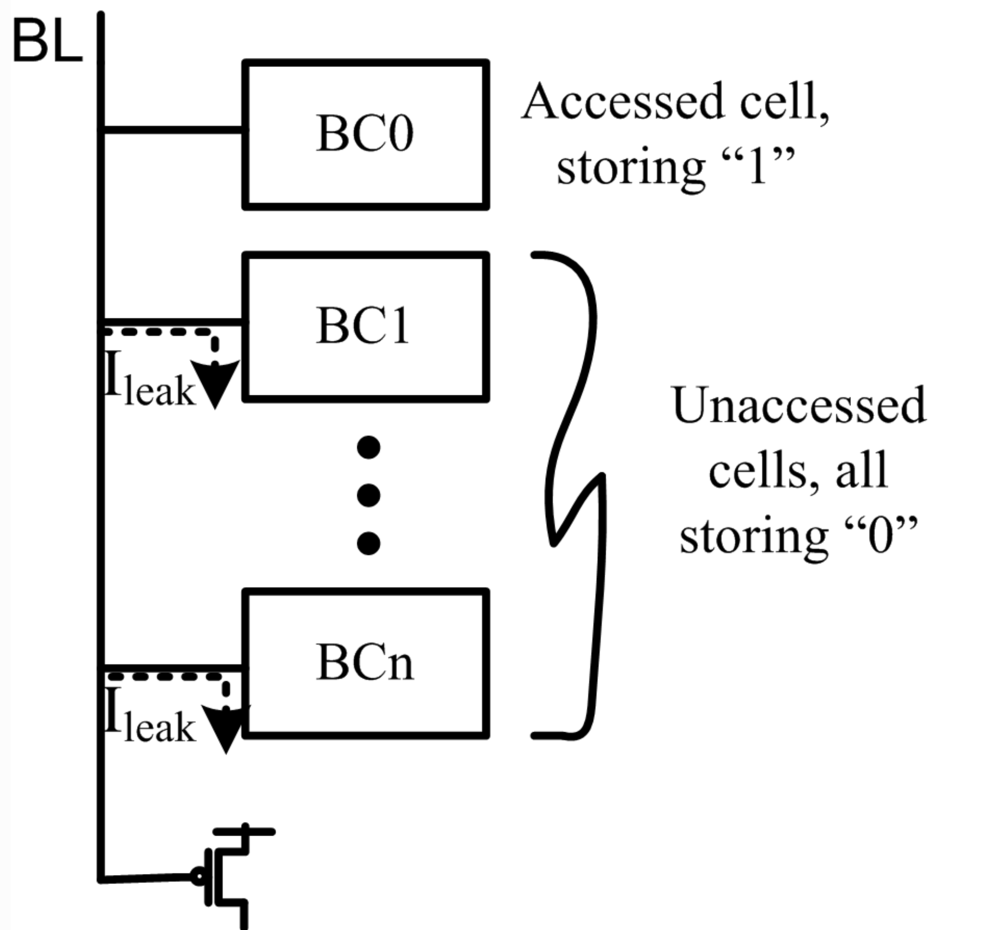
Conditionally decoupling regeneration



5T SRAM



Worst case read condition



: Worst case Bitline Leakage when reading a "1"

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