High-Performance Design

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Content & Learning Objectives

❑ SRAMs

- Memory hierarchy and organization, SRAM building blocks and peripherals, modes of operation, common and uncommonly used cell types with their merits / demerits, Assists circuitry
- Introduction to next generation memory (circuits)

❑ Reliability and Variation

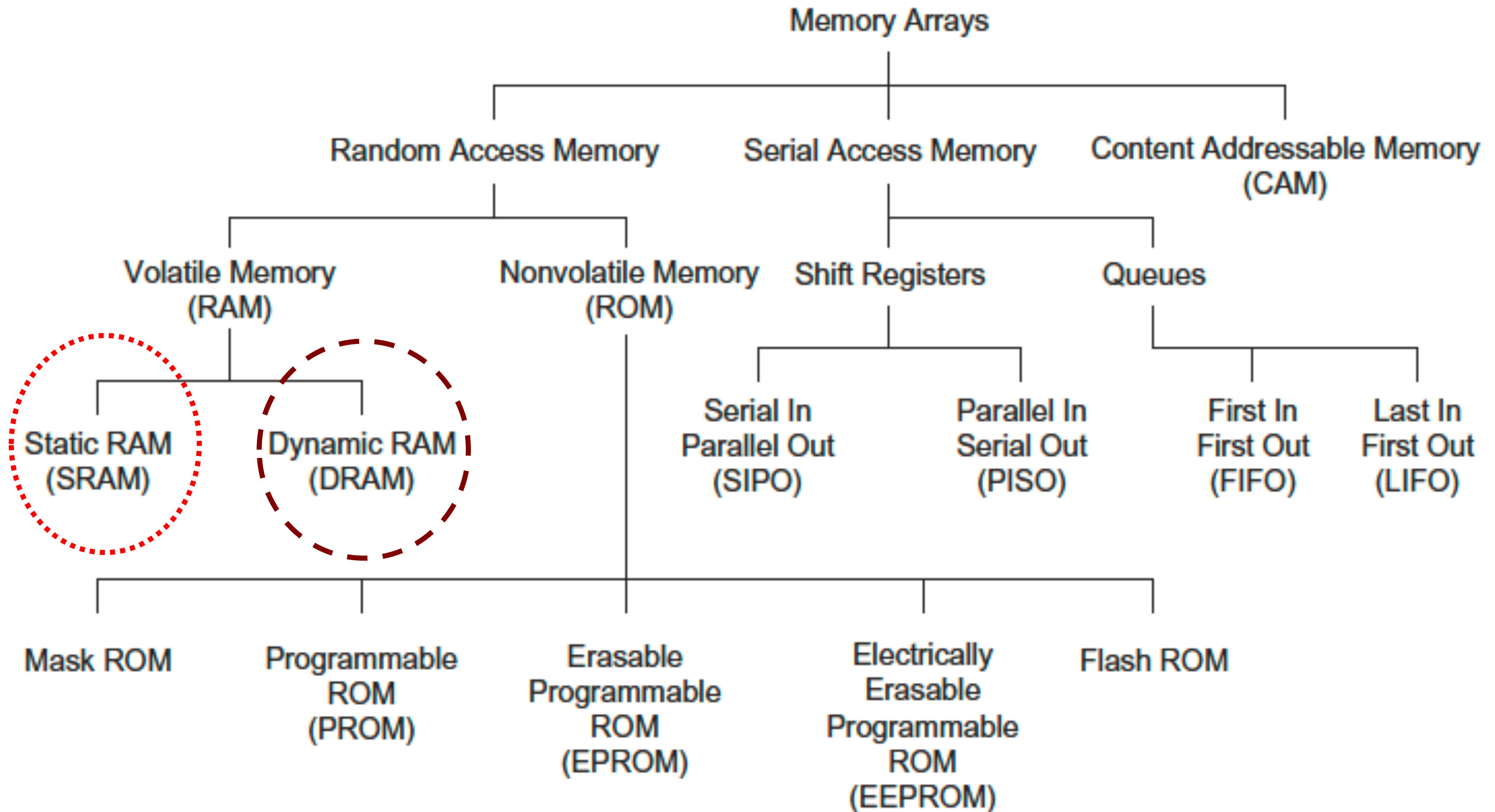
- Source of variation, Variation detection circuits, impact on SRAMs
- Bias Temperature Instability
- Variation tolerant circuits / methods

❑ Other topics?

References

- CMOS VLSI Design: Circuits and Systems Perspective
  - Chapter 12 'Array Subsystem'
  - Authors: Neil Weste and David Harris
- Design of High performance Microprocessor Circuits
  - Part V: Memory System Design
  - Authors: A Chandrakasan, W Bowhill, F Fox
- Conference / Journal papers (as we go)

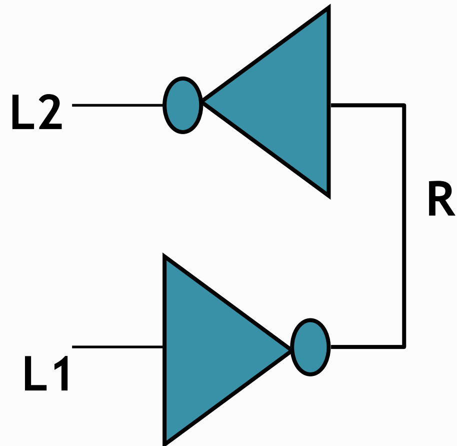
Memory Classification revisited

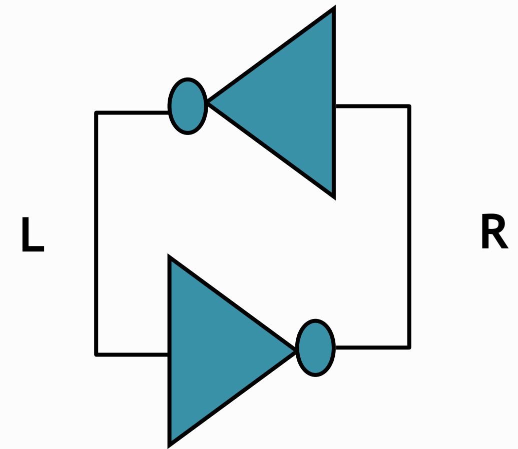


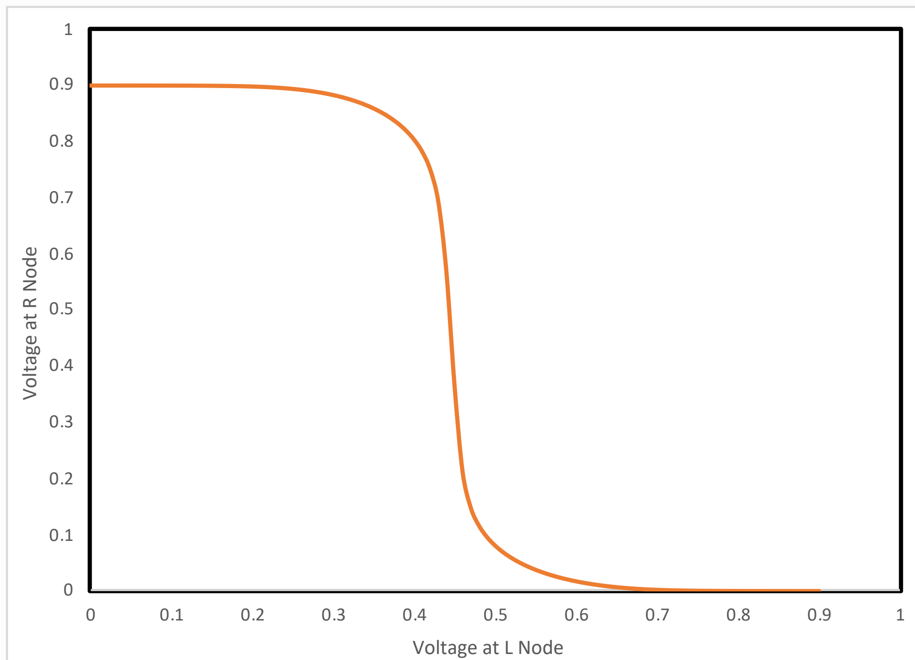
Topics

- SRAM : Basic memory element
- Operations and modes of failure
- Cell optimization
- SRAM peripherals
- Memory architecture and folding

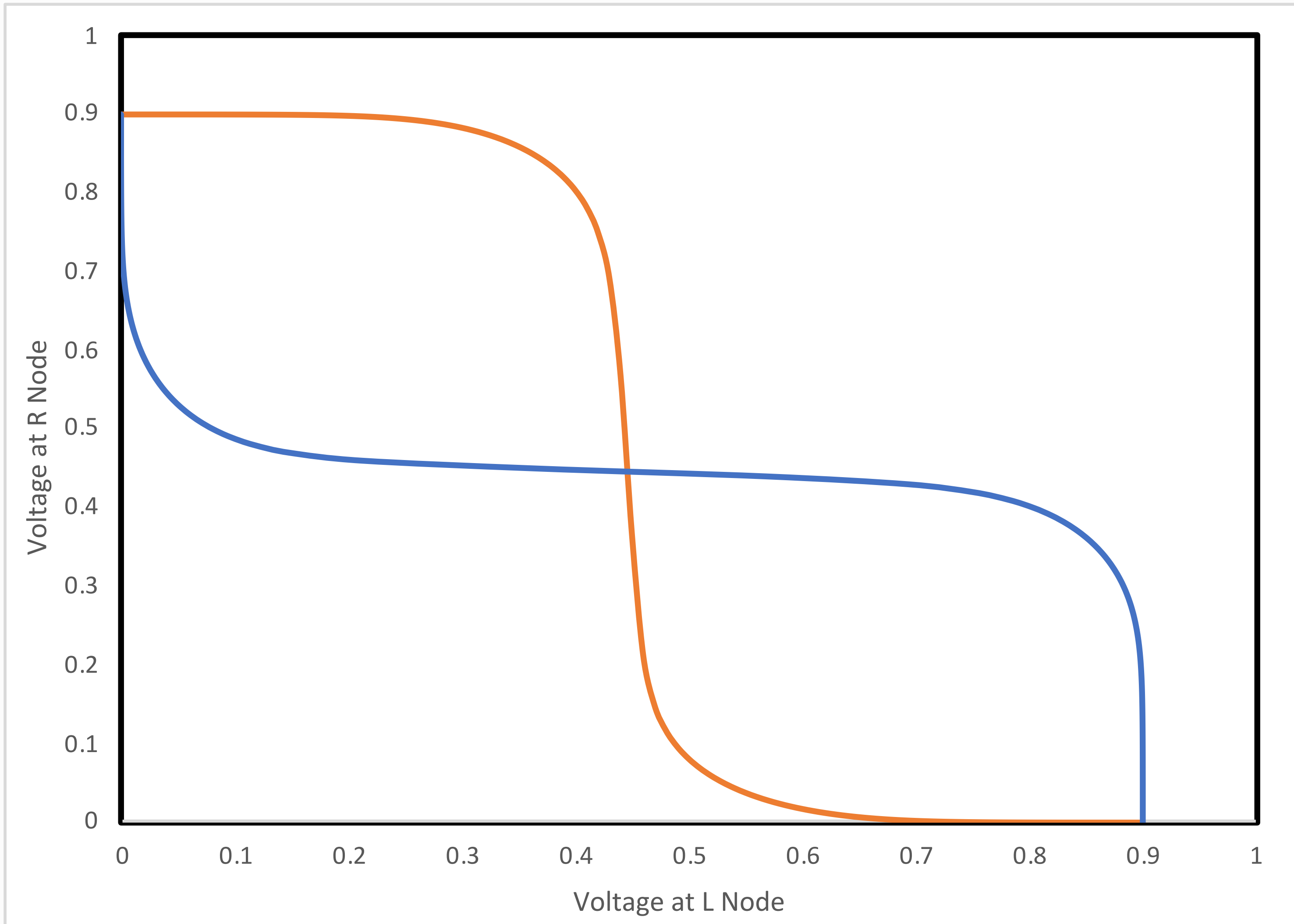
Back to Back Inverters



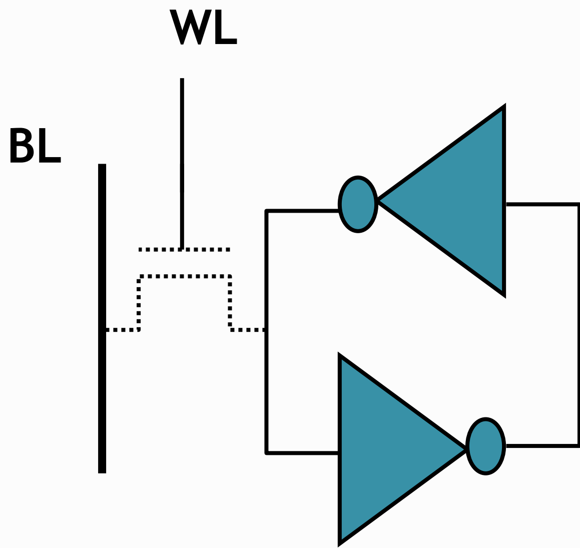




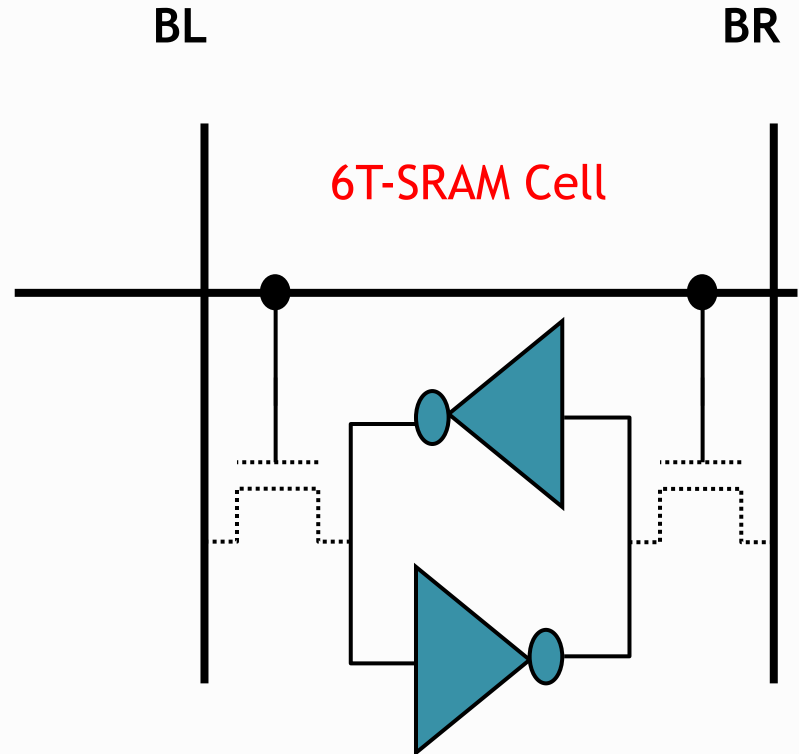
Butterfly Curve



SRAM Cell

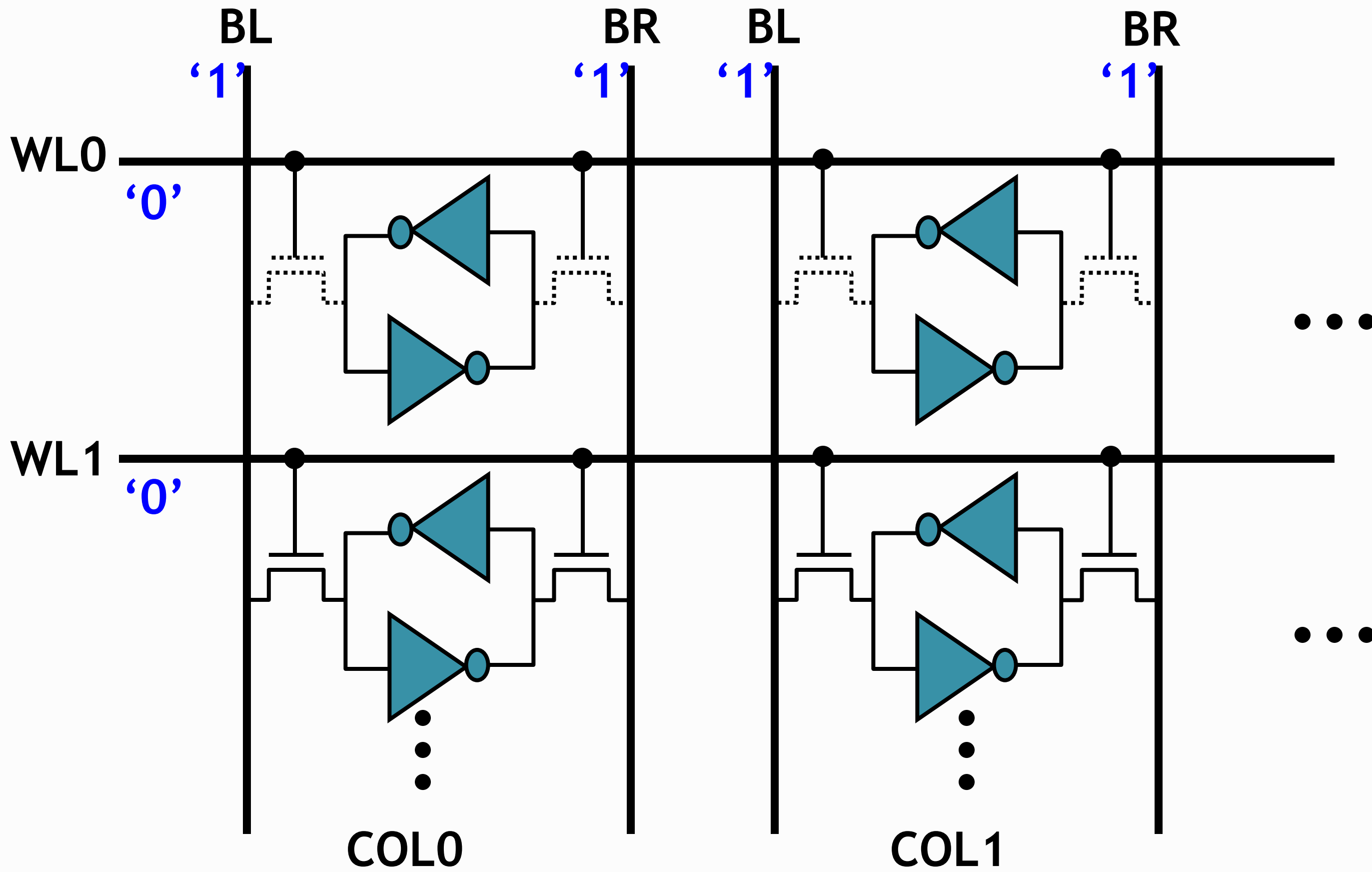


5T-SRAM Cell

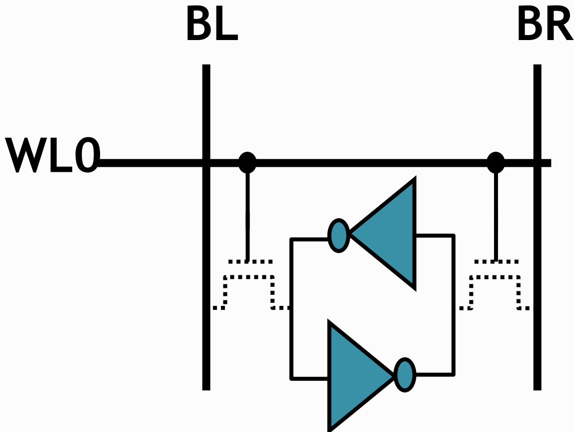


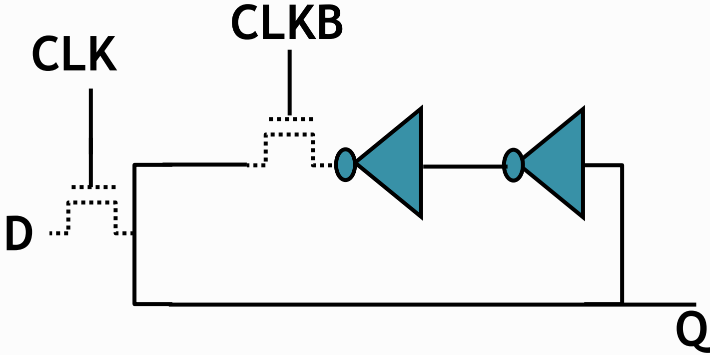
6T-SRAM Cell

No Operation (Hold)

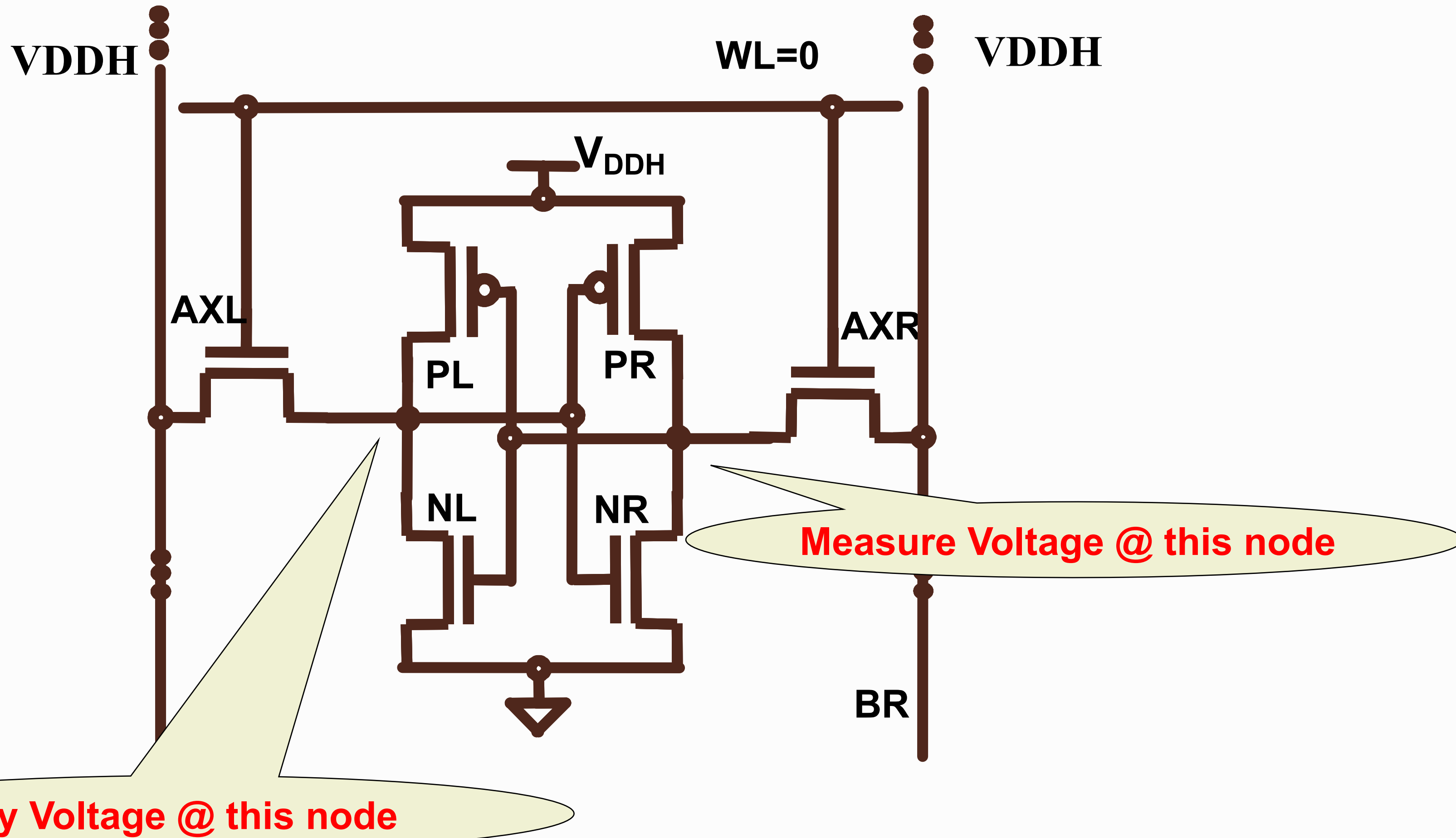


Differences between latch and memory cell?





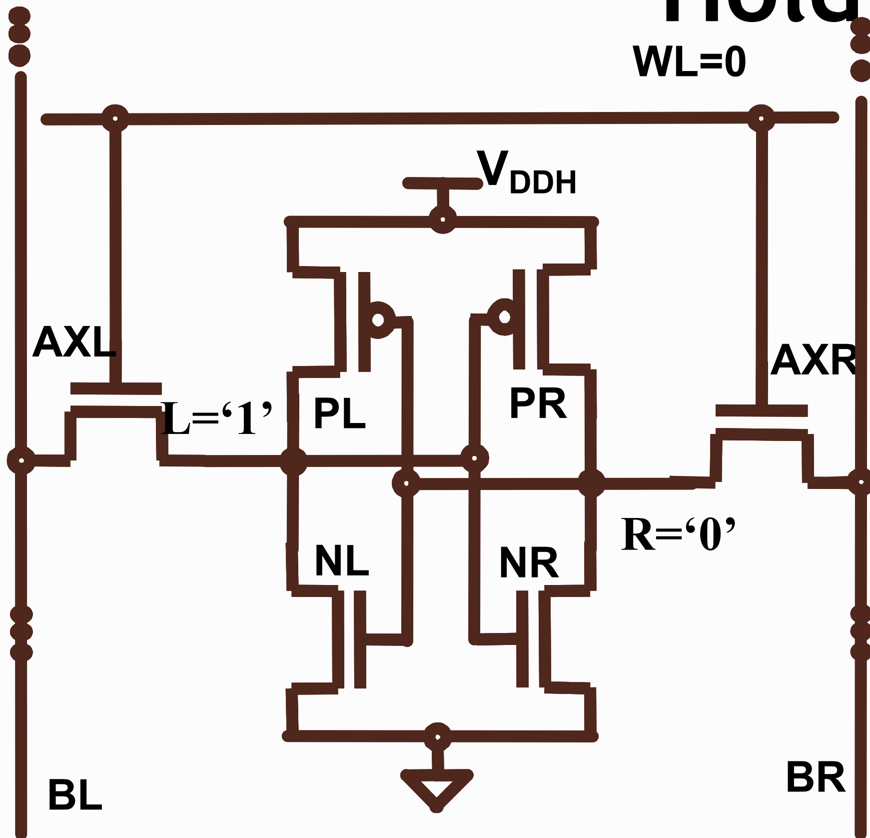
Margin Measurement

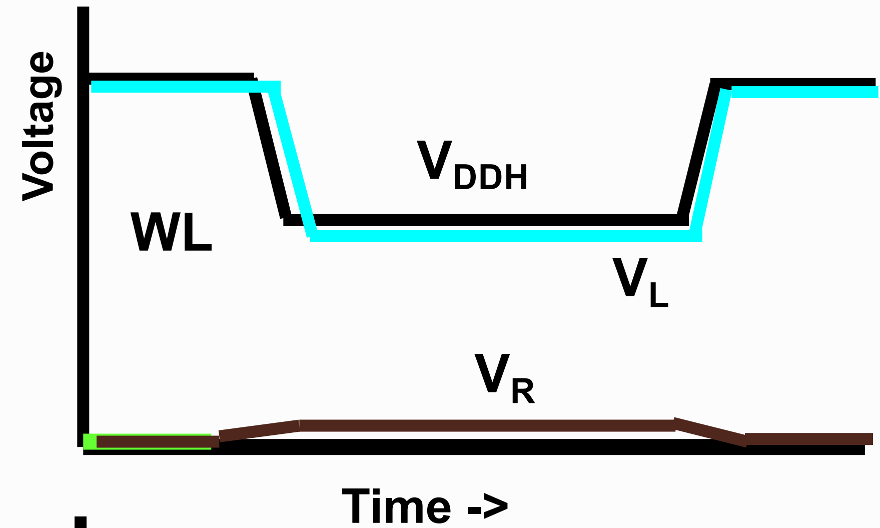


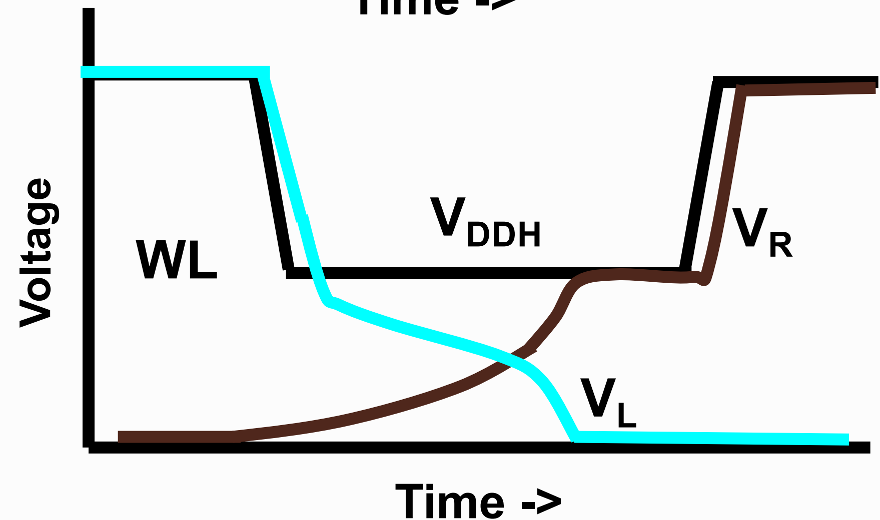
Then flip the application and measurement sides (use half cells).

Plot the Transfer curves on the same graph

Hold Failure





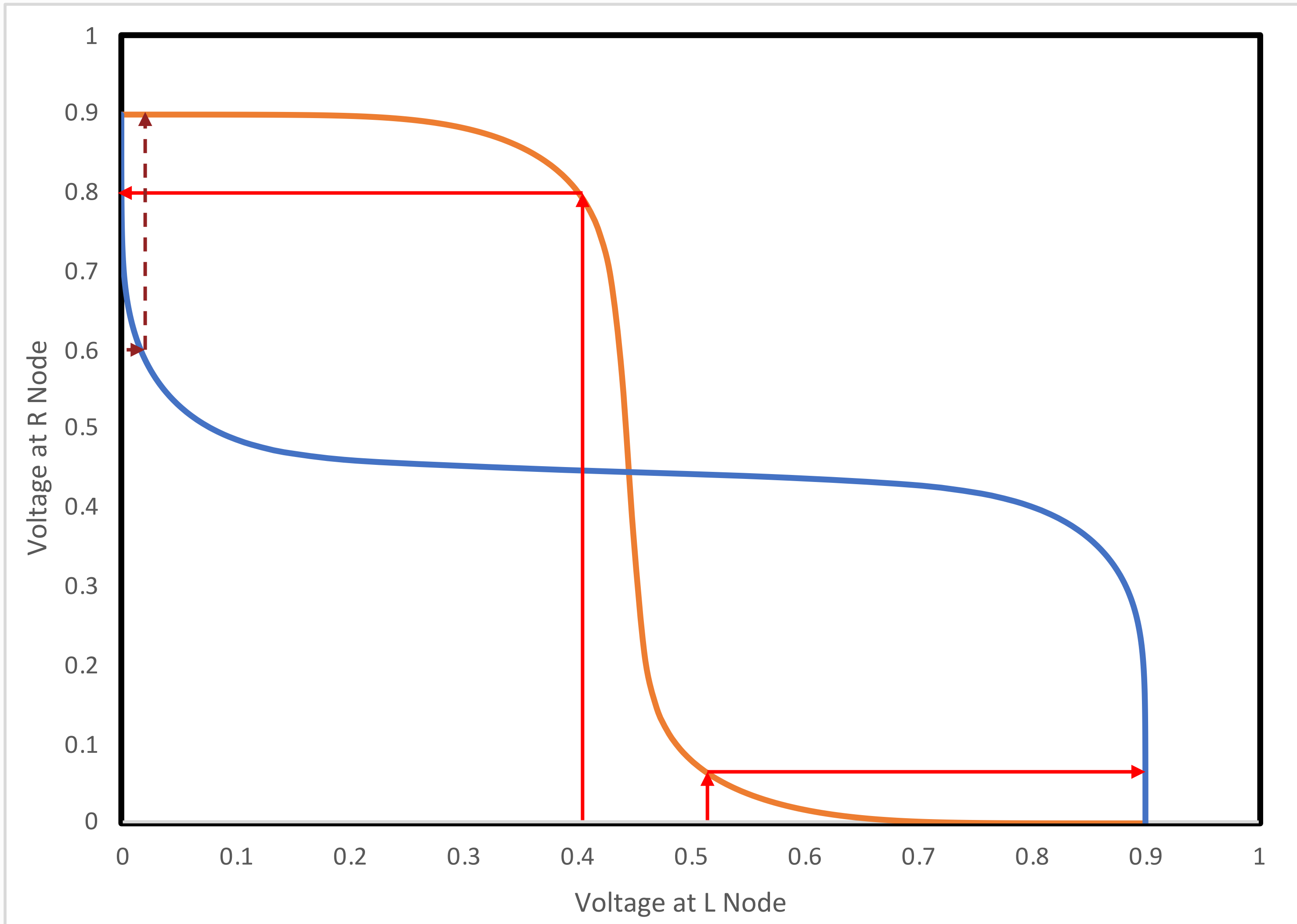


$$P_{HF} = P\left(V_{DDHmin} > V_{HOLD}\right)$$

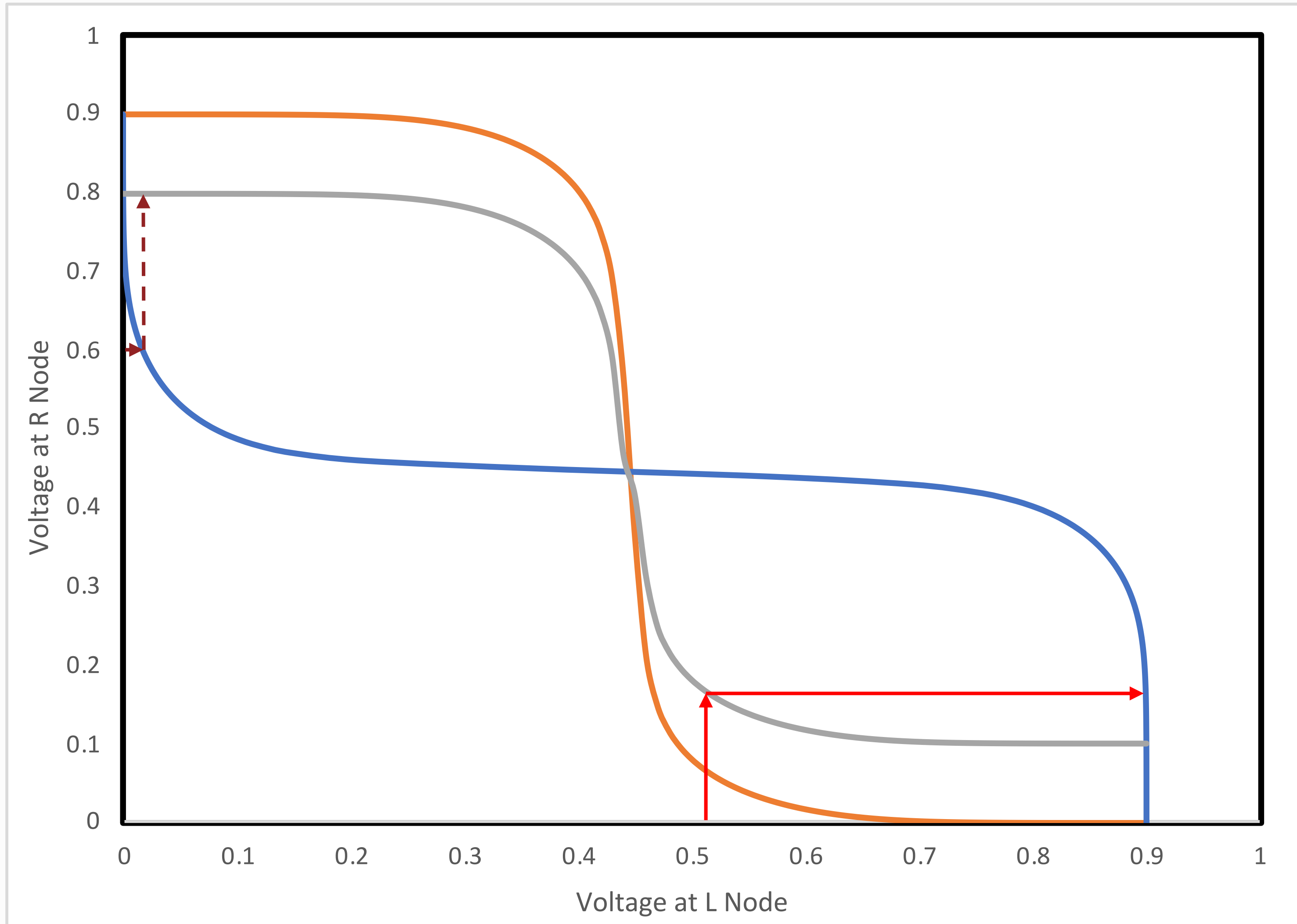
Hold Failure => Flipping of cell data in the Hold mode with the application of a lower supply voltage.

S. Mukhopadhyay, ITC 2010

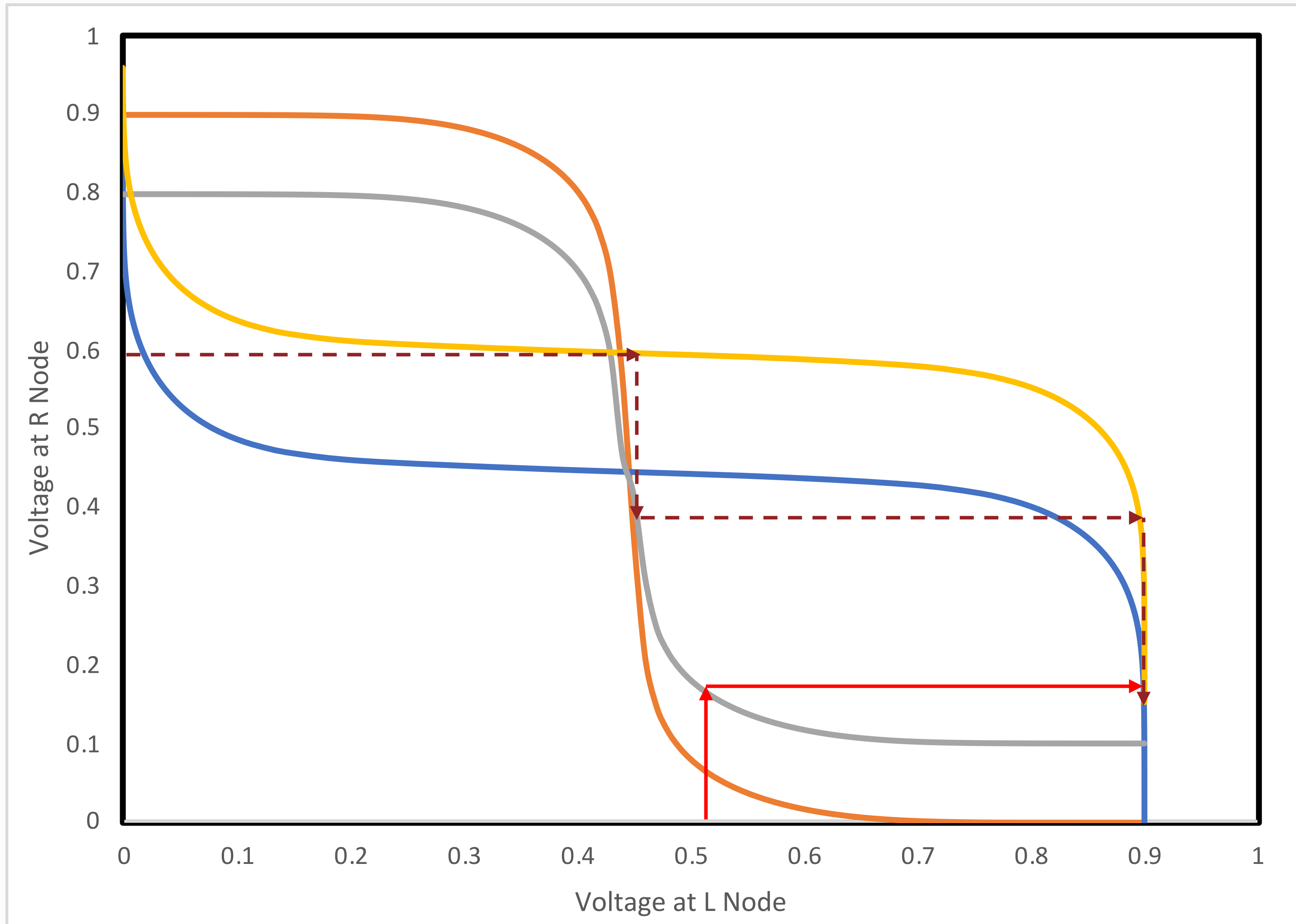
Hold Margin



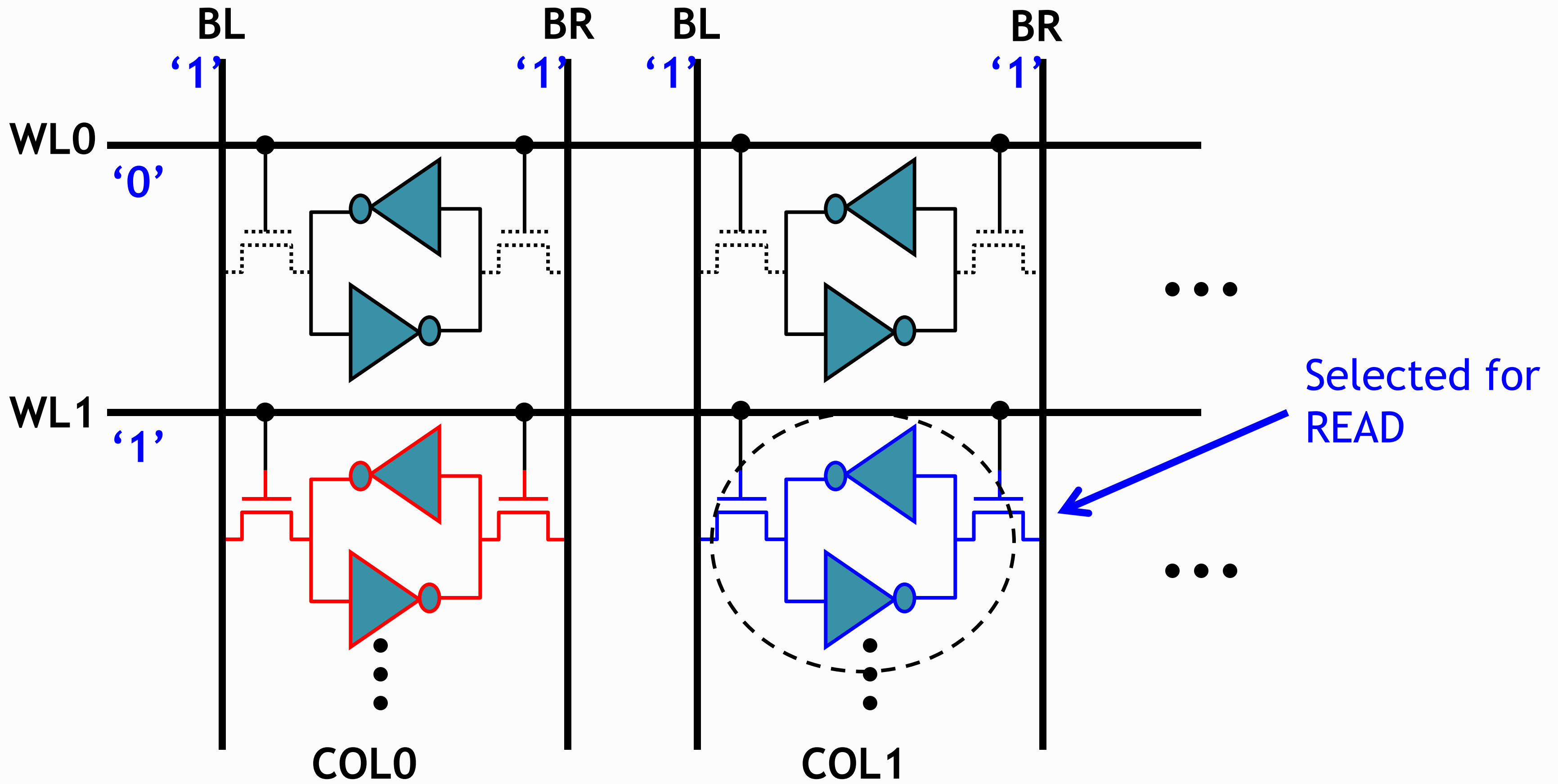
Hold Margin



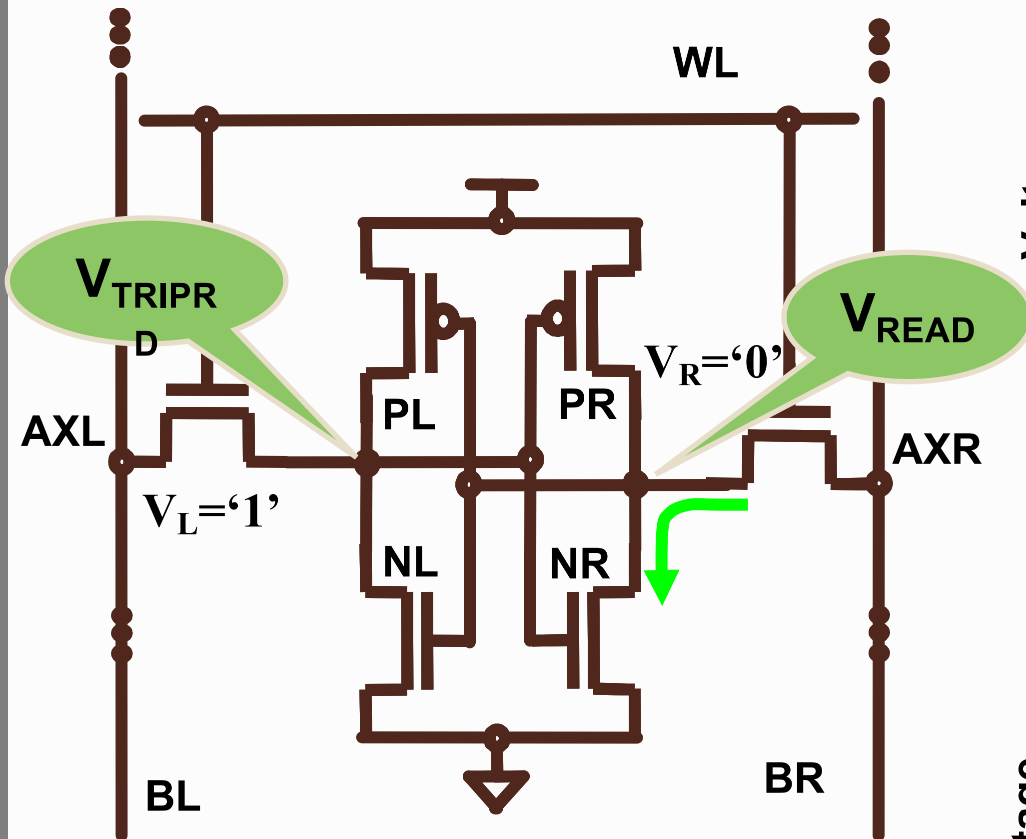
Hold Margin

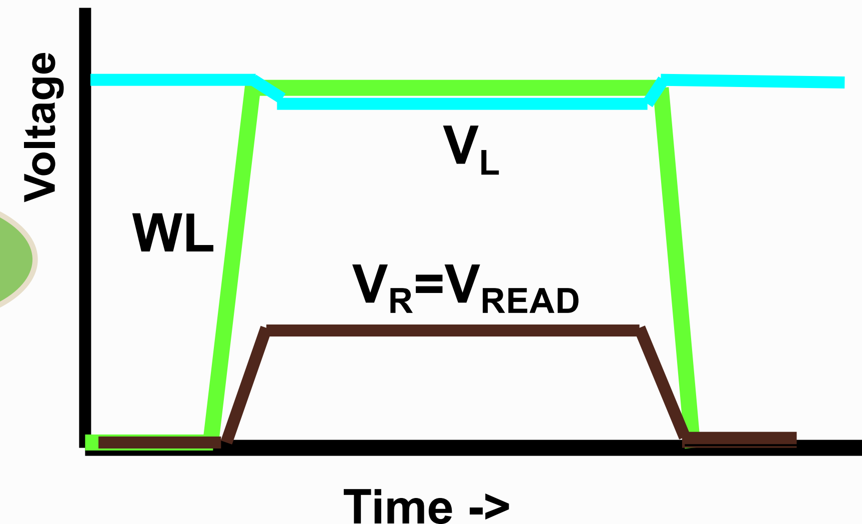


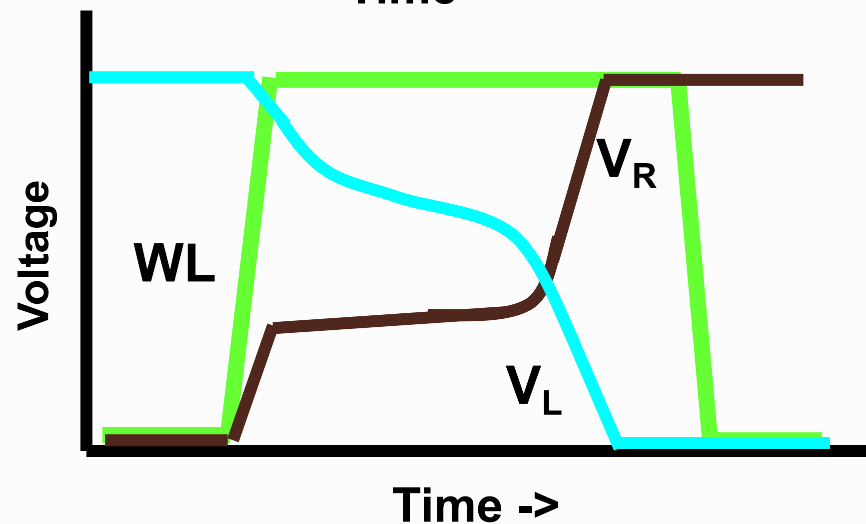
Read Operation



Flip During Read: Read Failure







$$P_{RF} = P(V_{READ} > V_{TRIPRD})$$

Read failure => Flipping of Cell Data while Reading

Question 1

- Hold Margin for an SRAM cell

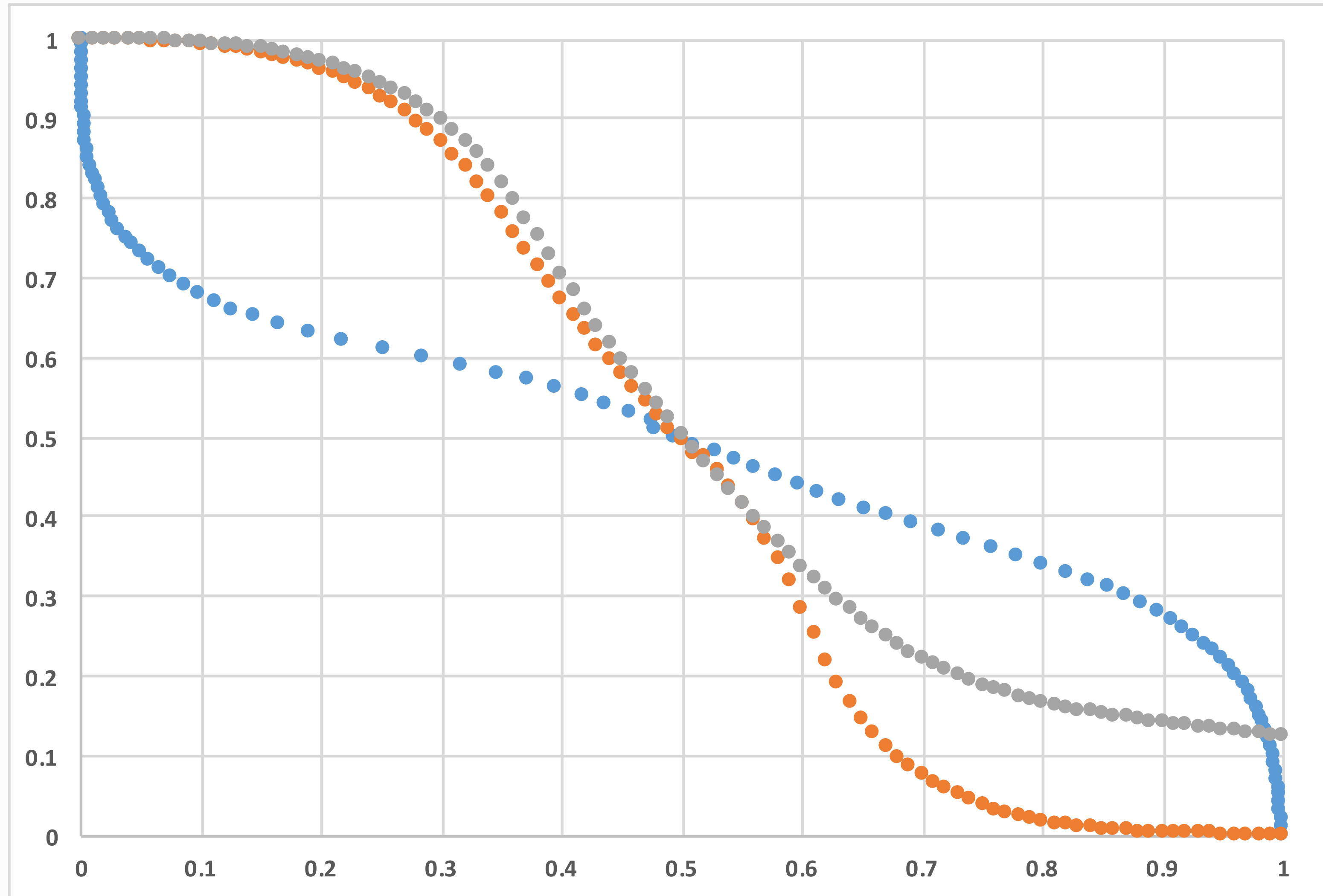
a) Is always greater than read margin

b) Can be improved by making the access transistor bigger

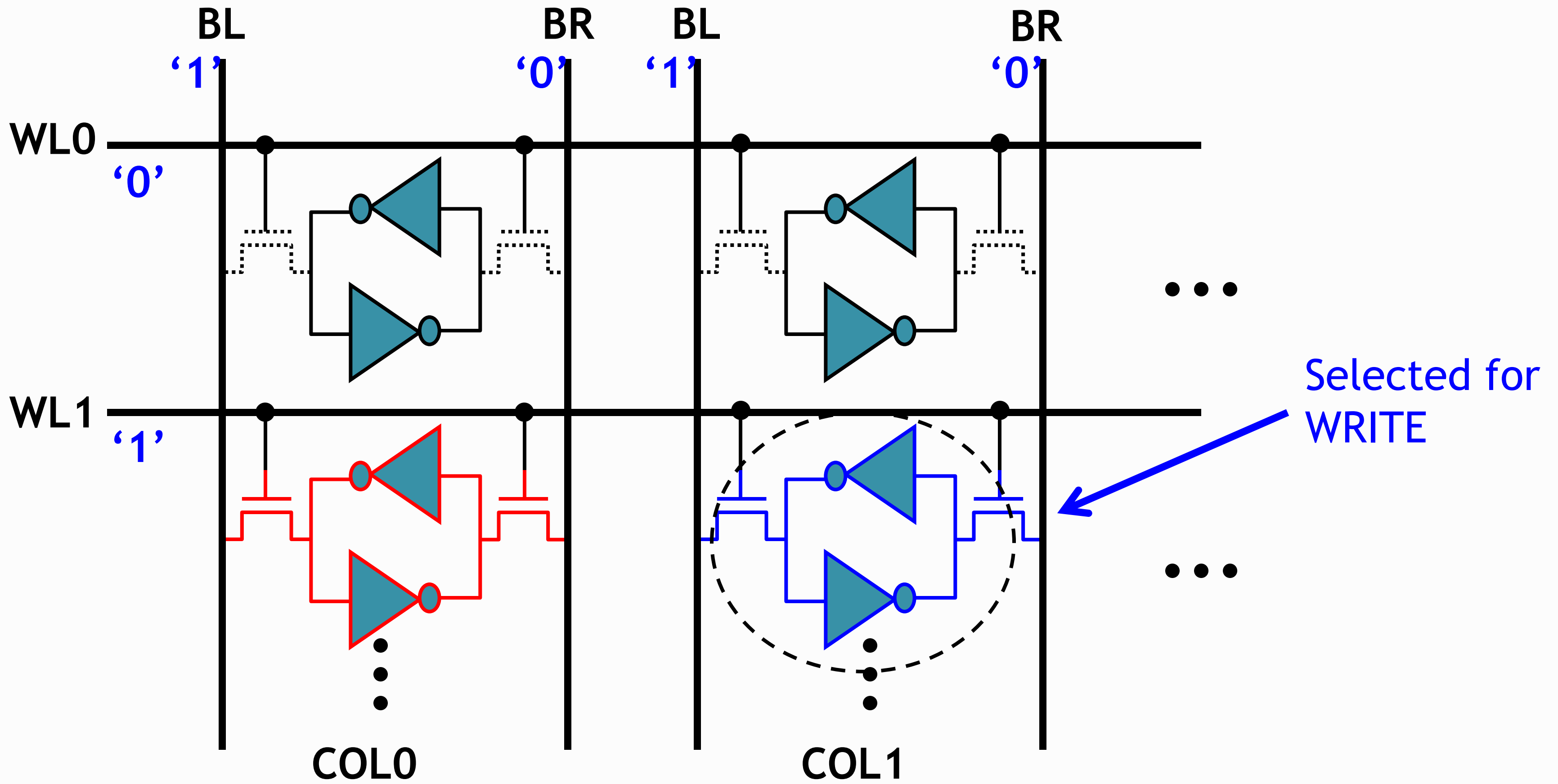
c) Defines the minimum supply voltage required to perform a read operation

d) Depends on the number of cells on the bit line

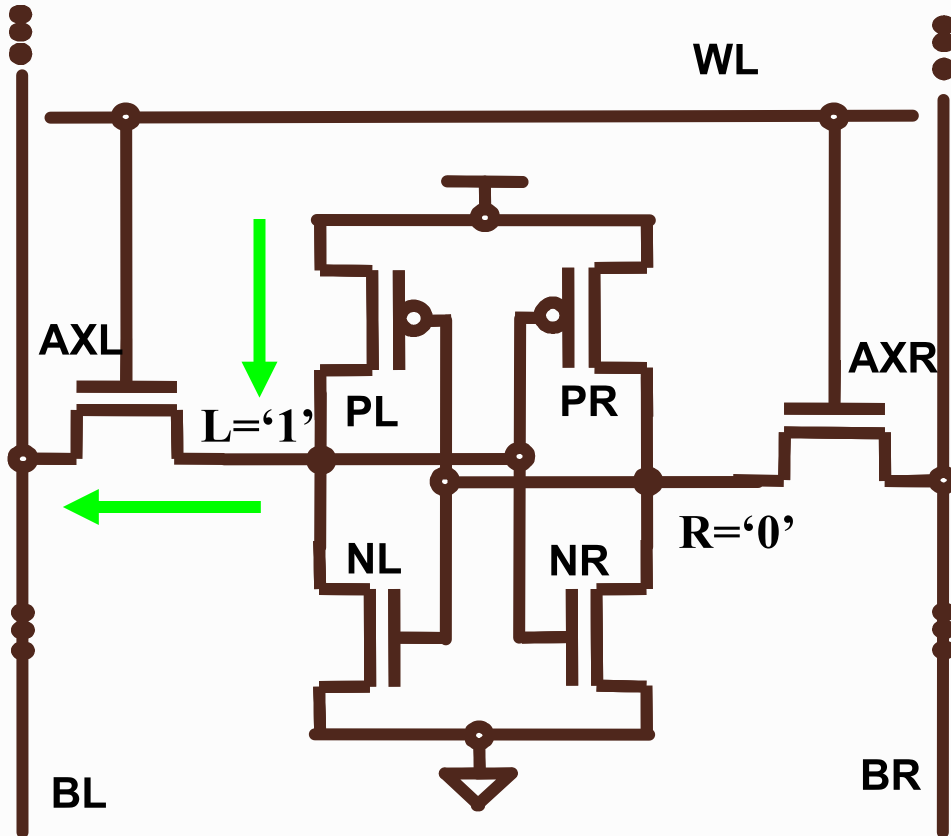
Hold vs Read Margin

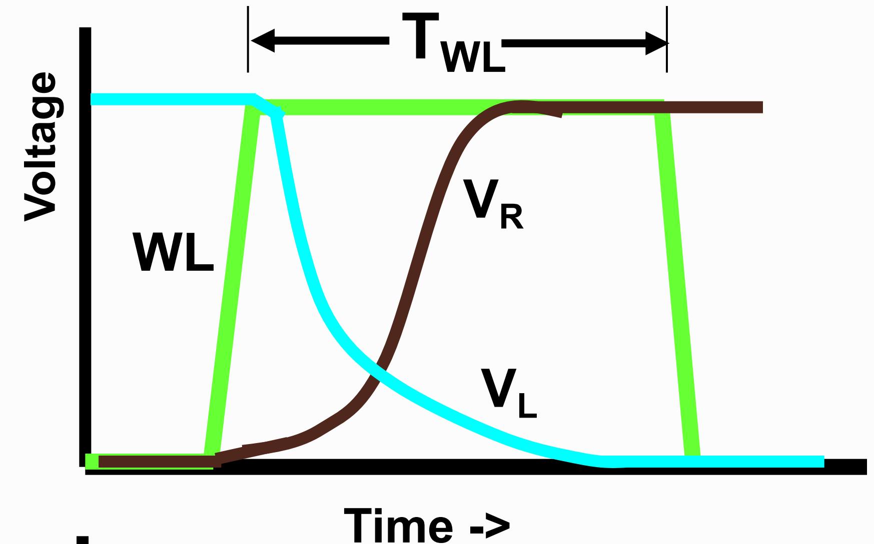


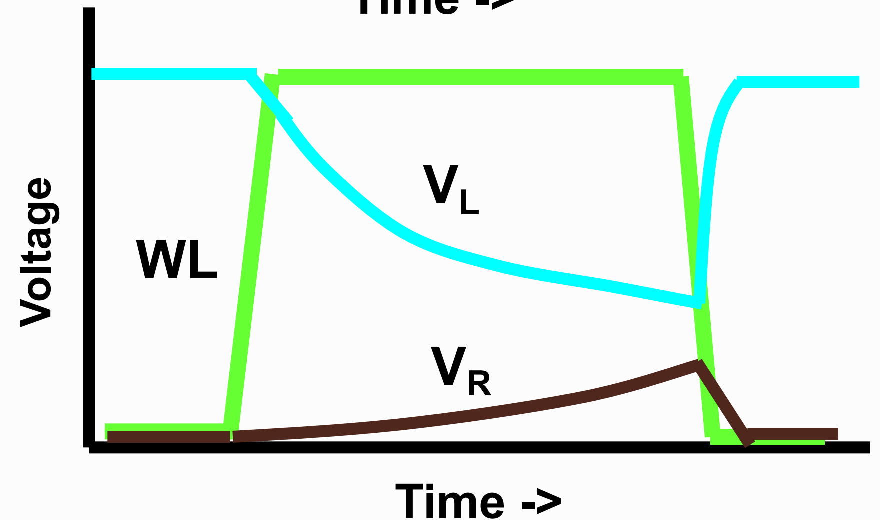
Write Operation



Write Failure



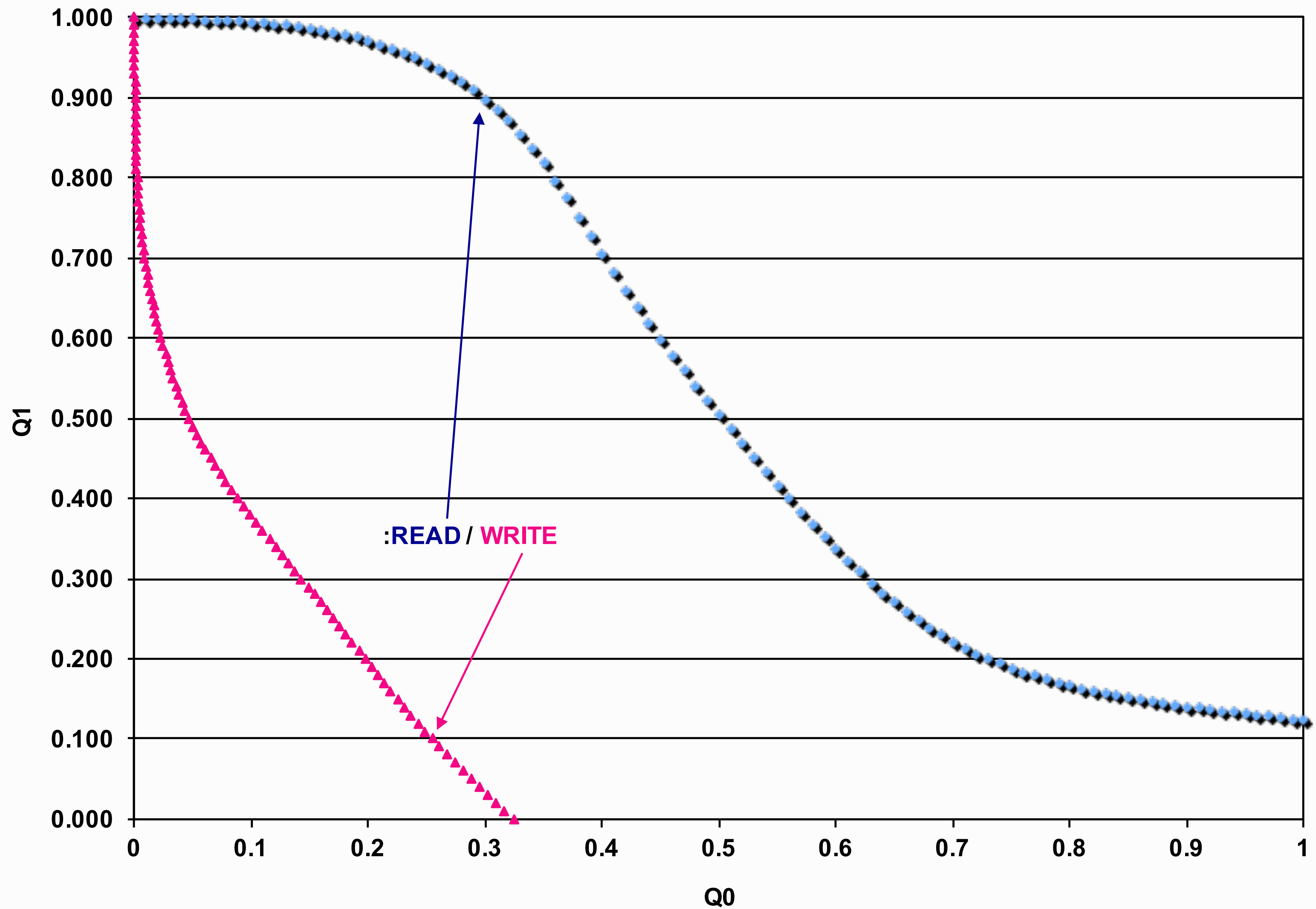




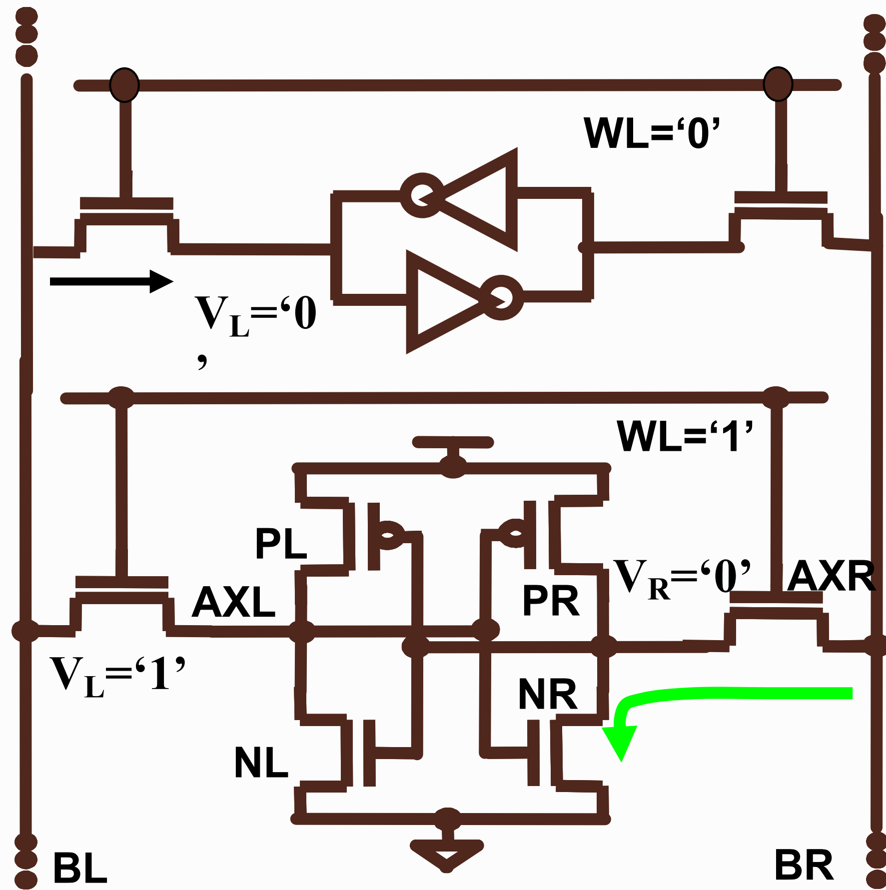
$$P_{WF} = P\left(T_{WRITE} > T_{WL}\right)$$

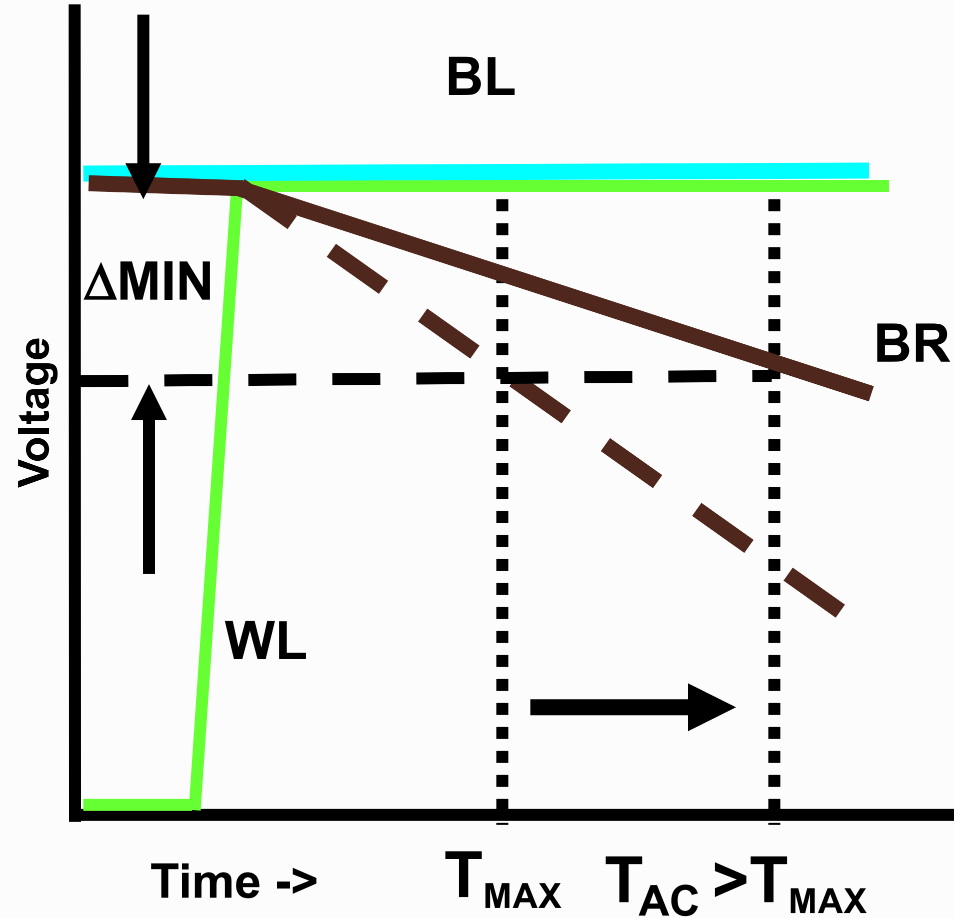
Write Failure => Unsuccessful write to the cell.

Write Margin



Access Failure





$$P_{AF} = P(T_{ACCESS} > T_{MAX})$$

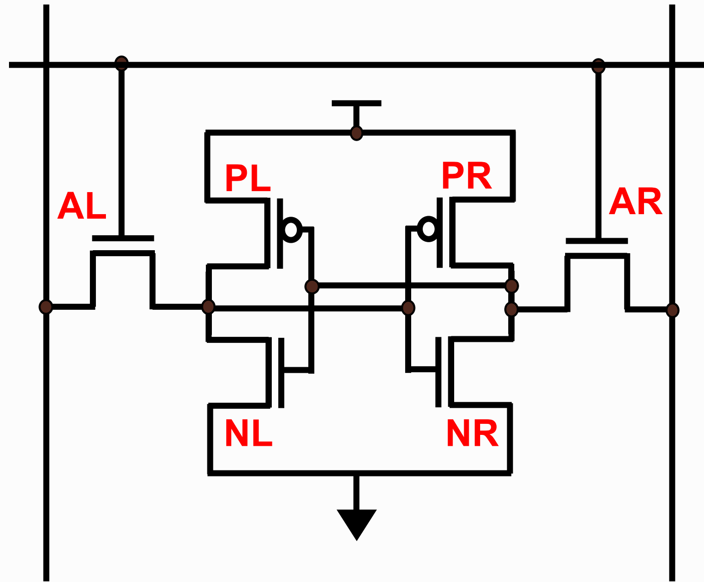
Access Failure : Time required to produce a pre-specified bit-differential is higher than a maximum allowed time.

Question 2

- Write Margin for an SRAM cell

a) Is always greater than read margin
b) Can be improved by making the access transistor bigger
c) Defines the minimum supply voltage required to perform a read operation
d) Depends on the number of cells on the bit line

The Balancing Act



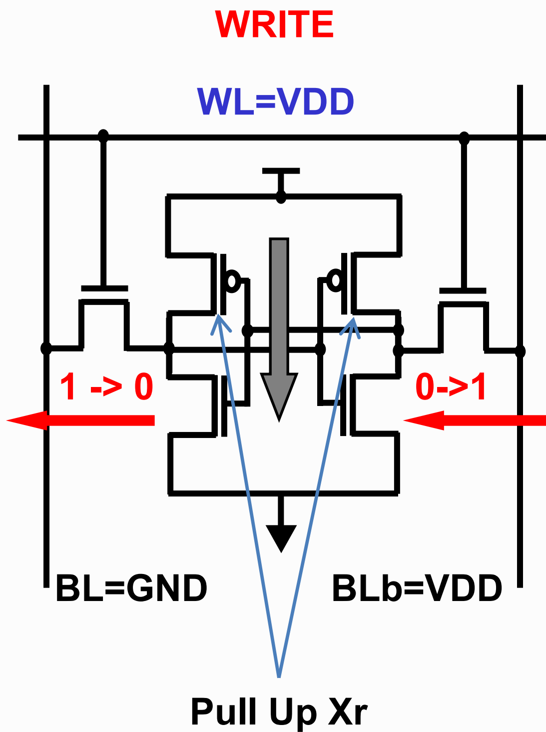
Large N: Better READ performance. If too large, trip voltage of inverter becomes so low that cell becomes unstable.

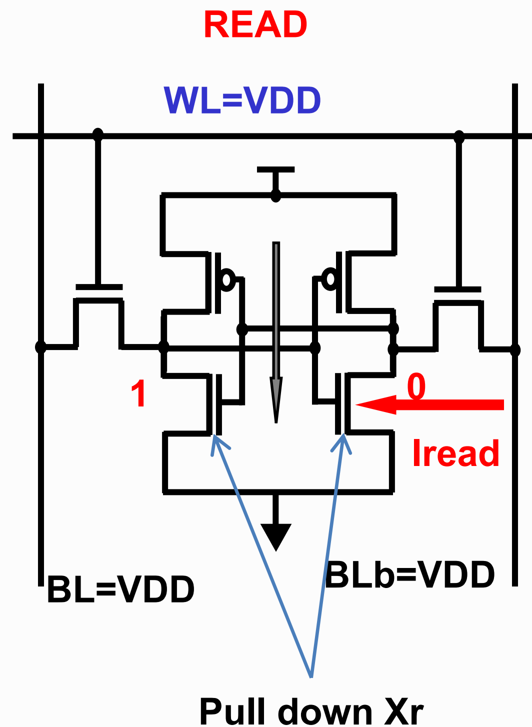
Large A: Better Performance. If too large, storage node voltage goes high during READ, causing cell flip

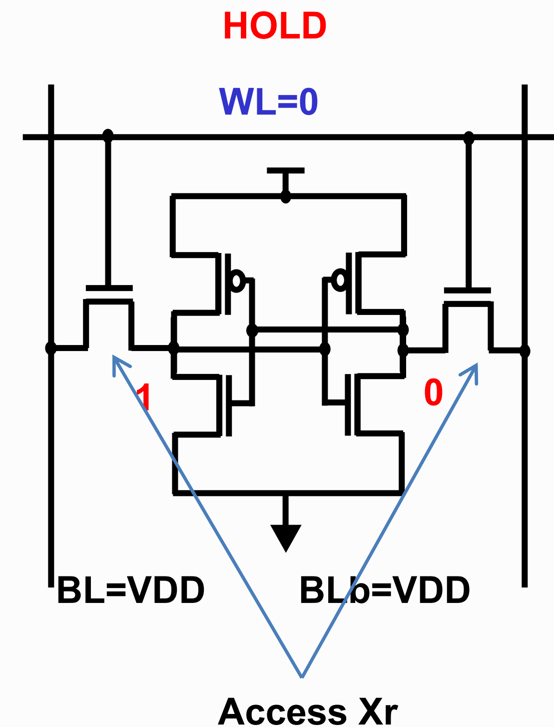
Large P: Increase stability. If too large, hard to WRITE.

Need to balance all : NR:XR:PR ~ 2:1:1

Workhorse 6T-Cell







Access Xr: On
Data driven on bit - lines
Data Flipped by over-coming pull-up / pull – down Xrs

Acess Xr: On
BL, Blb pre-conditioned, and then floated, one line discharges thru the cell (Iread), voltage sensed, Data Retained

Access Xr : Off
Data Retained, due to back-to-back inverters

Thin Cell (Litho-Friendly)

Cell area vital for density

Metal to diffusion contact

Poly-silicon (gate)

Metal or diffusion to poly contact

Metal to Metal via

word

N R

N L

P L

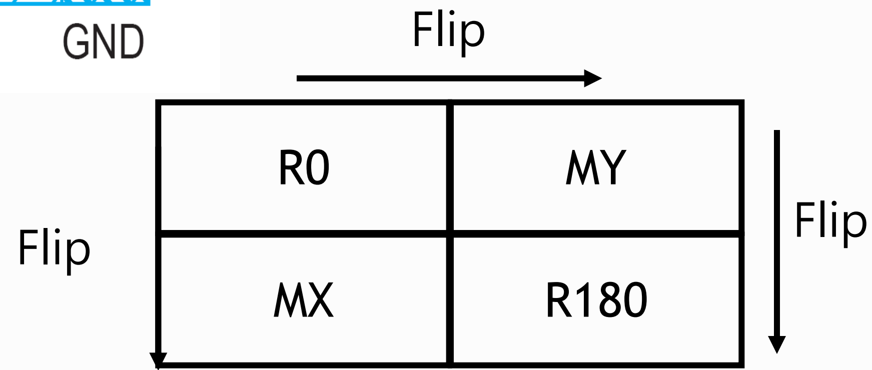
GND

bit

V_{DD}

bit_b

GND



Question 2c

- Decreasing the size of only one side of NFET transistors will improve the cell

a) Cell density

b) Read margin

c) Write margin

d) Hold margin

Topics

- Introduction to memory
- SRAM : Basic memory element
- Operations and modes of failure
- Cell optimization
- SRAM peripherals
- Memory architecture and folding

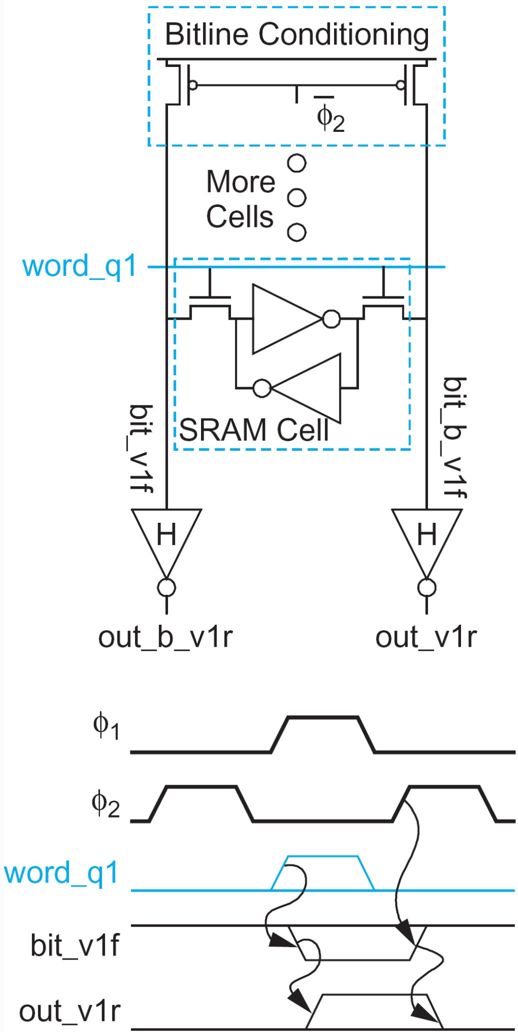
Decoders and Drivers

WL driver	cell	cell	cell	cell
WL driver	cell	cell	cell	cell

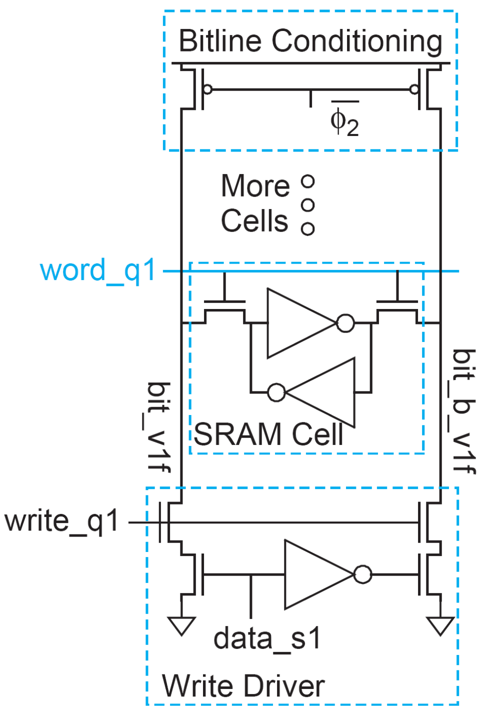
Word line driver layout needs to be pitch matched to SRAM cell

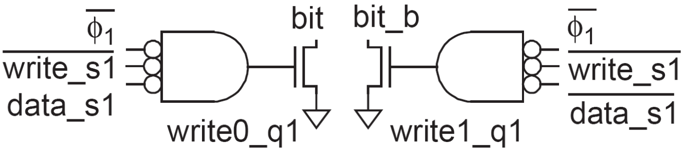
WL driver	cell	cell	cell	cell
WL driver	cell	cell	cell	cell
Decoder and Control	Column Circuitry			

Column Circuitry for Read and Write



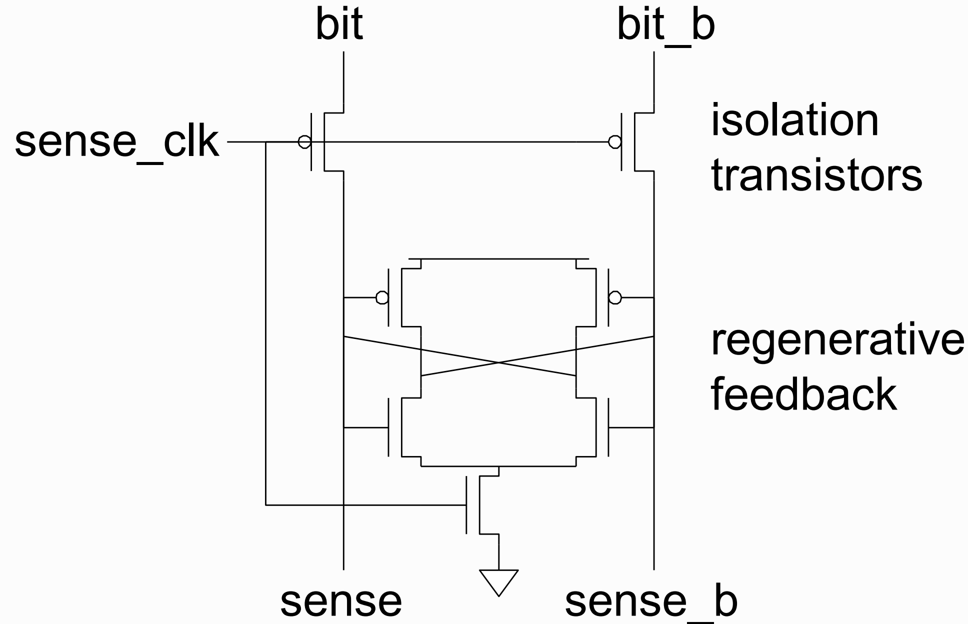
READ





WRITE

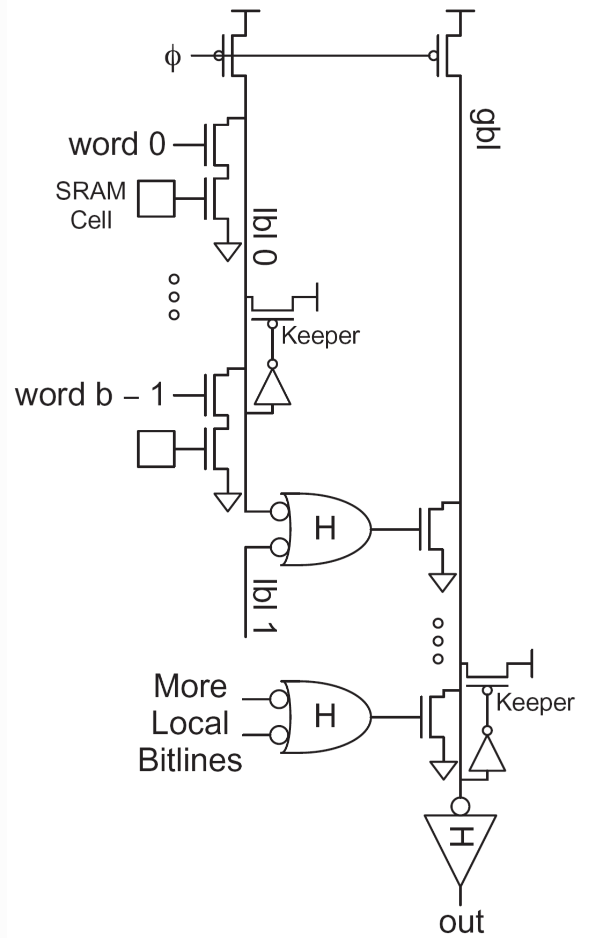
Sense Amplifiers



Sense-amp provide necessary gain (small input → large output) for read
If sense_clk arrives too early ➔ False read may happen due to too small difference
If sense_clk arrives too late ➔ Too slow

Isolation transistors: Disconnects sense amp to cutoff large bit line capacitance once sensing starts

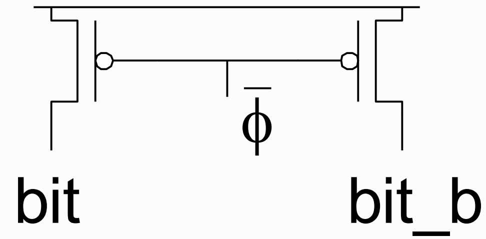
Hierarchical Bit-lines



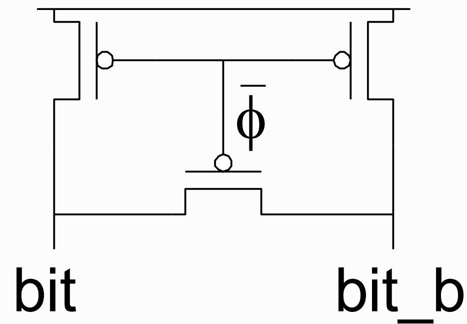
Hierarchical Bit-lines

Pre-Conditioning

Precharge



Equalizer



Question 3

❑Equalizer is required

a) Both the bitlines are pre-charged at the same time
b) To ensure that the bit-lines are conditioned suitably for write operation
c) To minimize offset between the bitlines prior to read operation
d) To improve the hold and read margin of the memory cells