High-Performance SRAM Design

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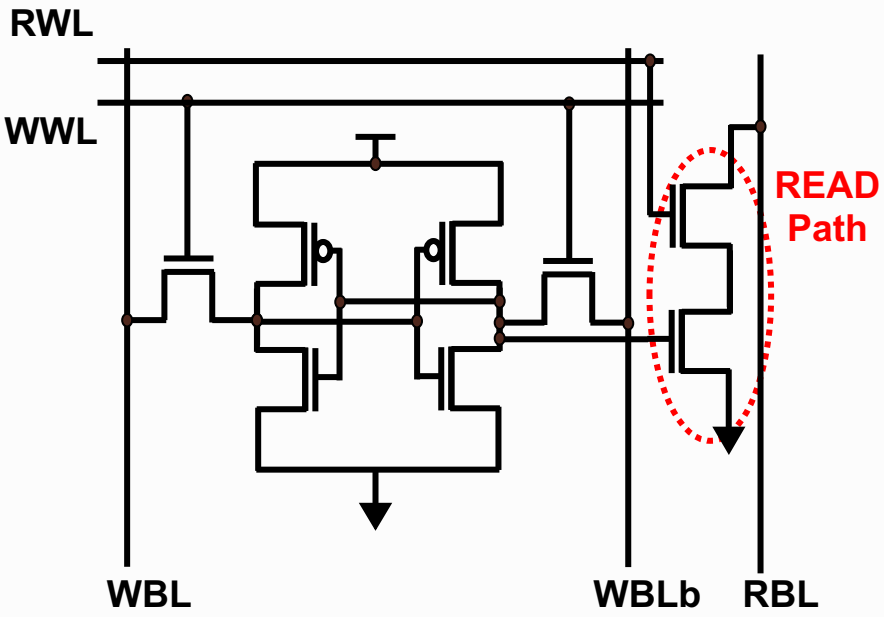
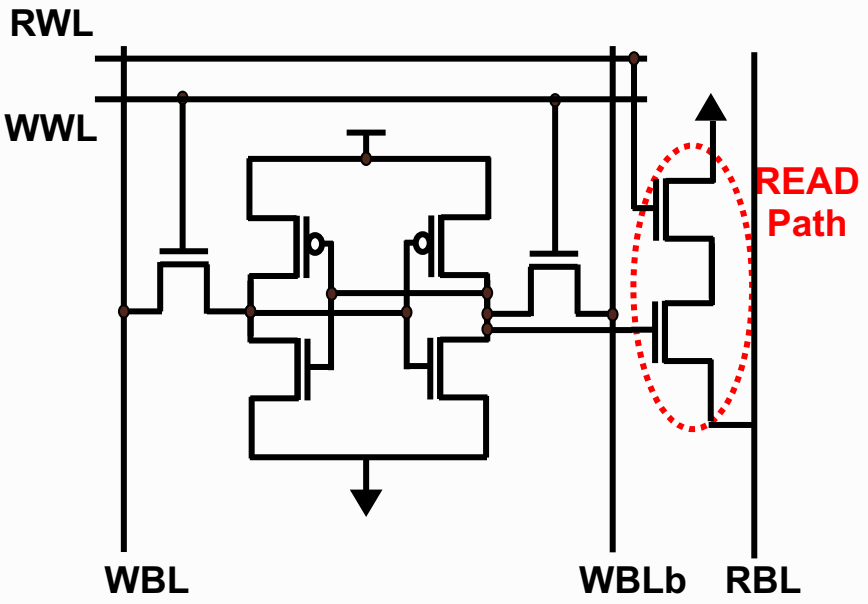
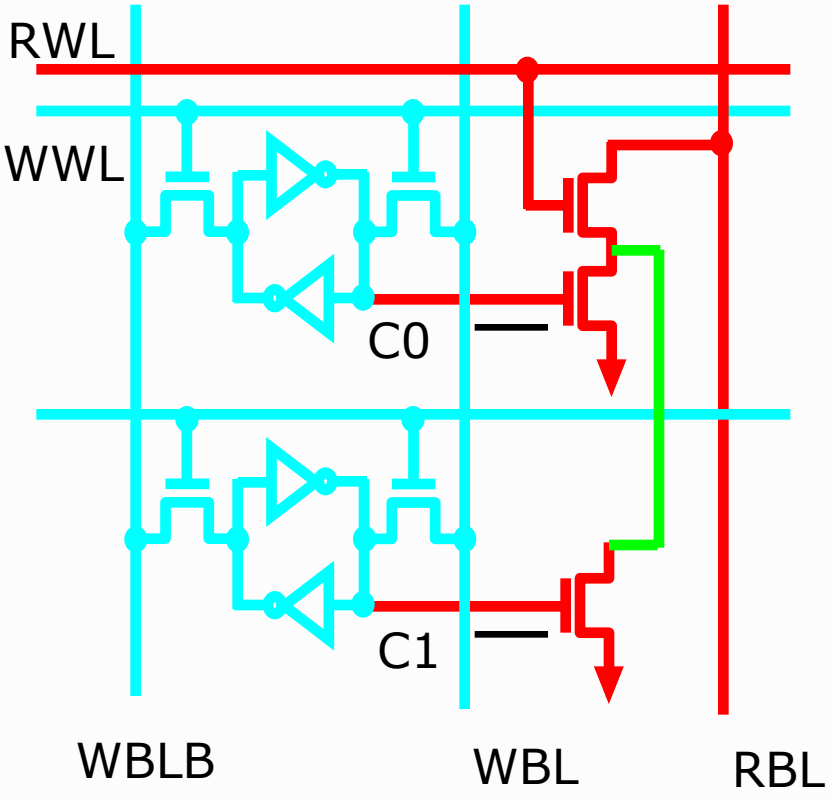
Thought exercise





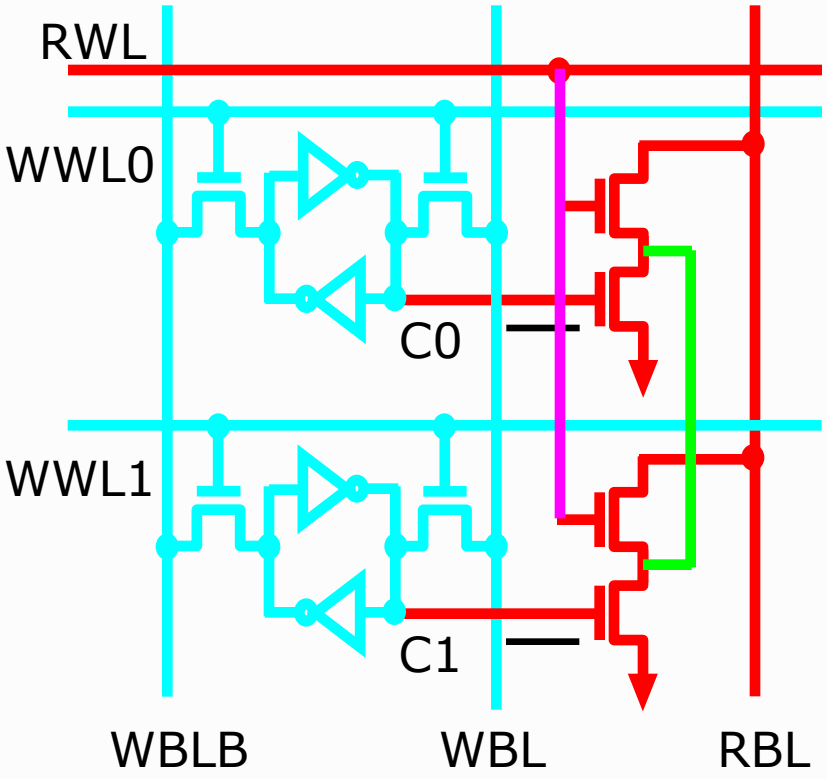
Implement logic function via 8T merge

- Concept: Use the 8-T portion of the cell for implementing logic functions
  - Possible due to decoupling of read and write paths
- RBL discharges when either C0 or C1 is high
  - Read stack remains 2-high
- And function: switch definition of WBL and WBLB
- An OR2 embodiment is shown on right
  - Can be complex OR4, OR8, etc.

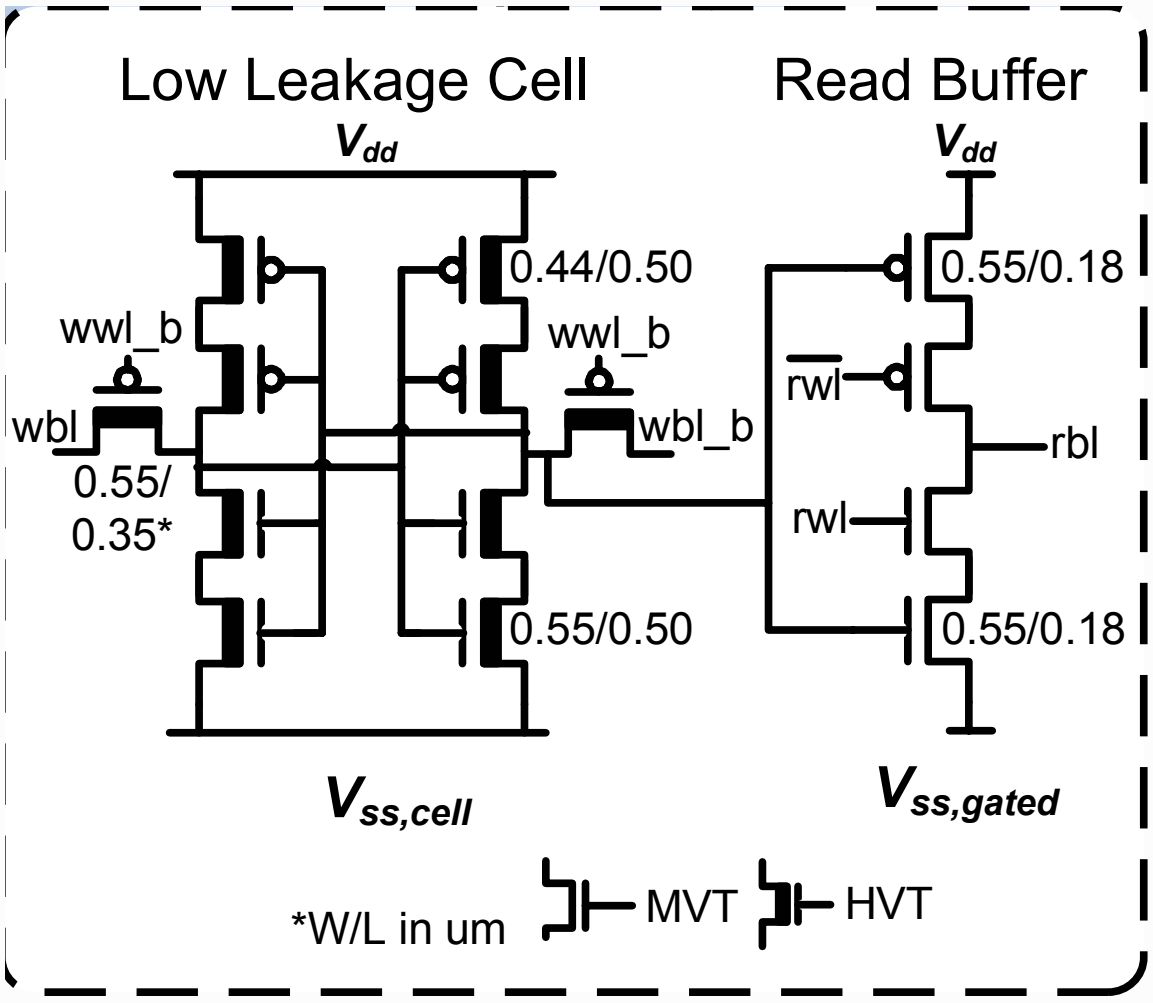


A More Practical Implementation

+ Share RWL between adjacent cells
  => 3 word-lines in 4 metal tracks
  - Reduces coupling capacitance (+ performance and power)
+ All FEOL features identical to conventional 8T cell
  - OR
  - upper device in stack can be made smaller, reducing cell size



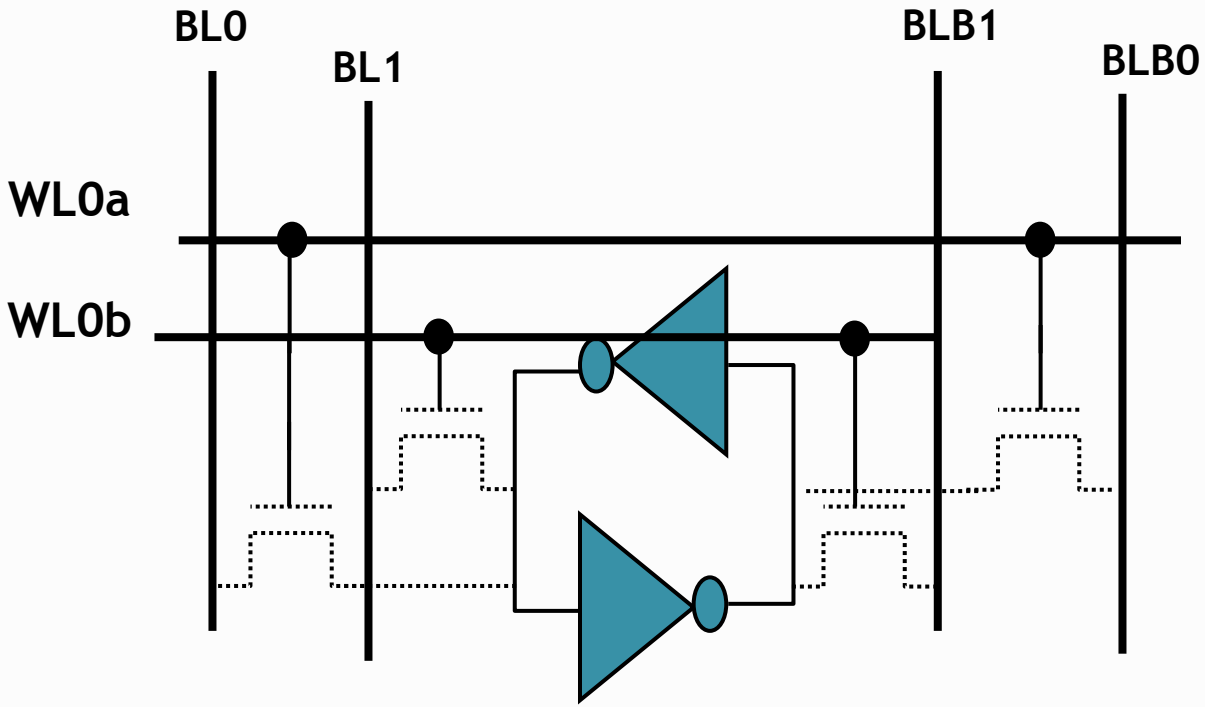
Low leakage SRAM



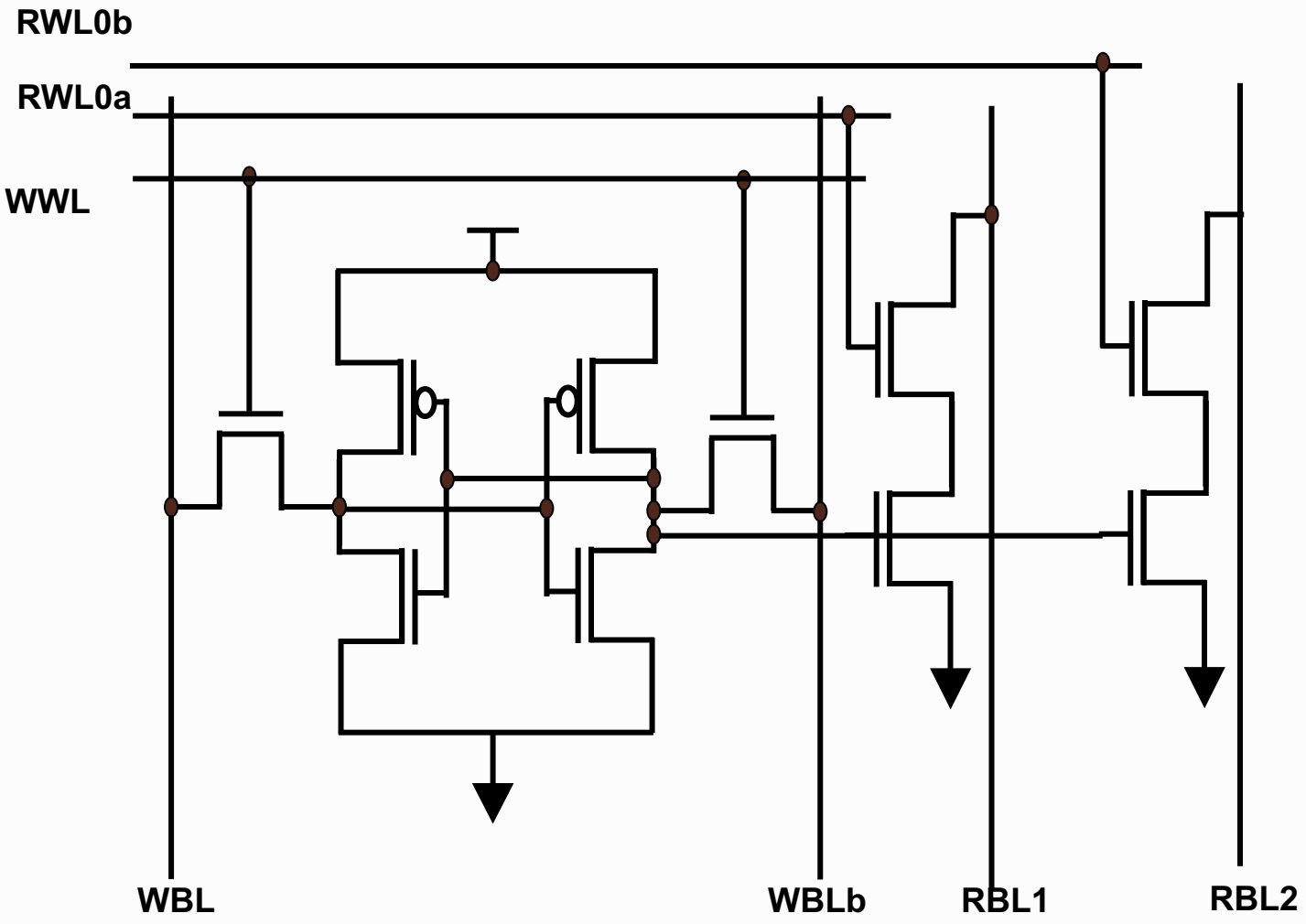
The Phoenix Processor: A 30pW Platform for Sensor Applications

(S. Hanson , VLSI Symp '08)

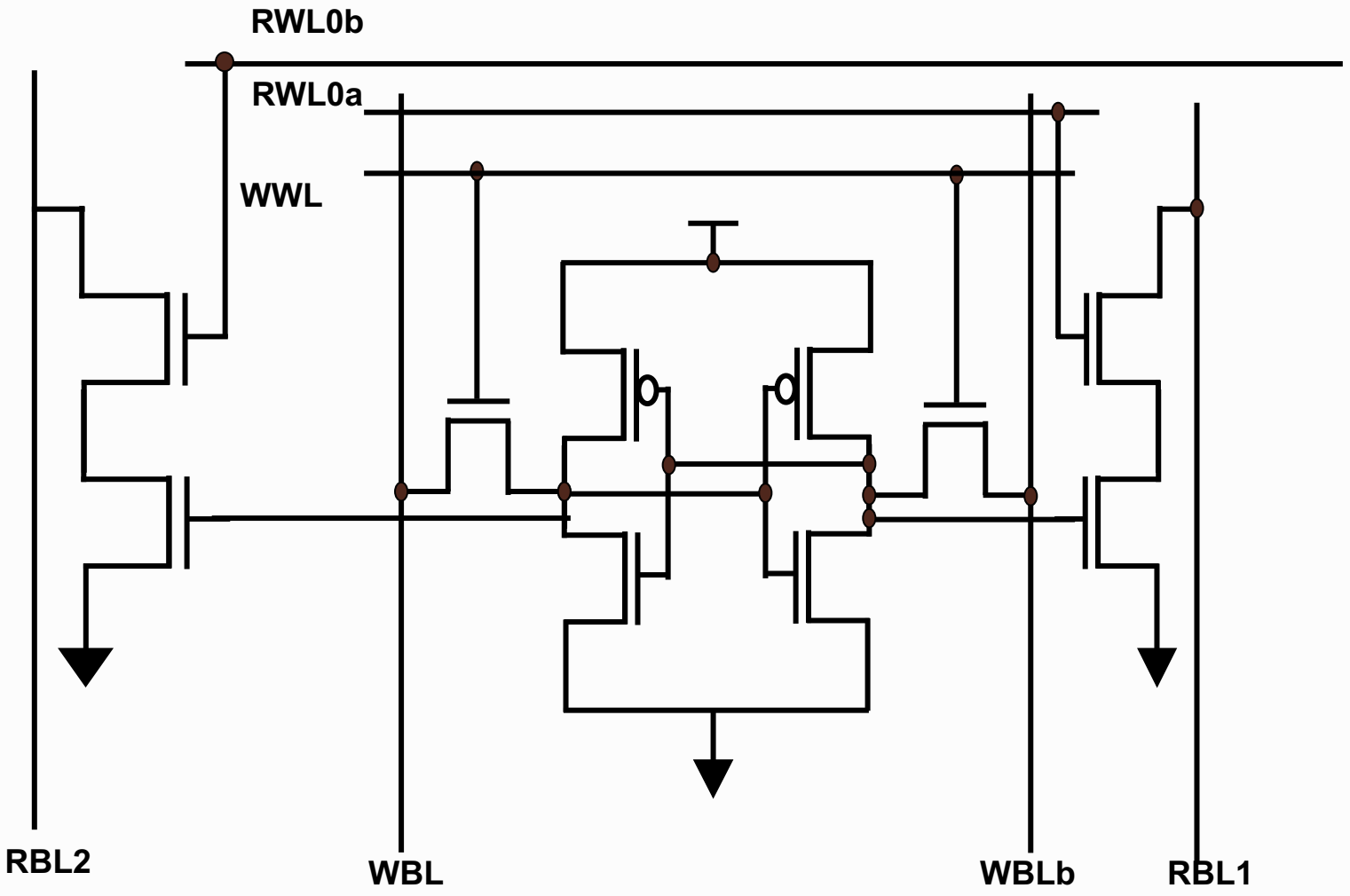
Multi-porting SRAM Cell



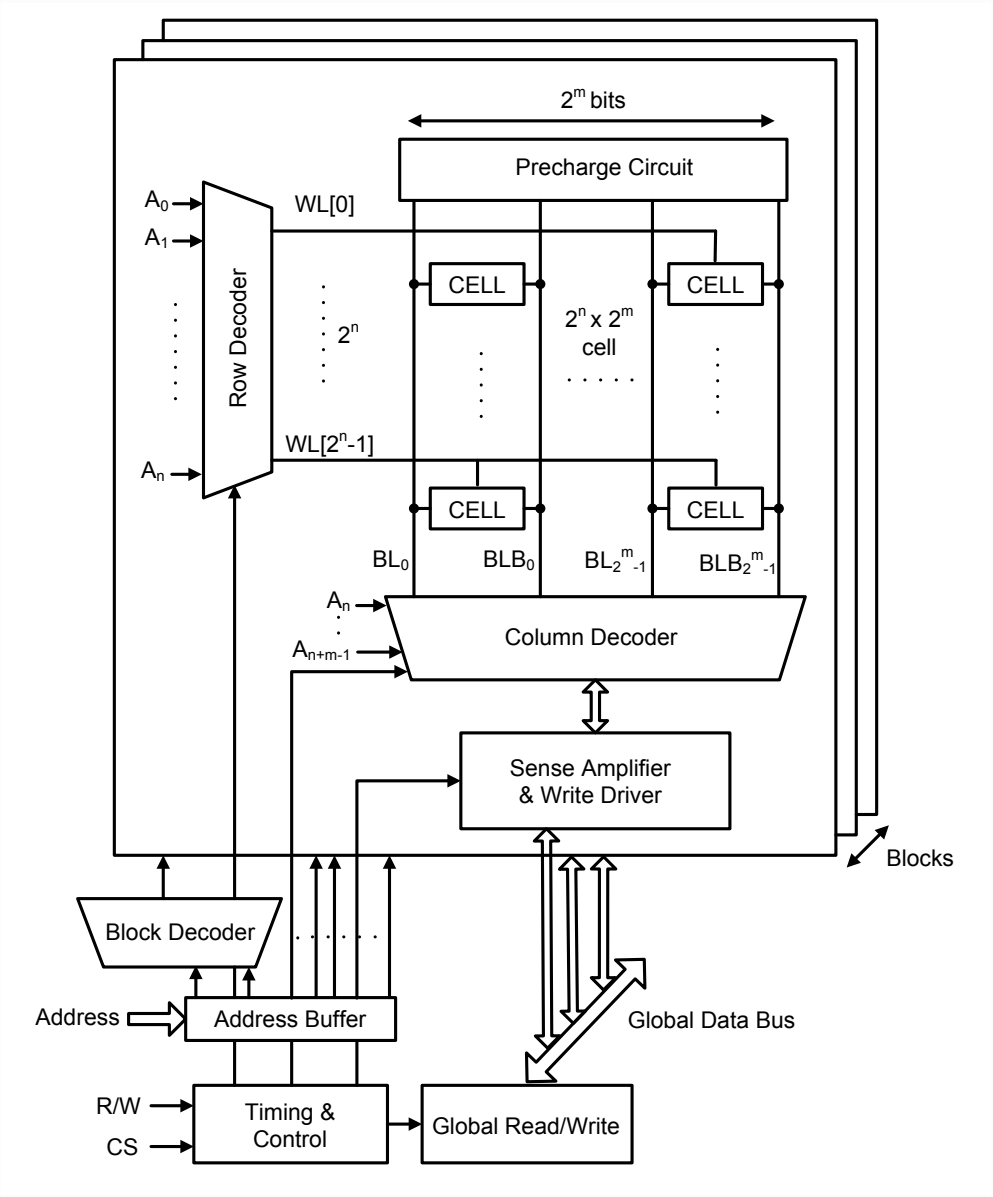
Multi read ports



Multi read ports

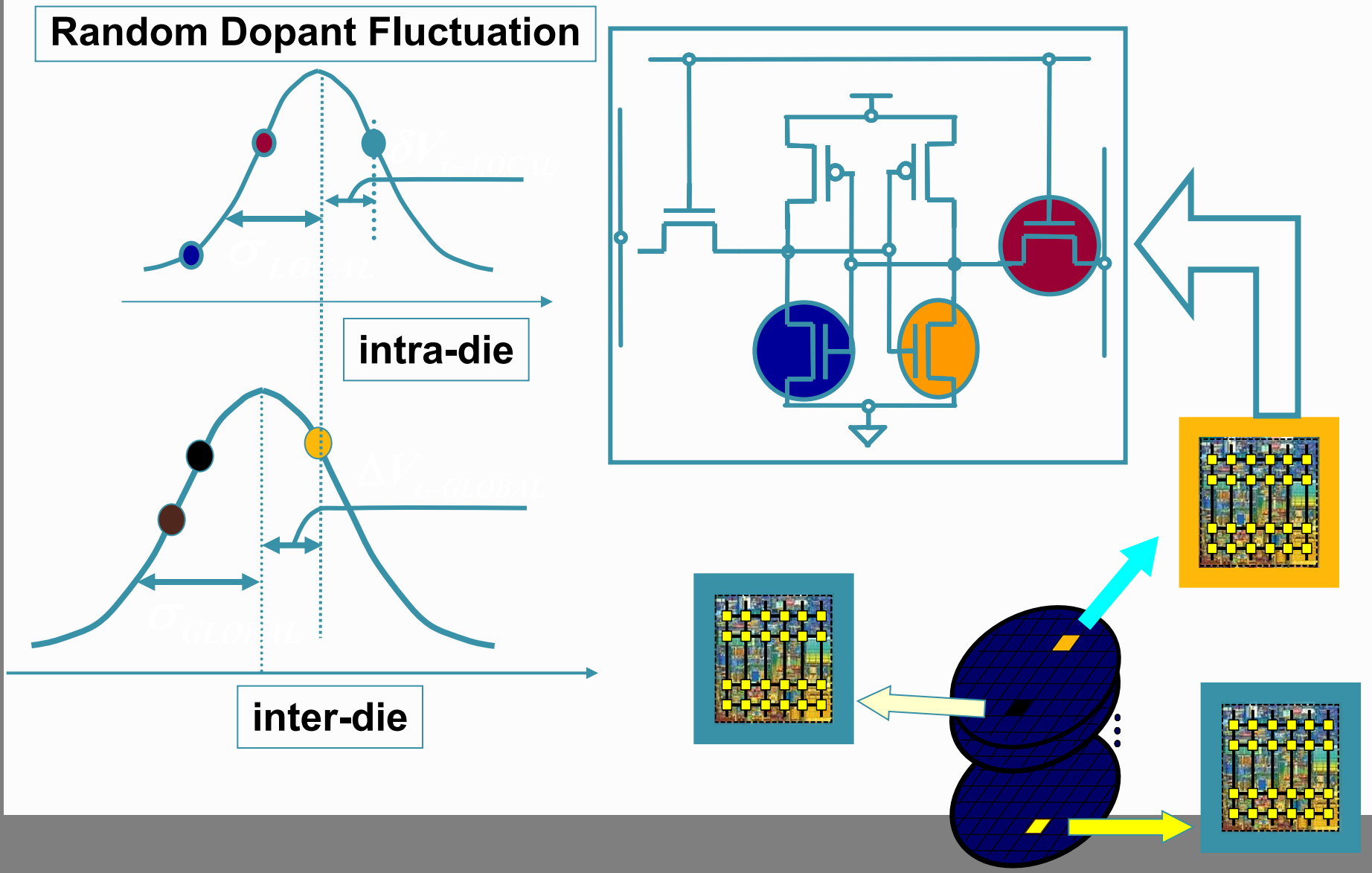


Block Diagram

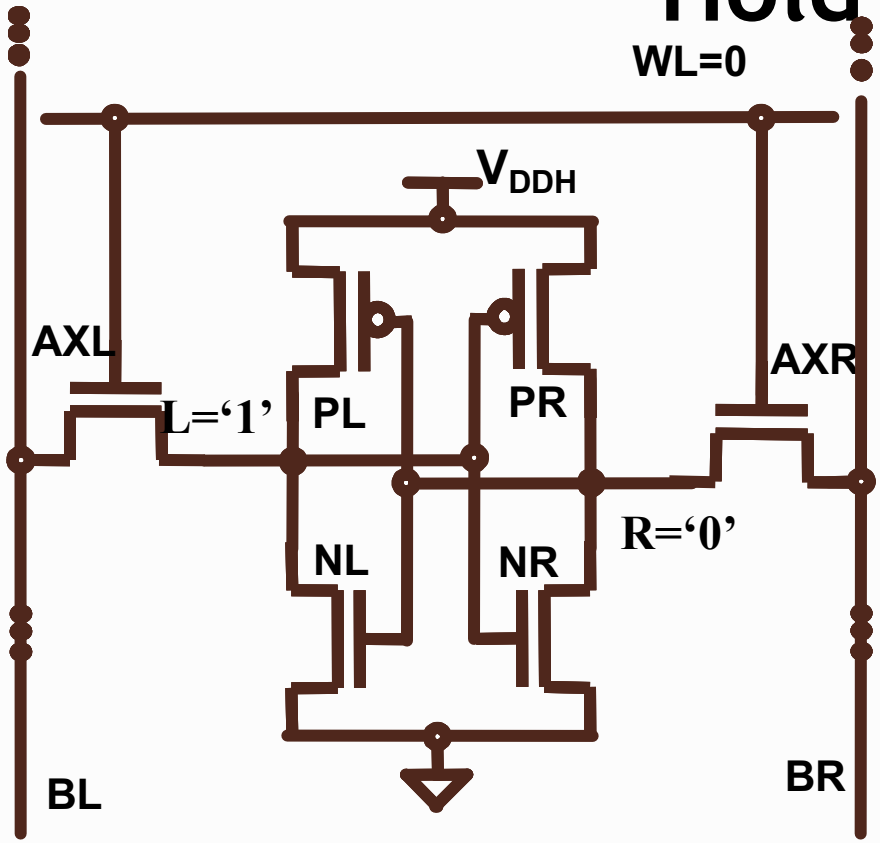


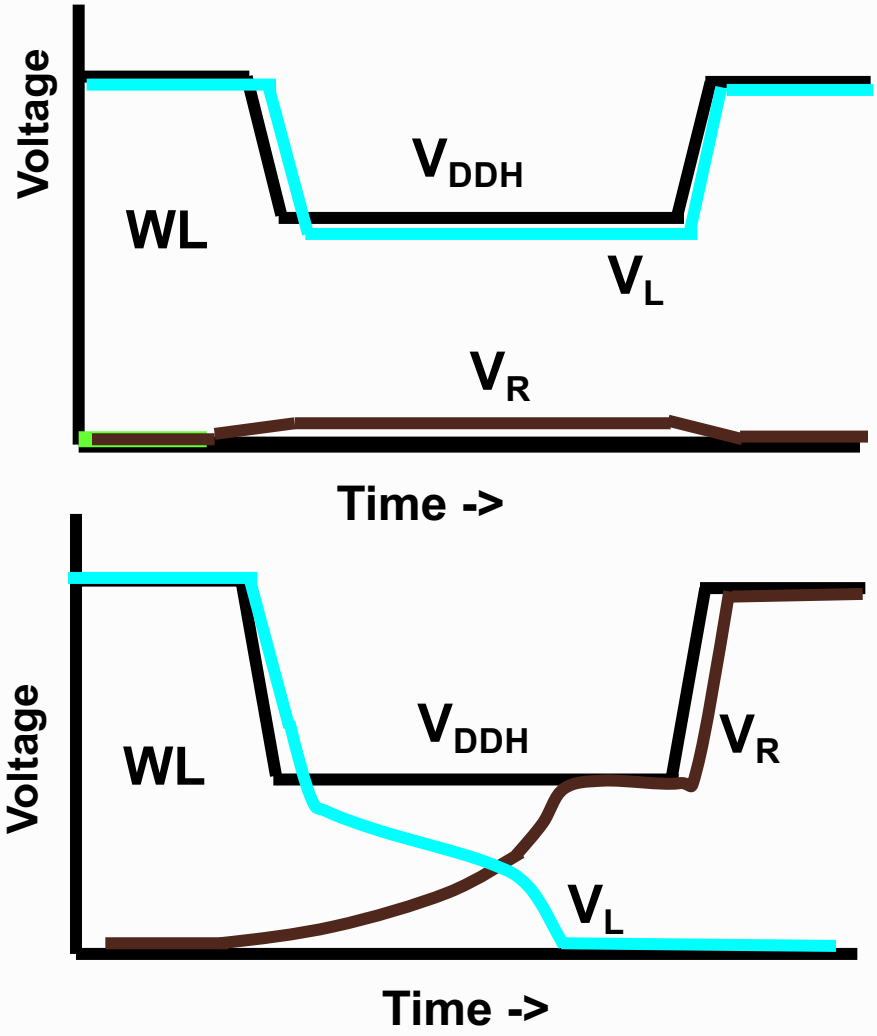
Bank and Bank Conflicts

Global and Local Variations

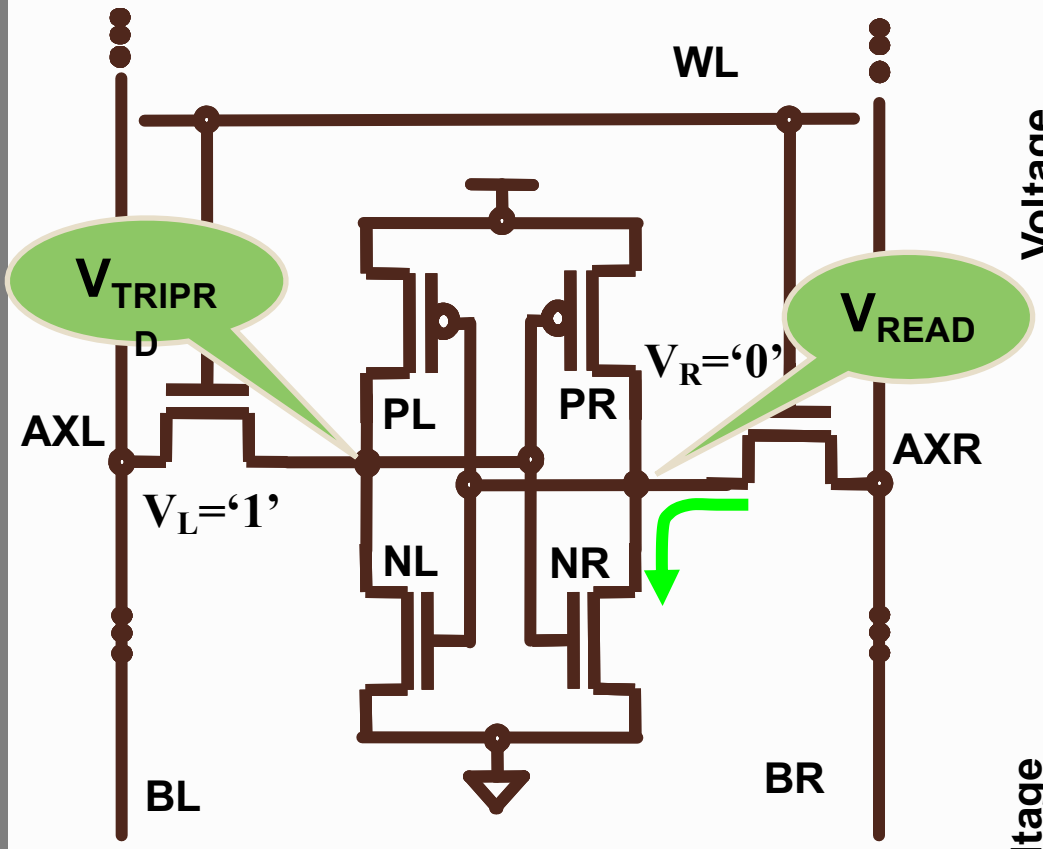


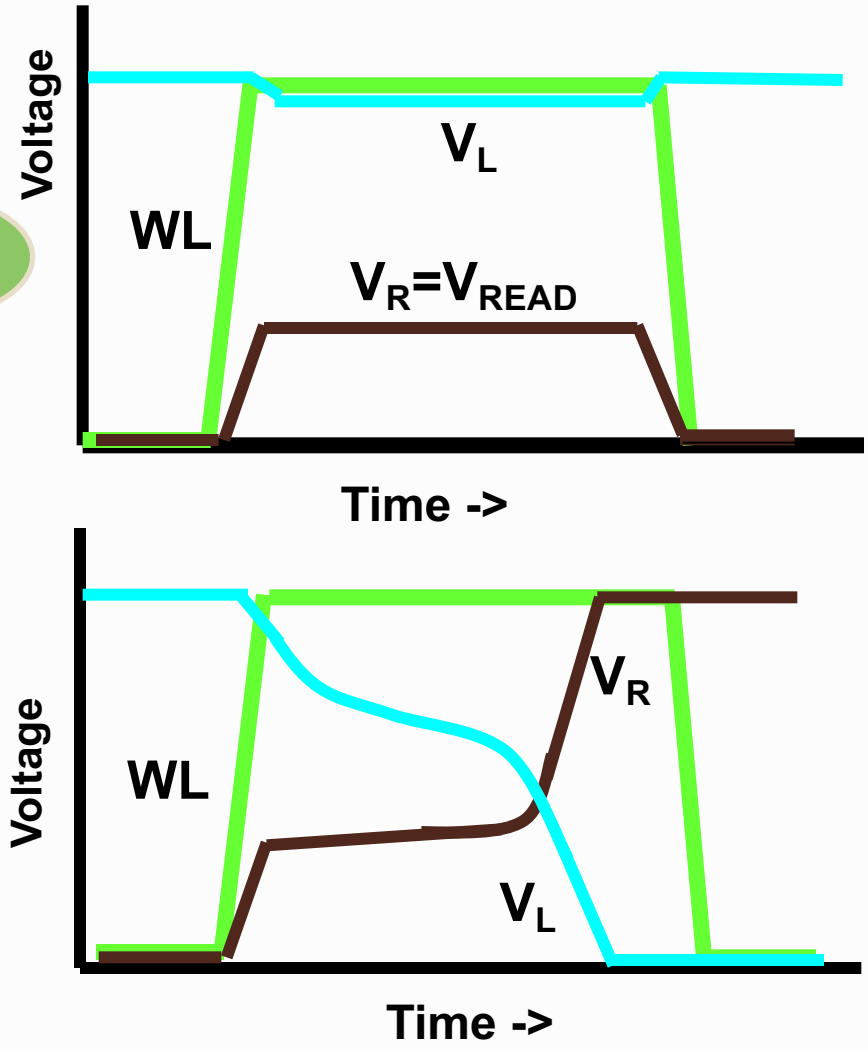
Hold Failure



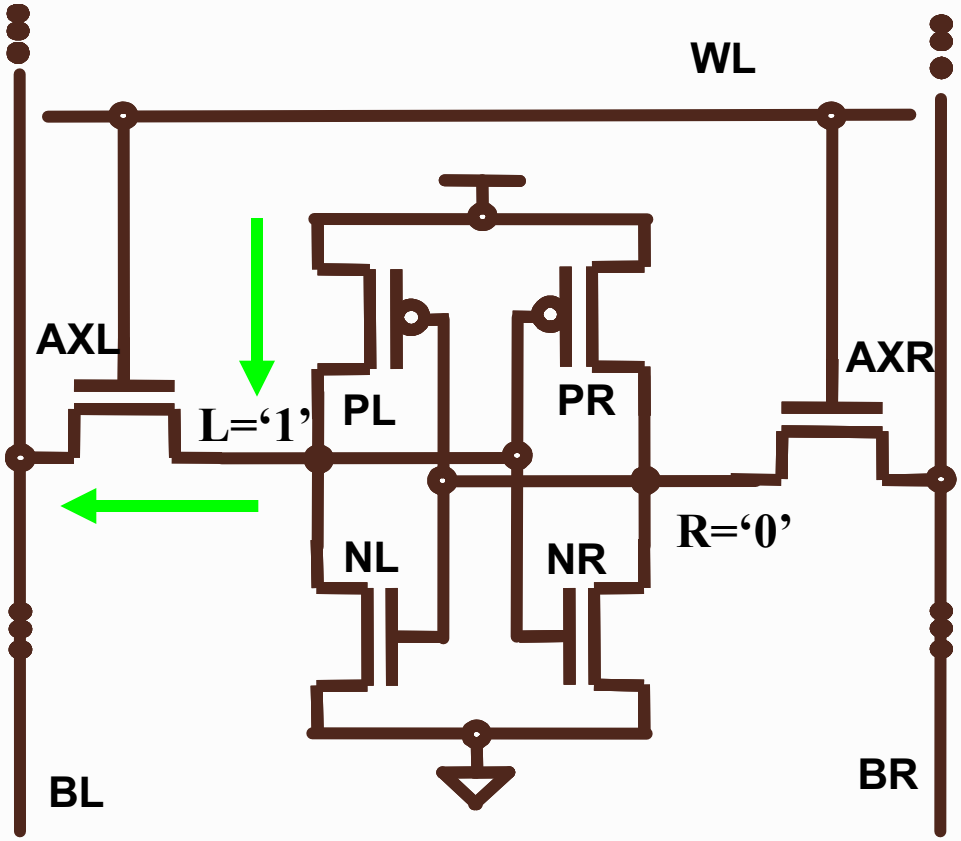


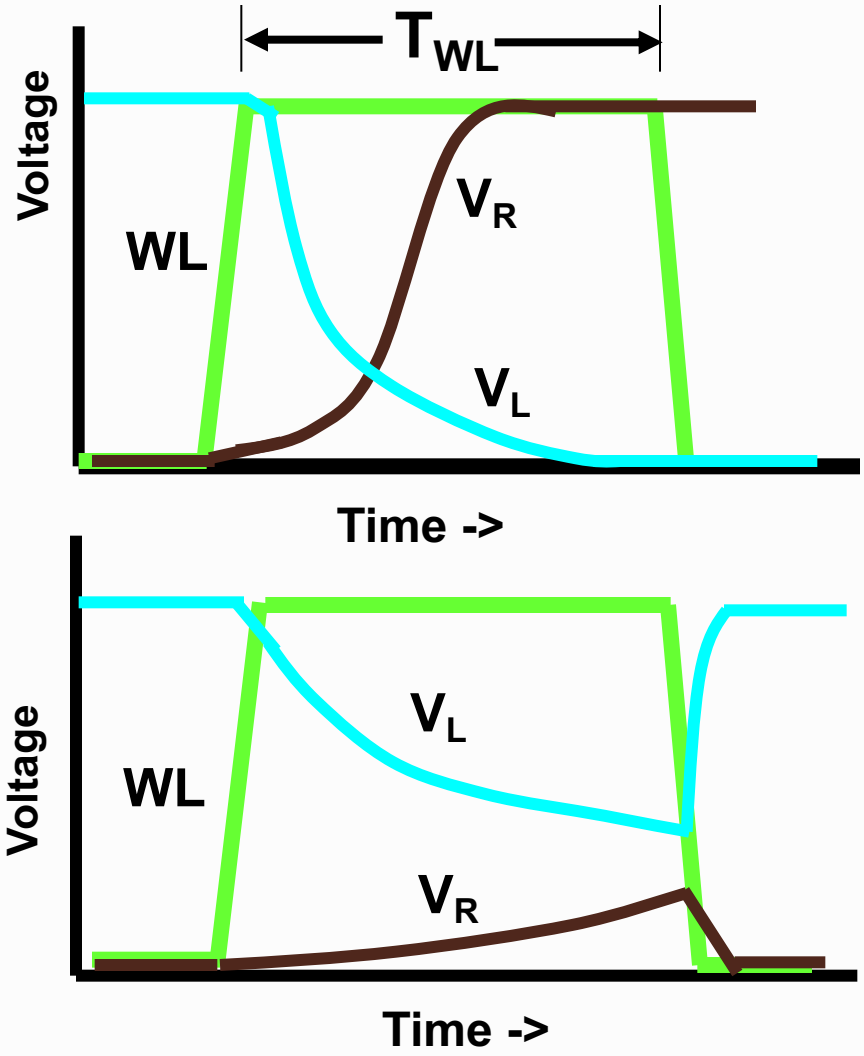
Read Failure



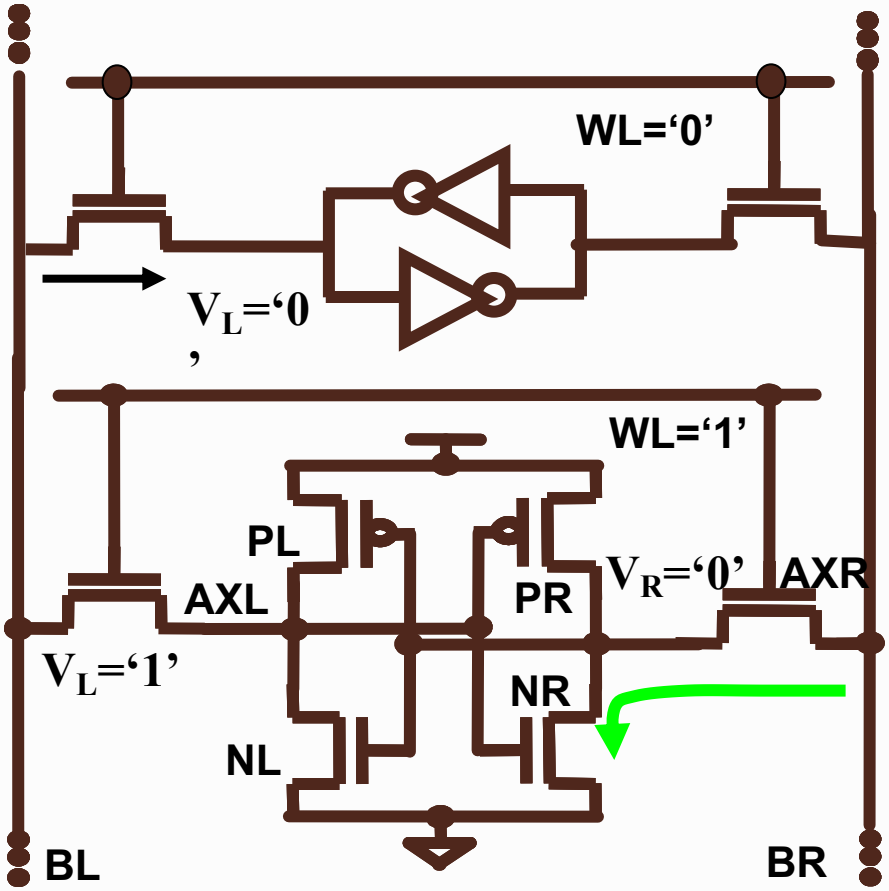


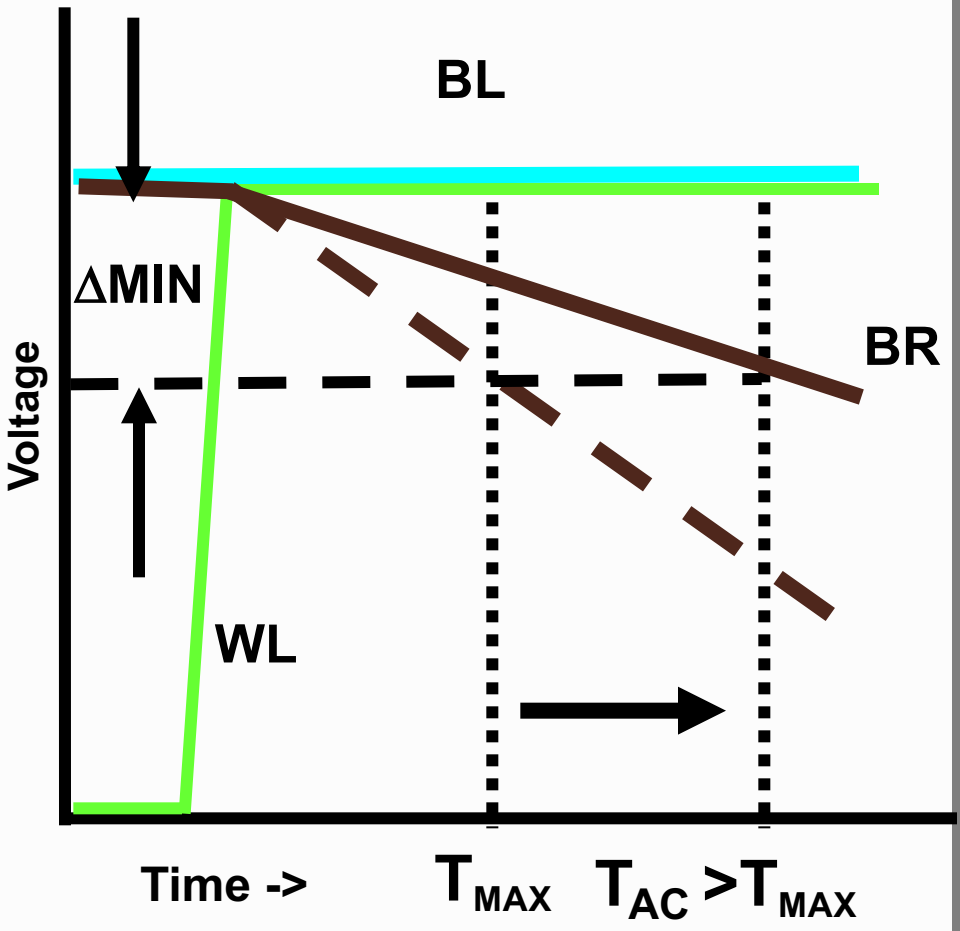
Write Failure



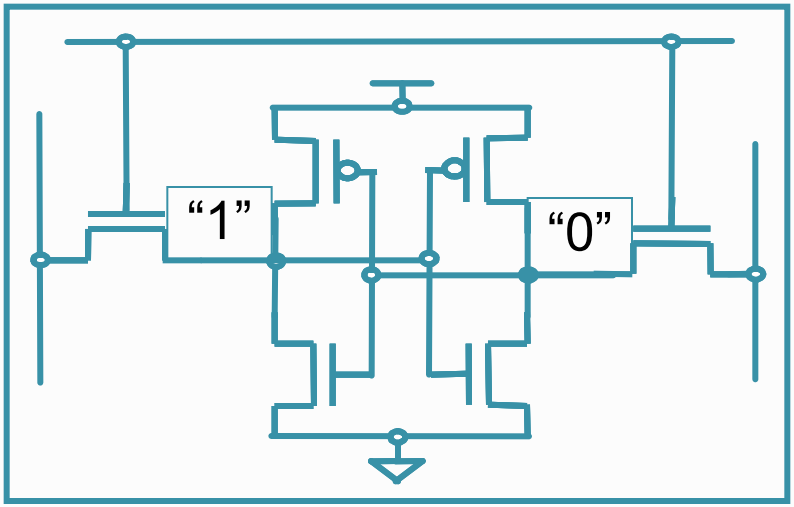


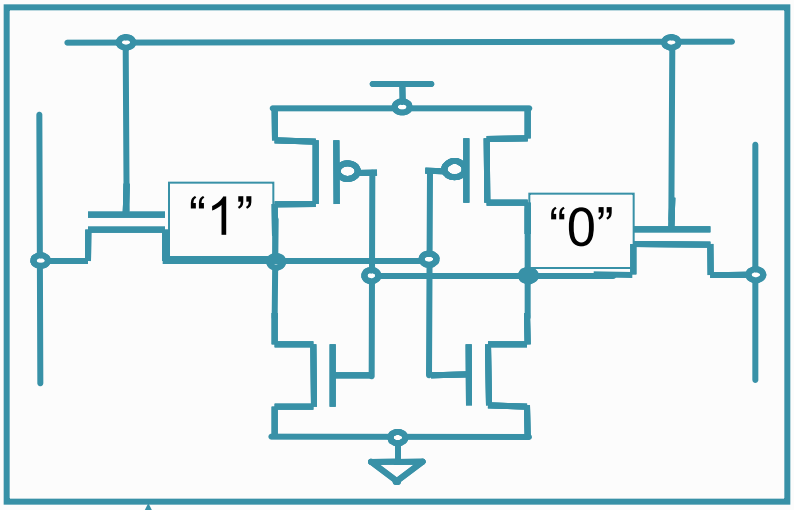
Access Failure

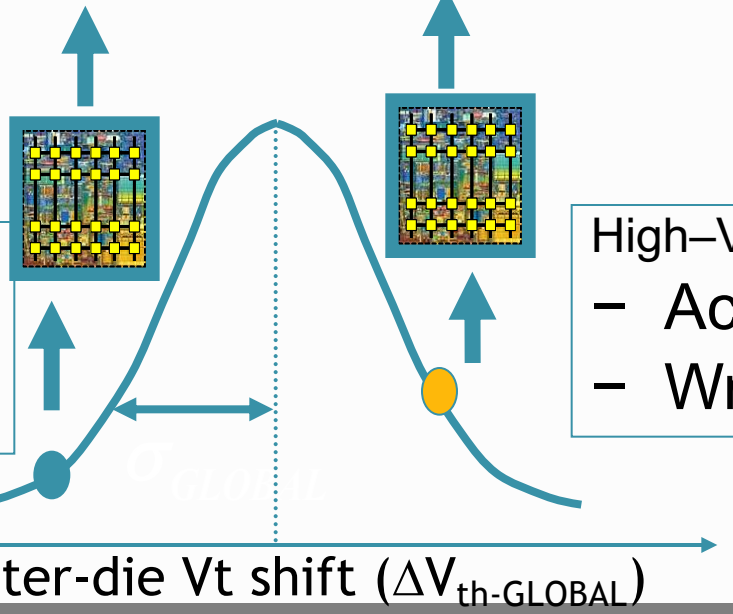




Inter-die Variation & Cell Failures







Low–Vt Corners
- Read failure ↑
- Hold failure ↑

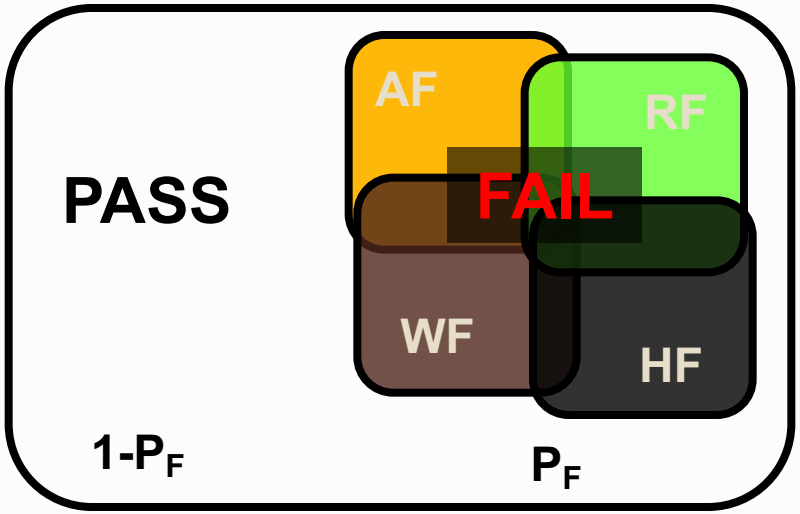
High–Vt Corners
- Access failure ↑
- Write failure ↑

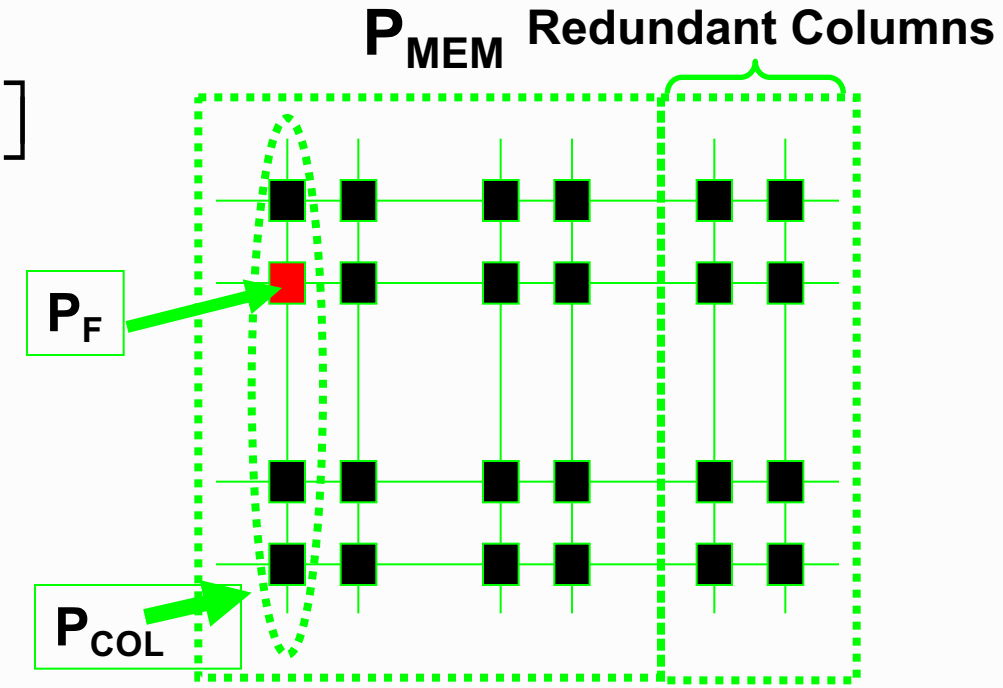
S. Mukhopadhyay et. al, ITC2005, VLSI2006, JSSC2007, TCAD2008

Failures in SRAM Array

Overall Cell Failure:

$$P_F = P[Fail] = P[A_F \cup R_F \cup W_F \cup H_F]$$

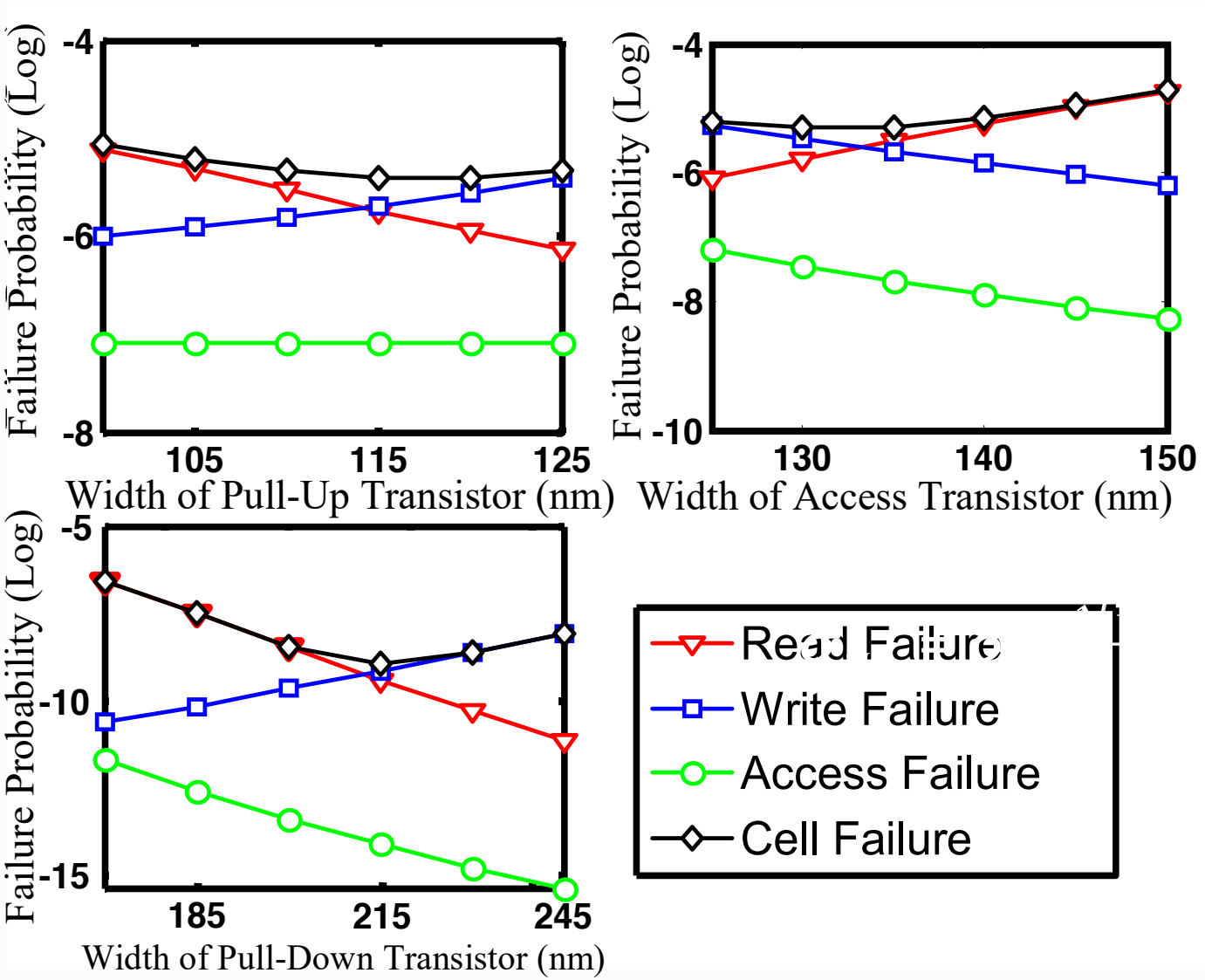




- P_{COL}: Probability that any of the cells in a column fail

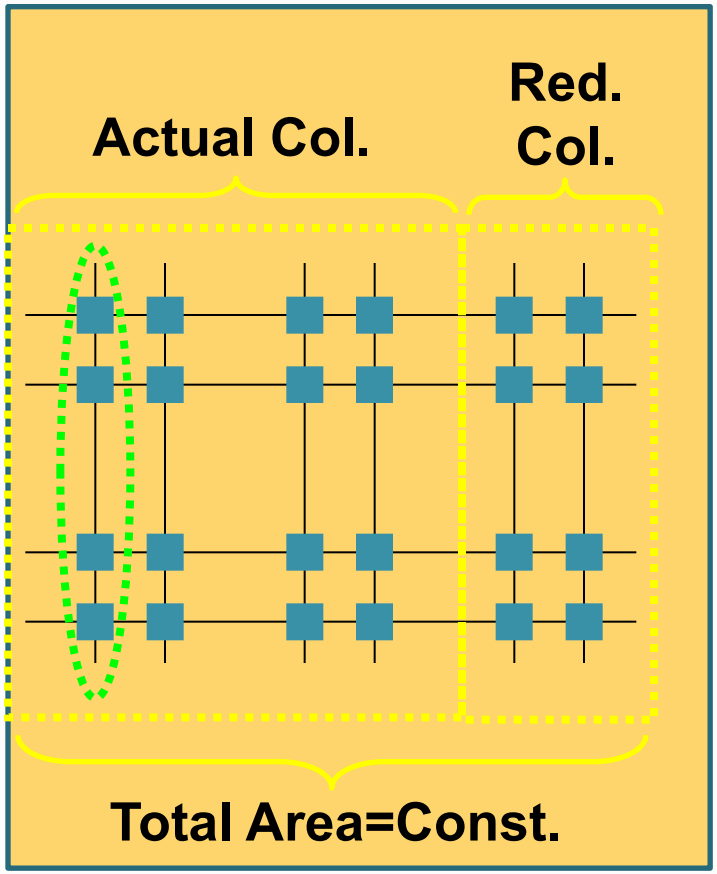
$$P_{COL} = 1 - (1 - P_F)^{N_{ROW}}$$

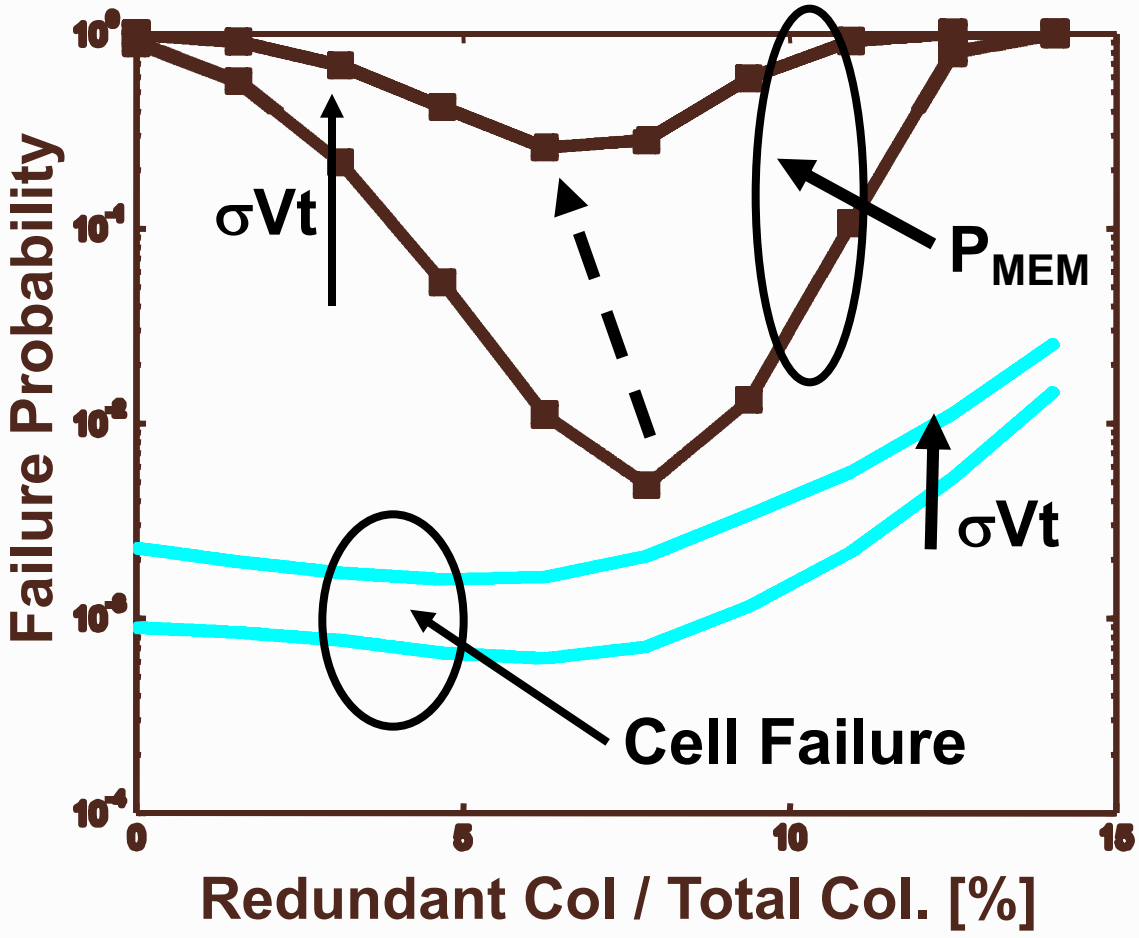
Transistor Sizing



- Slide contributed by K. Roy, Purdue

Impact of Redundancy on Memory Failure





Larger redundancy

(1) more column to replace (less memory failure).

(2) smaller cell area (larger cell failure).

Question

- Array redundancy

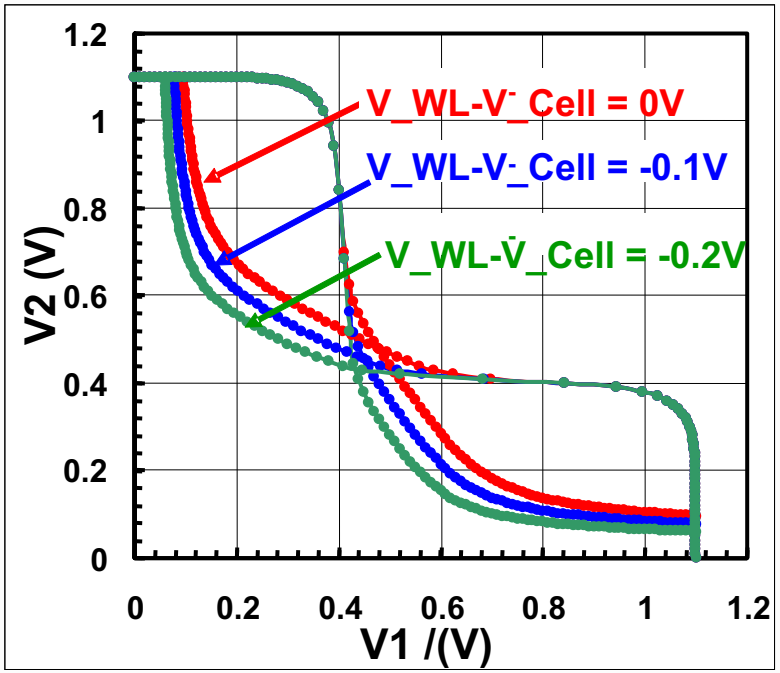
a) Improves cell stability

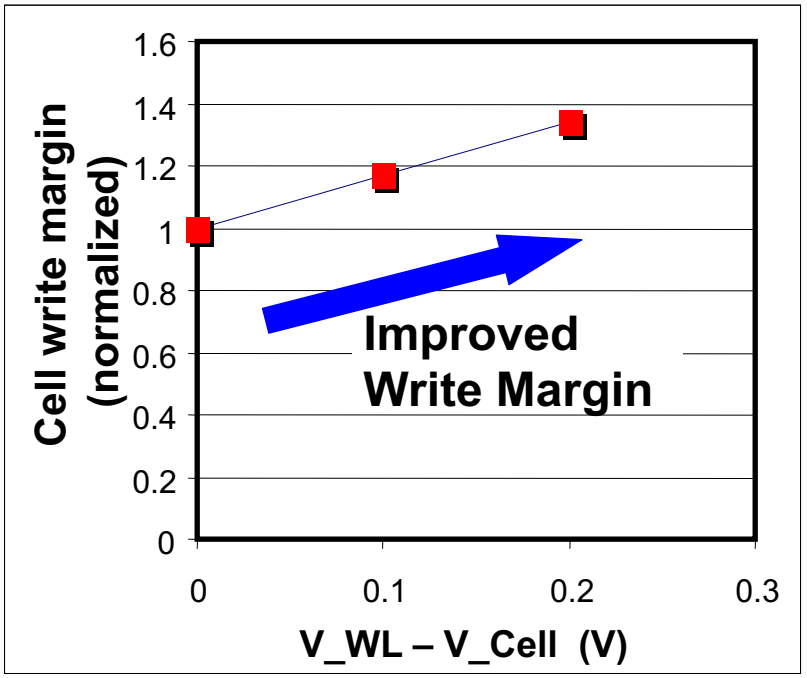
b) Degrades cell performance (i.e increases read and write times)

c) Does not require any change to cell peripheral circuits

d) Row redundancy is better than column redundancy

Example: Multi-VCC for SRAM Cell

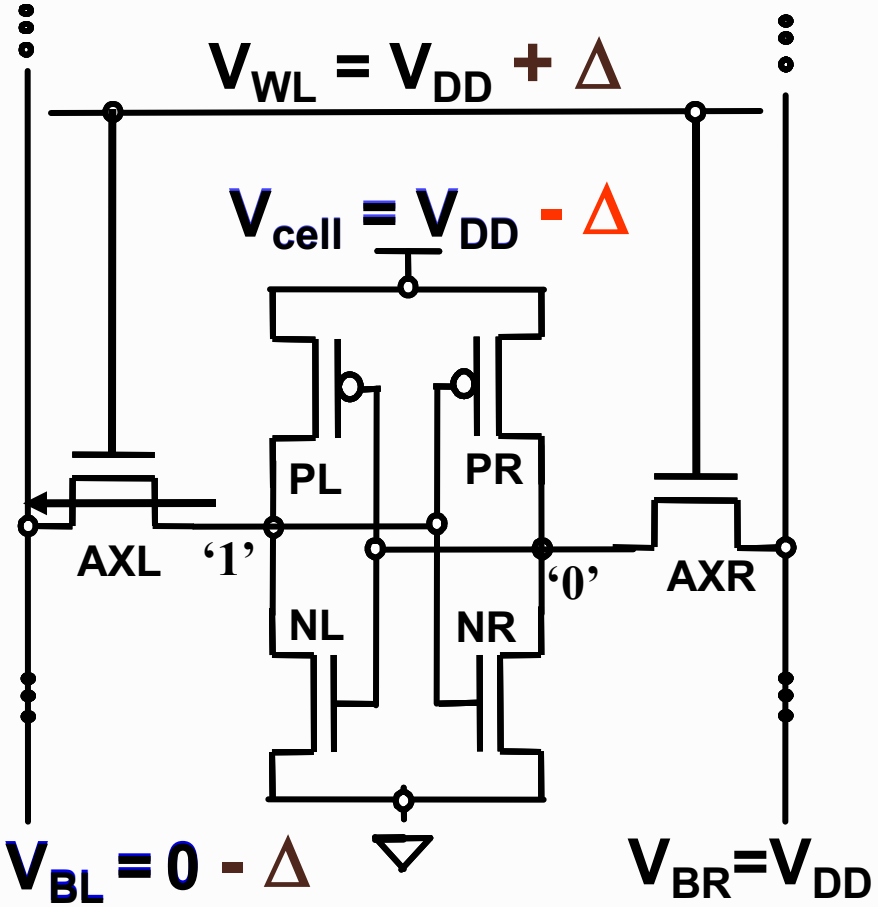




- Create differential voltage between WL and Cell to decouple the Read & Write
  - Write: V_WL > V_Cell
  - Read: V_WL < V_Cell

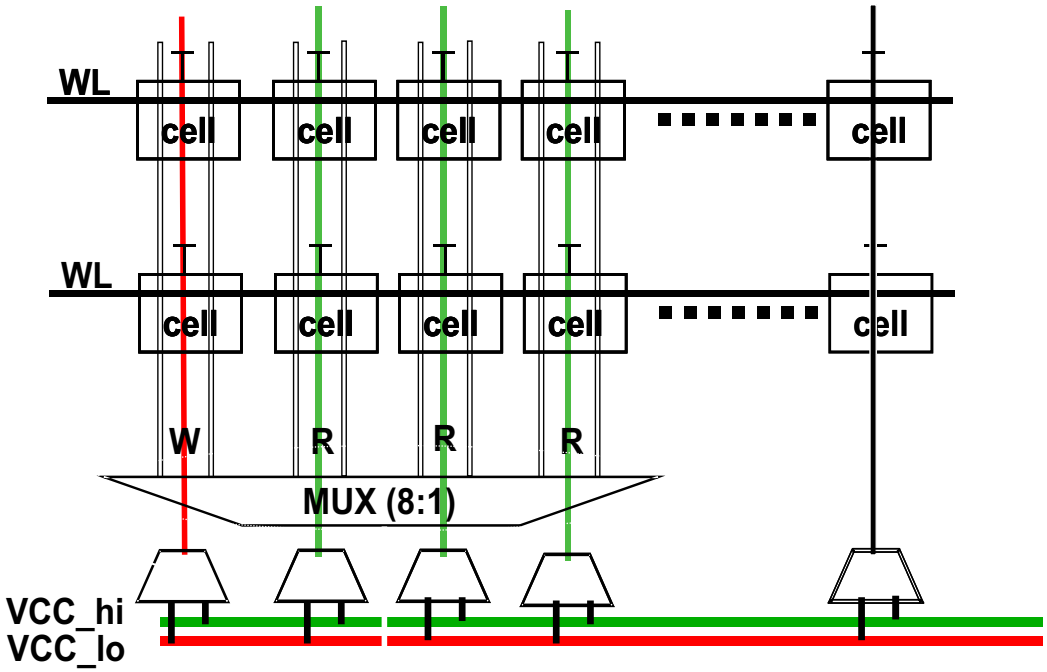
Source: K. Zhang et. al. ISSCC 2005

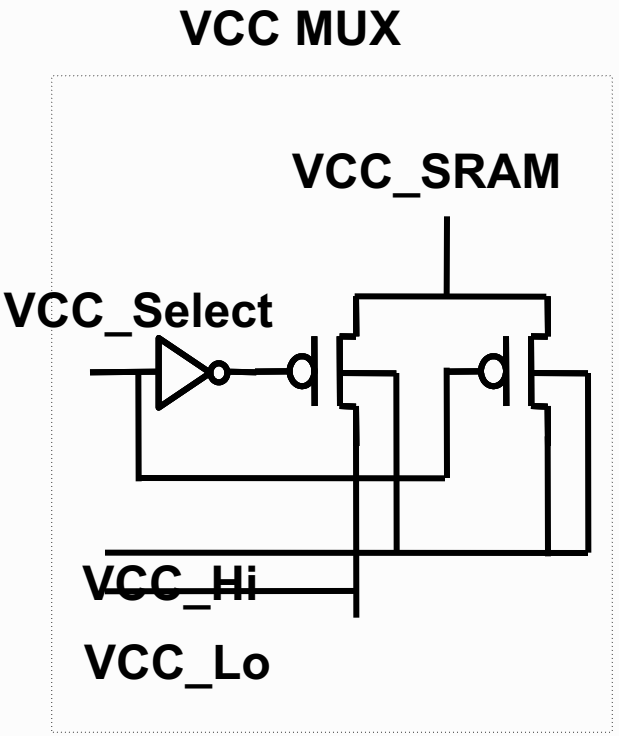
Dynamic Circuit Techniques for Variation Tolerant SRAM



	Read	Write
V_{WL}	Lower V_{WL} => lower V_{read} (weak AX)	Higher V_{WL} => Strong AX helps discharge
V_{cs}	Higher V_{cs} => lower V_{read} (strong PD) Higher V_{trip}	Lower V_{cs} => Weak PUP
V_{BL}	Weak impact	Negative V_{BL} for 0 => strong AX helps discharge

Example: Dual-Vcc based Dynamic Circuit Techniques

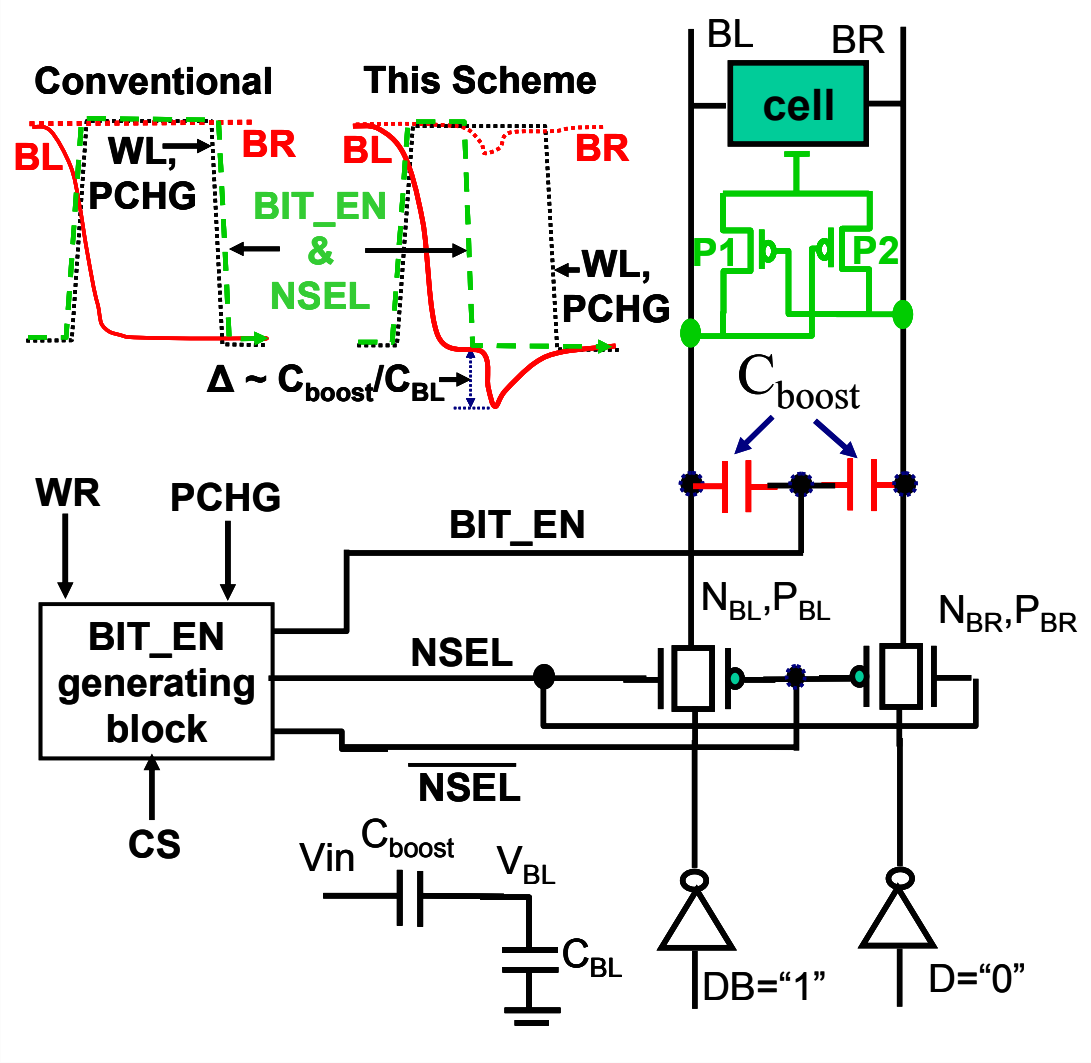




- Dynamic VCC MUX is integrated into subarray
- VCC selection is along column direction to decouple the Read & Write

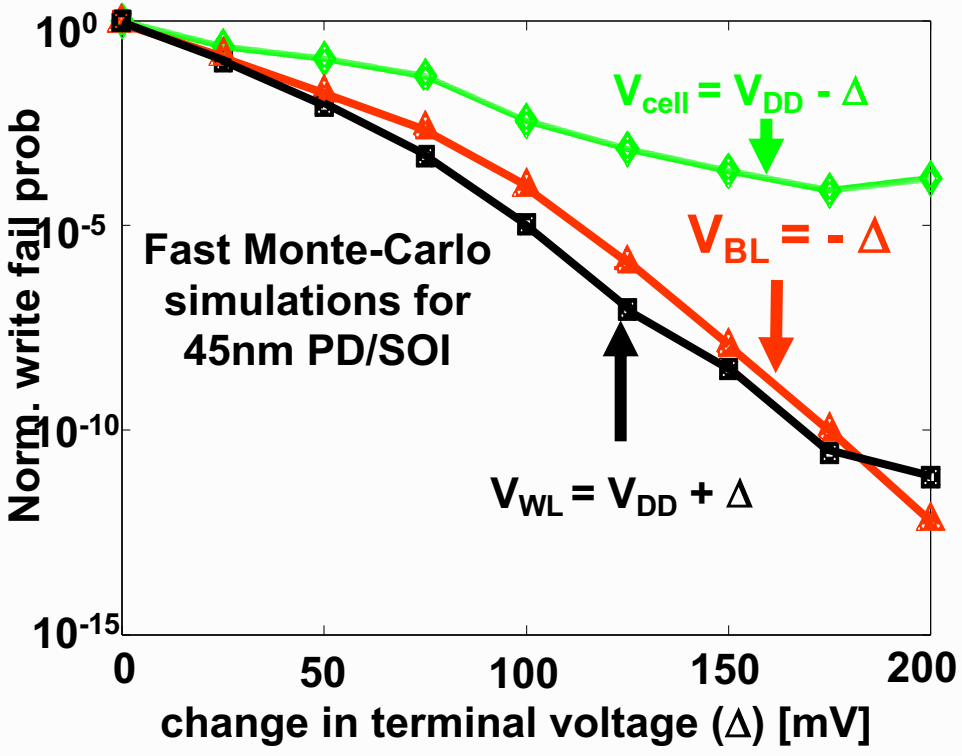
Source: K. Zhang et. al. ISSCC 2005

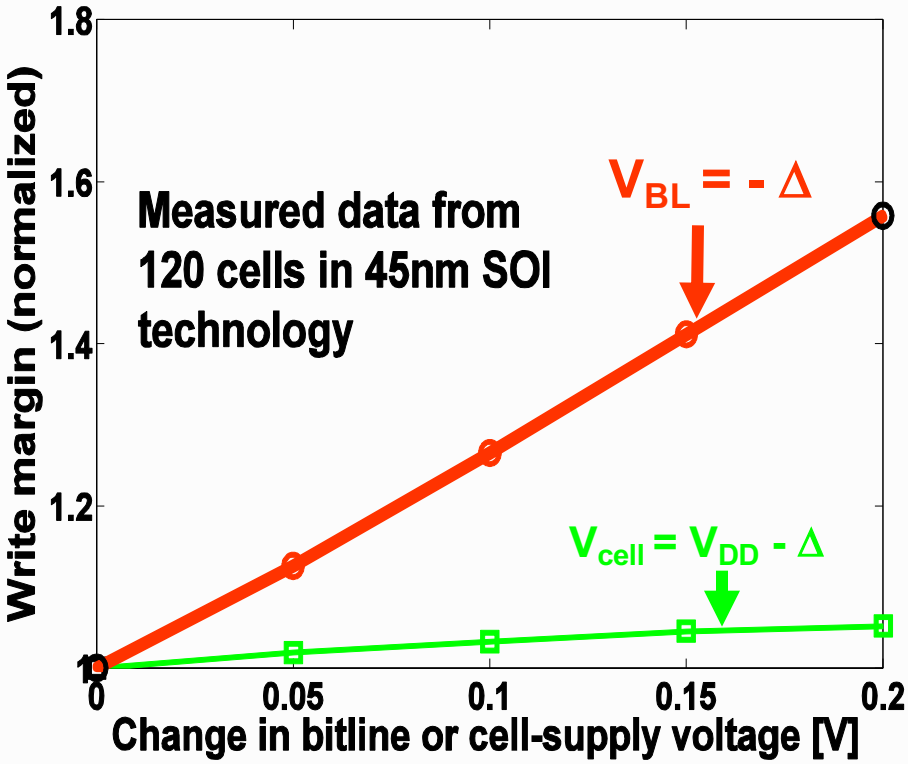
Negative Bit Line Scheme



Source: S. Mukhopadhyay, R. Rao et. al, TVLSI 2009

Effectiveness Considerations: Writability improvement

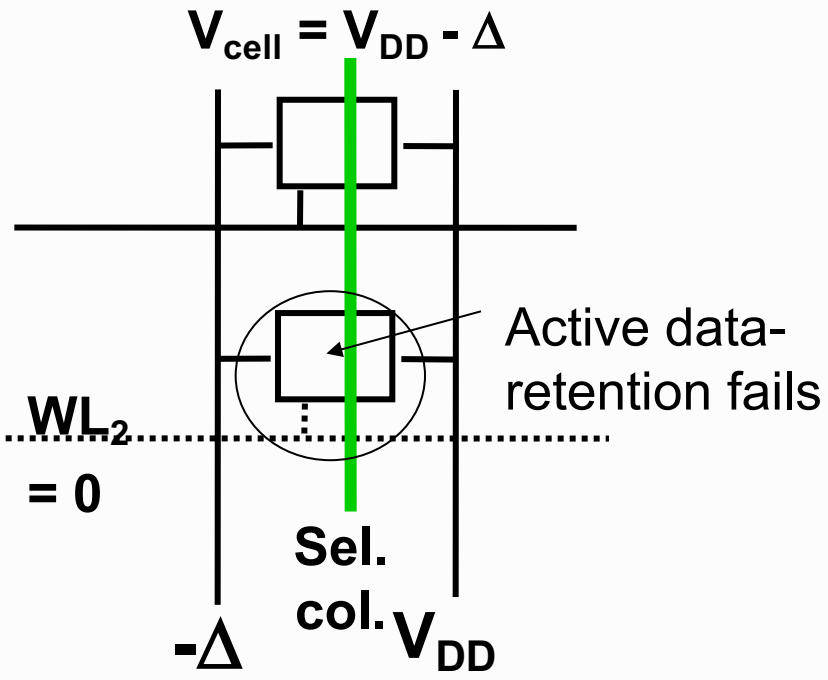


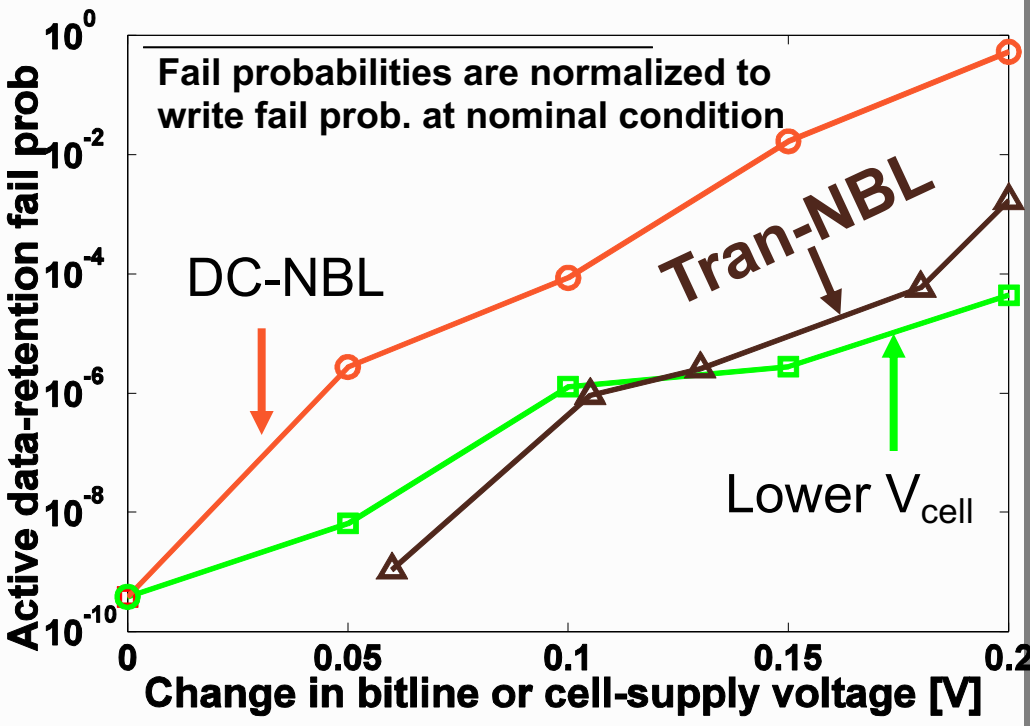


- Various dynamic schemes have different effectiveness in improving writability for similar read stability
  - Higher V_{WL} is most effective

Source: S. Mukhopadhyay, R. Rao et. al, TVLSI 2009

Impact on Active Data-Retention

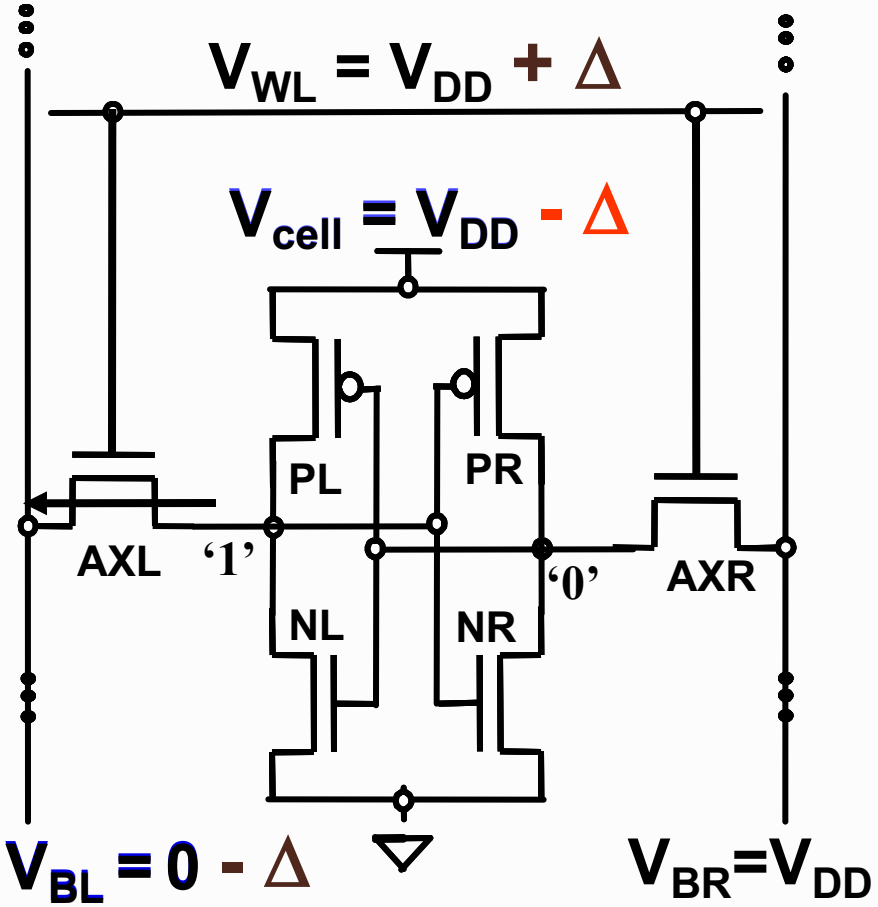




- Column based read-write control adversely impact the active data-retention failures
  - DC negative bitline has higher active data-retention failures
  - Tran-NBL and lower V_{cs} have comparable failure rates

Source: S. Mukhopadhyay, R. Rao et. al, TVLSI 2009

Dynamic Circuit Techniques for Variation Tolerant SRAM



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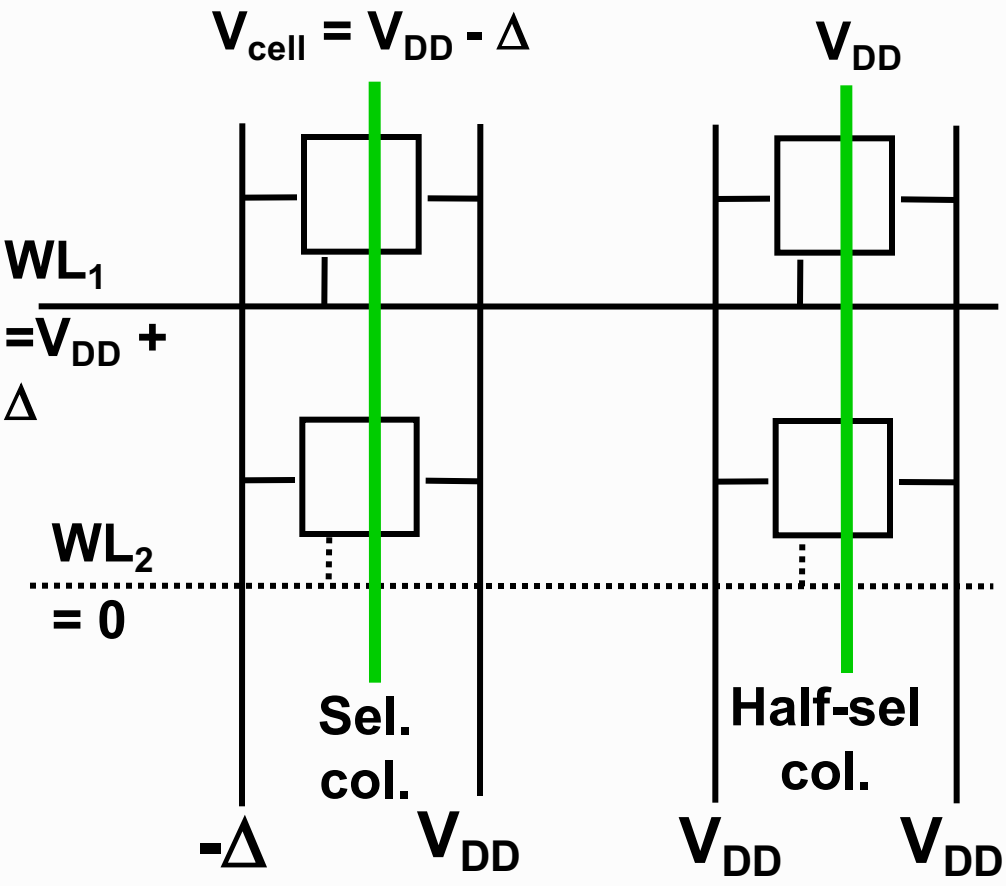
V_{cs}	Higher V_{cs} => lower V_{read} (strong PD) Higher V_{trip}	Lower V_{cs} => Weak PUP
V_{BL}	Weak impact	Negative V_{BL} for 0 => strong AX helps discharge

Implementation Consideration: Half-Select Stability

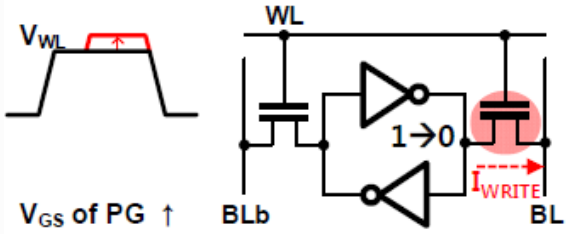


- Higher V_{WL}
  - – Row-based scheme
  - – Degrades half-select read stability of the unselected columns
- Lower V_{cell} or negative bit-line
  - + Column-based scheme
  - + Half-select read stability remains same

Assist Methods

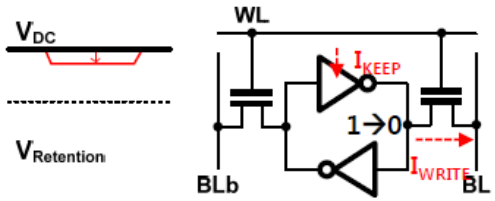
WLOD *(WL Overdrive)*

- Strengthen PG



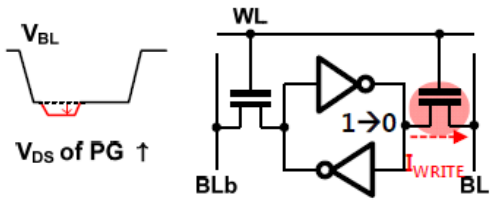
VCDL *($V_{DD,CELL}$ Lowering)*

Weaken PU



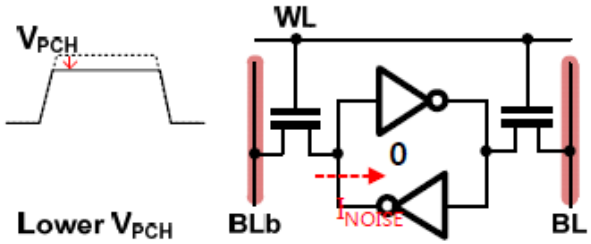
NBL *(Negative BL)*

- Strengthen PG



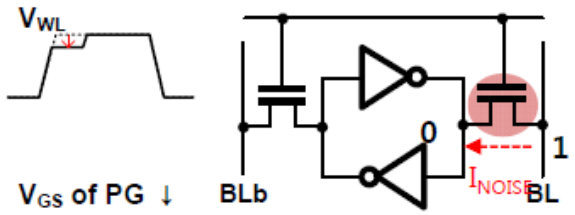
SBL *(Suppressed BL)*

Weaken BL noise



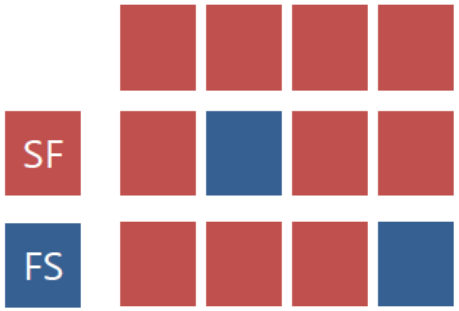
WLUD *(WL Underdrive)*

- Weaken PG

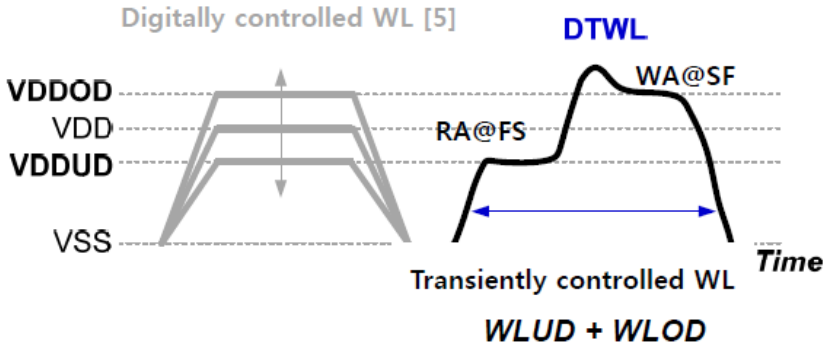


Proposed Dual-Transient WL (DTWL)

- Dual-Transient WL (DTWL) controls WL transiently
- DTWL provides mix-up assist for read and write
  - Covers different process-corner
  - DTWL mitigate the impact of WLOD (WA)



different process-corner



RA and WA

Question

- Of the various assist methods

a) Negative bit line scheme does not help 8-T sram cell

b) Word line under drive does not help 8-T sram cell

c) Word line over drive does not help 7-T conditionally decoupled sram cell

d) VCDL does not help any kind of assymetric sram cell

Precharge Time (Timing diagrams)

SRAM as random number generator